An Accurate Compact Modelling Approach for Statistical Ageing and Reliability

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***Abstract*— In this paper, we demonstrate a compact modelling approach that allows statistical circuit simulation at arbitrary stages of transistor BTI ageing, using advanced compact model generation techniques implemented in the GSS statistical circuit simulation engine RandomSpice. The methodology links statistical TCAD simulations where different 'frozen in time' stages of BTI degradation are described in terms of average trapped charge density and the corresponding statistical compact models, to statistical circuit level simulations where aging is expressed in terms of time. To accomplish this task we employ an ageing model that links the average threshold voltage shift and the corresponding average trapped charge density to the aging time. We also illustrate how this method can be used to study the evolution of the SRAM static noise margin with transistor ageing.**

***Keywords*— Compact model; reliability; Ageing;**

I. INTRODUCTION

Statistical variability in transistor characteristics is a critical issue affecting contemporary bulk CMOS technology. Such variability is introduced by the discreteness of charge and granularity of matter. In addition to 'static' variability arising from Random Discrete Dopants (RDD) [1] [2], Line Edge Roughness (LER) [3] and Poly/Metal Gate Granularity (P/MGG) [4], 'dynamic' variability arising from trapping of carriers in interface and oxide defect states is also of great concern. Furthermore, it has been shown that the interaction between static and dynamic variability can lead to significant performance degradation and functionality loss [5].

Transistor stress varies during circuit operation, depending on the activity of the circuit in question. As a result, electrons (or holes) trapped in defect states in the gate oxide can accumulate over time, progressively affecting circuit performance and functionality. Accumulation of trapped charge over time due to stress leads to time-dependent BTI degradation (ageing), a component of which is non-recoverable as charge becomes permanently trapped in the oxide.

In this paper, we demonstrate a compact modelling approach that allows circuit simulation at arbitrary stages of transistor ageing, using advanced statistical compact model generation techniques implemented in the GSS statistical circuit simulation engine RandomSpice. In order to connect statistical TCAD simulations and compact models, where stress is described in terms of average trapped charge density, with the circuit level simulations, where stress is expressed in terms of time, we employ an ageing model that links the average threshold voltage shift and the corresponding average trapped charge density to the degradation time. We also demonstrate how the model can be employed to evaluate the impact of ageing on SRAM cell.

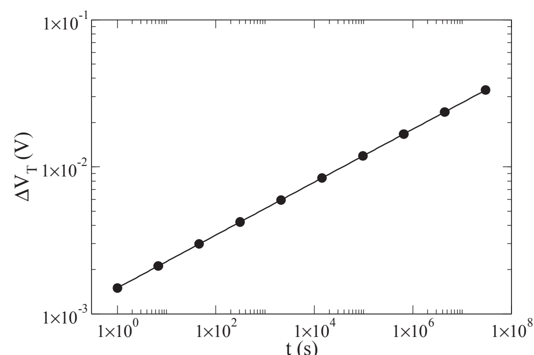

Fig. 1. Time dependent drift of ΔV_T.

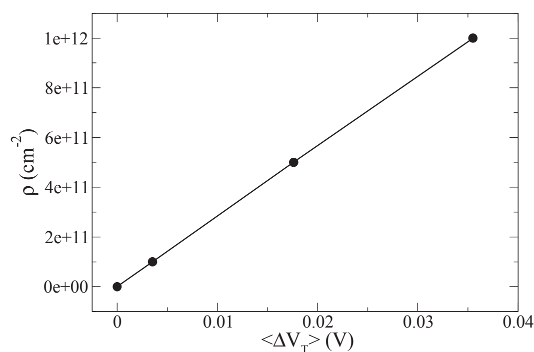

Fig. 2. Trapped charge density as a function of average ΔV_T.

II. PHYSICAL SIMULATION

In this study, a 25nm 'template' bulk MOSFET that meets the requirements of the 22/20 nm CMOS technology generation is used. In order to extract accurate compact models, statistical physical simulations were performed using the GSS 'atomistic' 3D TCAD simulator GARAND [6], in the presence

of three sources of statistical variability: Random Discrete Dopants (RDD), Line Edge Roughness (LER), and Metal Gate Granularity (MGG) and at trap densities of 0 (“fresh devices”), 1e11, 5e11, and 1e12 cm^{-2} respectively. Statistical compact models have been extracted from these simulations using Mystic [6] in order to provide inputs to the device model generation technology implemented in RandomSpice.

III. AGEING MODEL

The TCAD simulations for this study have been performed at specified conditions in terms of the average trapped charge density per unit area, rather than explicitly in terms of stress time. In general it is the stress time, rather than the trapped charge density that is readily available in the circuit level simulations. Consequently we have incorporated a relatively simple aging model in RandomSpice to map the stress time/age into an average charge density.

We assume a power law describing the dependence between stress time and ΔV_T, as observed experimentally in [7][8]. Using the results from physical simulation, we then extract the relationship between average ΔV_T and charge density. The power law coefficients are selected such that the simulated average charge densities (1e11, 5e11 and 1e12cm^{-2}) span the range of approximately 1 μs to 1 year, as illustrated in Fig. 1 and Fig. 2.

It should also be noted that, for the sake of simplicity, the ΔV_T value corresponding to a particular time is assumed to correspond to the *average* values of ΔV_T when calculating the trap density. These relationships are presented in Fig. 1 and Fig. 2 and have the following form:

$$\Delta V_T(t) = 1.5\times10^{-3} t^{0.18} \quad (1)$$

$$\rho\left(\overline{\Delta V_T}\right) = 1\times10^{10} + 2.82\times10^{13}\,\overline{\Delta V_T} \quad (2)$$

Using this ageing model, the degradation time corresponding to 0 (“fresh devices”), 1e11, 5e11 and 1e12 cm^{-2} densities is approx. t=0, 60 s, 10 days and 12 months. RandomSpice is able to accurately generate ensembles of statistical compact models corresponding to an arbitrary degradation time using this model. In order to verify the accuracy of the generated models, TCAD simulation were performed again at an intermediate trap density of 7.5e11 cm^{-2} (3 months) for validation. Fig. 3 and Fig. 4 compare V_{TH} and correlations of figures of merit from TCAD simulation and from RandomSpice, showing excellent agreement between the generated models and the TCAD simulations, verifying the accuracy of the method. It is important to stress that the TCAD simulated data at t=3 months was not used as an input to RandomSpice’s generators.

IV. SRAM SIMULATION

SRAM is frequently used as a benchmark of a particular technology node. It is important for microprocessor cache as an integral component, and the corresponding SRAM cell usually consists of devices with minimum dimensions and the highest integrated density for a technology node. Therefore, it has very strict design constraints on chip area as well as power density. Additionally, it is most vulnerable to statistical variability compared to other circuits as it is often composed of minimum geometry devices, which rely on matched transistor performance, and a single cell failure can be catastrophic. In this study, SRAM was chosen as the test vehicle to demonstrate both the impact of ageing on cell performance, and the capability of the developed compact model generation methodology. With the developed approach, it is possible to investigate the impact of NBTI/PBTI induced ageing on 6-T SRAM performance. The SRAM cell under investigation is shown in Fig. 5. All devices have L=25nm, and width dimensions are shown in Table I.

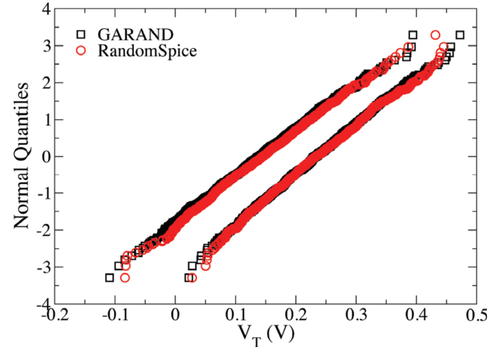

Fig. 3. QQ plot comparing V_T from TCAD simulations and RandomSpice generated models. Low and high drain bias, Q=7.5e11cm^{-2}/t=3 months.

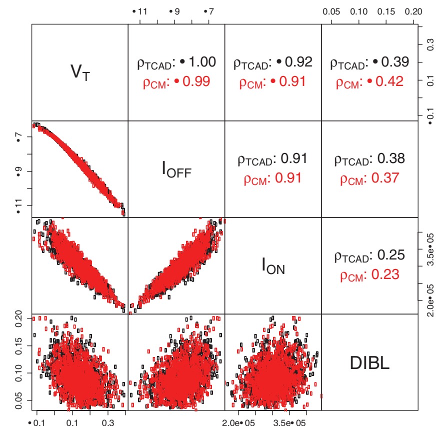

Fig. 4. Correlation matrix comparing device figures of merit from TCAD and RandomSpice generated models. High drain, Q=7.5e11cm^{-2}/t=3 months.

TABLE I. SRAM CELL DIMENSIONS

Device	Width (nm)
PU	50
PD	100
PASS	50

a.

A. Simulitions using Lookup Table models (LUT)

Simulations were carried out using Lookup Table models (where compact models are directly substituted in the circuit) for ages corresponding to the four levels of trap densities (fresh, 1e11, 5e11 and 1e12cm^{-2}) for which TCAD simulations

were also performed. For each density, 100,000 SRAM cells were simulated, and cell stability was evaluated in terms of static noise margin (SNM), which is illustrated Fig. 6. Note that only the “ON” transistors are degraded, representing the situation where the cell has been holding a particular state for a long period of time. The rest of the transistors in the cell are fresh.

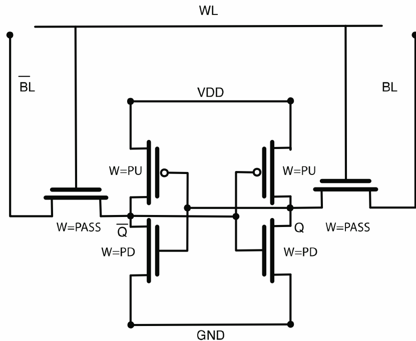

Fig. 5. SRAM cell under investigation.

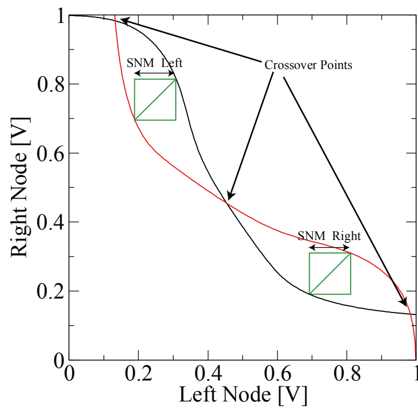

Fig. 6. Definition of SNM.

Fig. 7 shows the change in the first two moments (mean and standard deviation) of the distribution of SNM as a function of the cell age, illustrating the degradation in average stability as well as the increase in the spread of the distribution, as would be expected. Fig. 8 shows CDFs of SNM, plotted on a log scale, showing the increased occurrence of extreme cells with the transistor aging. Both of these figures show that the larger mismatch of the transistor age between the ‘ON’ transistors and the rest of the transistors in the cell, the more unstable the cell will be, resulting the more extreme occurrences.

B. Comparision between different Compact Modelling strategies

In evaluating SRAM performance, it is the rare events that are of most interest. Due to the limited number of “rare” devices in the LUT compact model ensemble, it becomes difficult to access these rare events in metric of interest. As a result, discretization and truncation starts to occur in the tails of the distribution of the performance metric and little useful information can be obtained about problematic rare cells.

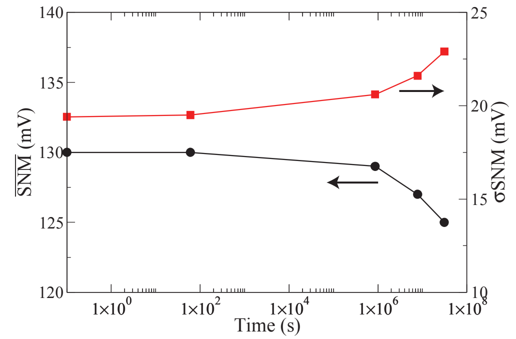

Fig. 7. : Dependence of the mean and standard deviation of SNM on time.

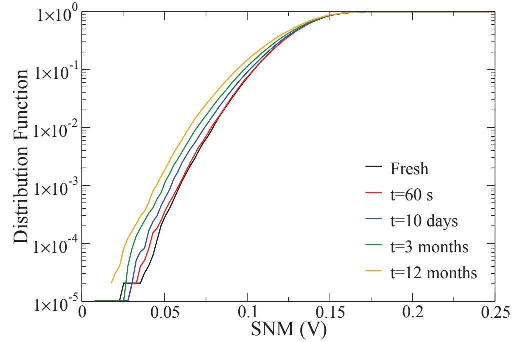

Fig. 8. CDF of SNM for SRAM of different ages.

In order to remedy these problems, we employ compact model generation using two approaches. Compact model generation is based on the premise that the statistics of the compact model parameters extracted from TCAD can be modeled and new random instances can be generated that follow the same statistics.

For the first generation approach, we use Gaussian V_T generators, where only a single BSIM parameter, *vth0*, is used. The mean and variance for *vth0* are obtained directly from the full models for the TCAD simulated trapped charge densities. Intermediate trapped charge densities are obtained by linear interpolation of the mean and variance for *vth0*. Obviously this approach does not fully capture the impact of ageing on device characteristics, however V_T does capture the first-order effects, and it is a commonly used approach and is presented here as a baseline for comparison.

In order to fully capture the non-Normal parameter distributions and inter-parameter correlations in the full models, we employ the more advanced model generation methods provided by RandomSpice. In this simulation study, both Gaussian V_T generators and RandomSpice’s advanced model generators were constructed based on the Lookup Table models used in the previous section and used to carry out SNM simulations at the same cell ages (thus corresponding to the appropriate trap densities obtained from TCAD simulation and used for LUT models). As previously, 100,000 cells were simulated at each time point using RandomSpice.

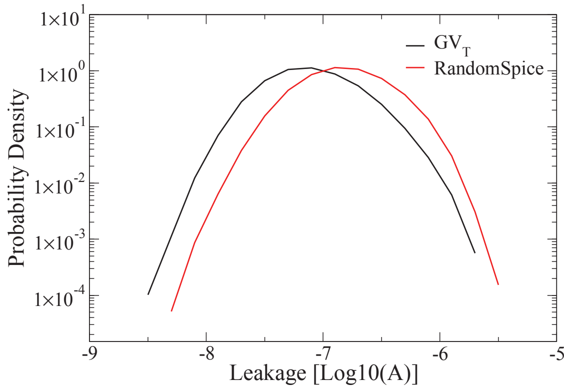

Fig. 9. Comparison of histograms (log) obtained from RandomSpice generated models and GV_T simulations for stand-by leakage. t=12 months.

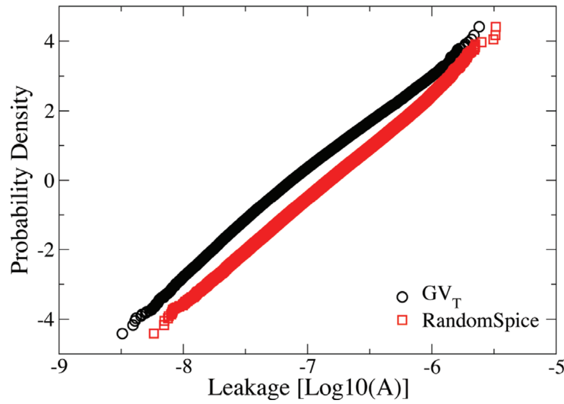

Fig. 10. Comparison of QQ plots obtained from RandomSpice and GV_T simulations for stand-by leakage. t=12 months.

Fig. 9 and Fig. 10 compare the results obtained for SRAM cell leakage simulation using both RandomSpice's advanced model generators and a traditional Gaussian V_T approach. It is clear from these results that Gaussian V_T simulation methods are insufficient to capture the complex effects of ageing.

V. Conclusions

In this study, an accurate method of incorporating transistor ageing into SPICE-level circuit simulations has been demonstrated. It was shown that simulations can be performed with RandomSpice at arbitrary stress times and accurately capture variations in transistor performance at different stages of ageing.

Acknowledgment

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