Recent Enhancements in BSIM6 Bulk MOSFET Model

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***Abstract*— In this paper, we discuss the recent enhancements made in the BSIM6 bulk MOSFET model. BSIM6 is the latest compact model of bulk MOSFET from BSIM group which have body referenced charge based core. Junction capacitance model is improved over BSIM4 and is infinitely continuous around V_{bs}=V_{bd}=0V. Symmetry of the model is successfully validated by performing Gummel Symmetry Test (GST) in DC and symmetry test for capacitances in AC. Self heating model is also included in BSIM6 and test results are reported. Model capabilities are compared against an advanced 40nm CMOS technology and it is observed that simulated results are in excellent agreement with the measured data.**

I. Introduction

BSIM group has long history of producing industry oriented compact models for circuit simulations. Starting with BSIM1 and BSIM2, BSIM3 gained huge popularity due to the accuracy and simplicity which made it an obvious choice for the industry after the Compact Model Coalition (former Compact Model Council [1]) standardization [2]. With rapidly changing technology, new BSIM4 model surfaced for advanced nodes in 2000 and is still used by many industries even for technology nodes as high as 28nm [1]. Beauty of the BSIM4 lies in the flexibility it offers to the device engineers to match measured data. Although it is able to accurately capture real device effects, it is not symmetric around $V_{ds} = 0$, which is a bottleneck for RF design. BSIM6 is the latest industry standard compact model for bulk MOSFET which is mainly developed to make model more physical and suitable for high speed analog applications and for this it builds upon a physical charged based core derived from Poisson solution for long channel MOSFET. The real device effects like gate current, series resistance, current saturation, DIBL etc. are modeled similar to BSIM4 with same parameter names, thus allowing smooth transition from BSIM4 to BSIM6 [3]. Although most of the popular real device models are inherited from BSIM4, however it has been ensured that BSIM6 remains symmetric around $V_{ds} = 0$, thus paving the way for RF implementation. The paper is organized as follows. Basic BSIM6 core is discussed in Section II. Junction capacitance model is described in Section III and symmetry properties of BSIM6 are tested in Section IV. Section V describes self heating model of BSIM6. Model validation with physical data is carried out in Section VI and conclusion is drawn in section VII.

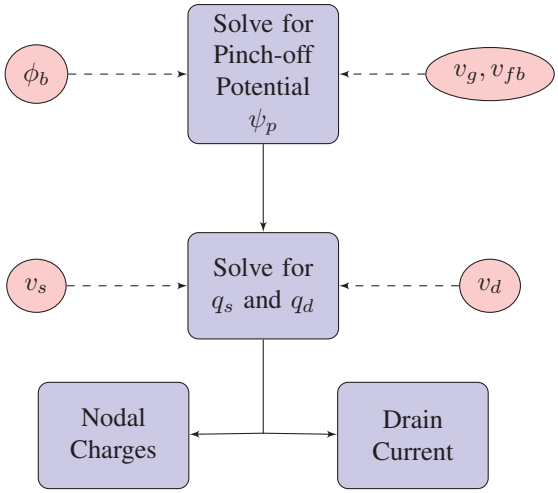

Fig. 1. BSIM6:Solution of the Core Model

II. BSIM6 Model

BSIM4 has delivered excellent user experience in terms of speed, accuracy and flexibility. Certain class of circuits using MOSFET as a bidirectional switch, like pass gate, demands symmetry around $V_{ds} = 0$ and because of asymmetry, BSIM4 cannot be used. Therefore BSIM group started working on BSIM6 in 2010, with an aim to make it more physical for RF applications. Fig. 1 summarizes the sequence of steps followed for obtaining drain current and terminal charges in BSIM6 (without real device effects). The core of the BSIM6 first solves for the pinch-off potential from the knowledge of gate terminal voltage and device parameters. Equation (1) describes pinch off potential expression for all biases. The detailed derivation of the equation can be found in [4]. Here ψ_{p0} is the approximation of pinch-off potential when it is close to zero, γ is the body factor and ψ_p, v_g, v_{fb} and ϕ_b are the pinch off potential, gate voltage, flat band voltage and bulk potential respectively, normalized to nV_t where V_t is the thermal voltage.

This knowledge of ψ_p is used to obtain inversion charge density (q_i) by solving (2). The earlier attempt to solve this equation requires approximations which leads to error com-

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$$\psi_p = \begin{cases} 1 + \left[\sqrt{v_g - v_{fb} - 1 + \left(\frac{\gamma}{2}\right)^2} - \frac{\gamma}{2}\right]^2 & \text{if } v_g - v_{fb} > \phi_b + \gamma\sqrt{\phi_b} \\ 1 - e^{-\psi_{p0}} + \left[\sqrt{v_g - v_{fb} - 1 + e^{-\psi_{p0}} + \left(\frac{\gamma}{2}\right)^2} - \frac{\gamma}{2}\right]^2 & \text{if } \phi_b + \gamma\sqrt{\phi_b} \geq v_g - v_{fb} \geq 0 \\ -\ln\left[1 - \psi_{p0} + \left(\frac{v_g - v_{fb} - \psi_{p0}}{\gamma}\right)^2\right] & \text{if } v_g - v_{fb} < 0 \end{cases} \quad (1)$$

pared to numerical solutions. In BSIM6, no approximations are made [5] and it is solved in such that accuracy as well as computational efficiency, both are maintained.

$$\ln(q_i) + \ln\left[\frac{2n_q}{\gamma}(q_i\frac{2n_q}{\gamma} + 2\sqrt{\psi_p - 2q_i})\right] + 2q_i = \psi_p - 2\phi_f - v_{ch} \quad (2)$$

Inversion charge densities at source (q_s) and drain (q_d) ends are obtained by using $v_{ch} = v_s$ and $v_{ch} = v_d$ in (2) respectively. The drain to source current is then obtained by drift diffusion model [4]

$$I_{DS} = 2 \cdot n_q \cdot \mu_{eff} \cdot \frac{W_{eff}}{L_{eff}} \cdot C_{ox} \cdot nV_t^2 \frac{\Delta q(1 + q_s + q_d)}{D_{vsat}} \quad (3)$$

Here n_q is the slope factor and the term D_{vsat} accounts for the effect of current saturation on device characteristics.

III. Improved Junction Capacitance Model

The diode junction capacitance model of BSIM4 shows asymmetry in second derivative (around V_{bs} = 0) and therefore had issues with the ac symmetry test. In BSIM6, the model is updated so that it is infinitely differentiable and symmetric around V_{ds} = 0. The drain-to-body (D/B) junction capacitance is modeled as [4], [6],

$$C_{bd} = A_{drain}.C_{jbd} + P_{drain}.C_{jbdsw} + W_{cj} \cdot NF \cdot C_{jbdswg}$$

The C_{jbd} is modeled as

$$C_{jbd} = \begin{cases} CJD(1 - \frac{V_{bd}}{PBD})^{-MJD} & \text{if } \frac{V_{bd}}{PBD} \leq x_0 \\ \frac{CJD}{(1-x_0)^{MJD}}\left(1 + MJD\left(1 + \frac{\frac{V_{bd}}{PBD} - 1}{1 - x_0}\right)\right) & \text{if } \frac{V_{bd}}{PBD} > x_0 \end{cases} \quad (4)$$

where C_{jbd} is the unit area bottom D/B junction capacitance, C_{jbdsw} and C_{jbdswg} are the unit length D/B junction sidewall capacitance along the isolation edge and gate edge respectively. The parameter CJD corresponds to unit-area bottom junction capacitance at zero bias, PBD is the corresponding built-in potential, MJD is the grading coefficient and x_0 is 0.9. BSIM4 junction capacitance model is the special case of this BSIM6 model, with the later reducing to former for $x_0 = 0$. The sidewall junction capacitance along isolation edge, C_{jbdsw} and along the gate edge, C_{jbdswg}, are also calculated using similar expressions.

Fig. 2 shows the junction capacitance derivative comparison between BSIM4 and BSIM6. The third derivative of charge (second derivative of capacitance) will produce a kink around $V_j = 0$ for BSIM4. However in BSIM6, this point has been shifted away from $V_j = 0$ (to large V_j) so that the derivatives remains continuous for all practical applications.

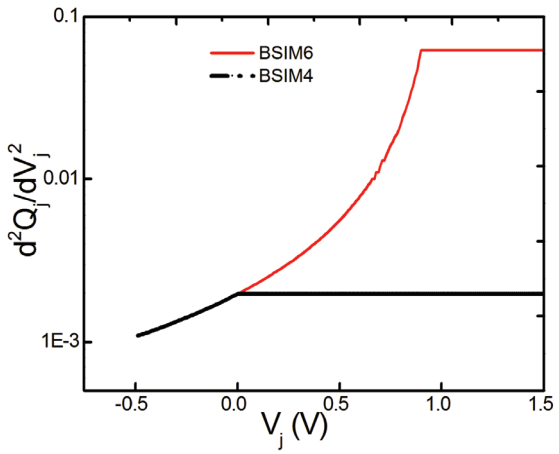

Fig. 2. Junction capacitance model : BSIM4 vs BSIM6. Symmetry issues around Vds=0 can be seen in BSIM4. This is removed in BSIM6, which is now infinitely differentiable at that point.

IV. Symmetry Test

Bulk MOSFET behaves identical if the source and drain terminals are interchanged i.e. source and drain terminals are indistinguishable and it is the external voltage which determines the terminal names. Compact model sometimes becomes too complicated that they does not reflect this symmetry property, severely limiting the physicality of the model. In order to validate symmetry of the BSIM6, DC Gummel symmetry test [7] is performed and symmetry of the charge model is verified by AC symmetry test. Fig. 3 shows the normalized (to their maximum value) fourth derivative plot for strong and weak inversion regions. The derivatives can be observed to be continuous and symmetric around V_{ds} = 0. In fact any order of derivative can be made continuous by proper choice of parameter DELTA, which monitors the transition of V_{ds} to V_{dsat}. Fig. 4 shows the ac symmetry test for gate capacitance, where it can be seen that capacitance δC_g is an odd function of voltage V_X and derivative is continuous around V_{ds} = 0.

V. Self Heating Effect (SHE)

As the device dissipates power, its operating temperature changes (due to fluctuation in instantaneous temperature) and

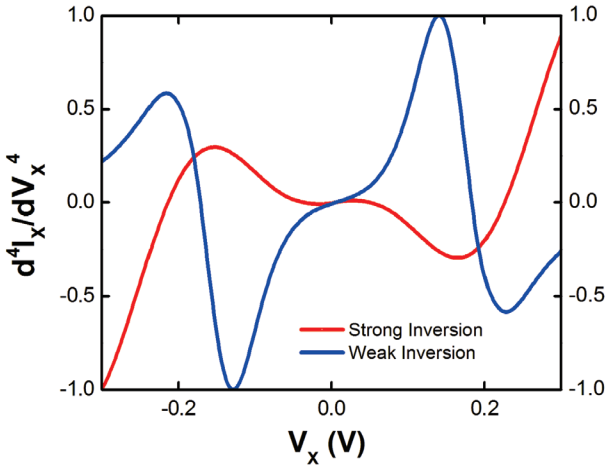

Fig. 3. Gummel symmetry test: the I_{DS} current vs. $V_X = \frac{V_D - V_S}{2}$ when V_D= -V_S.

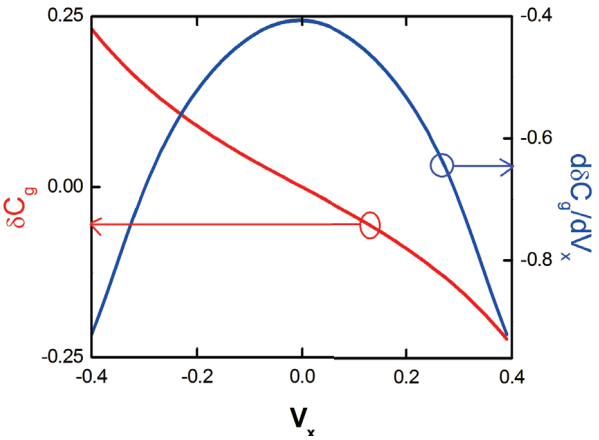

Fig. 4. AC symmetry plot for gate capacitance. Model shows excellent symmetry properties for several order of derivatives.

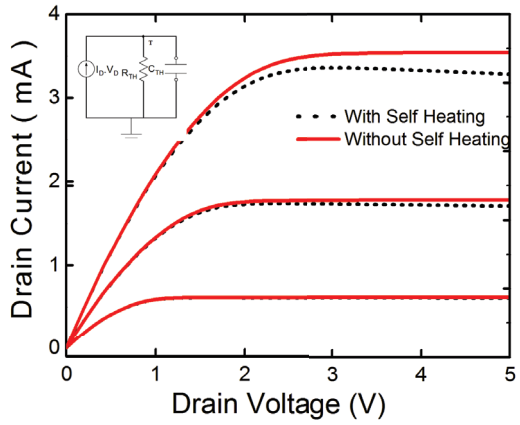

Fig. 5. Effect of self heating on drain current. Inset figure is the thermal network. Self heating effect is observed mainly at high power, causing the drain current to decrease with drain voltage.

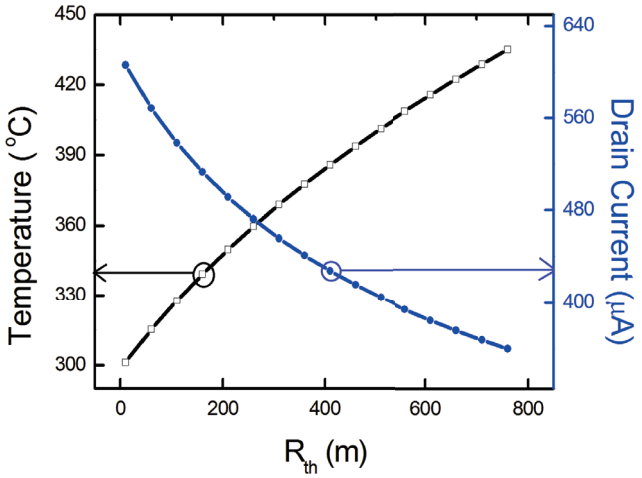

Fig. 6. Variation of temperature and current with thermal resistance, when self heating model is on.

affects different aspects of the device like mobility, threshold voltage, etc., which finally propagates to the terminal currents. For the devices with very high power dissipation, SHE can have significant effect on overall performance. BSIM6 models SHE by employing a thermal network, consisting of thermal resistance R_{th} and capacitance C_{th}, and driving it by current equal in magnitude of the total power dissipation of the device [8], as shown in the inset of Fig. 5. The voltage at thermal node T gives the rise in temperature, which is then added with the effective temperature of the device. Fig. 5 also shows the effect of self heating on ID-VD characteristics where the decreased in ID is observed as VD is increased.

For testing the self heating model [9], NMOS is biased in strong inversion region and thermal resistance R_{th} is sweeped and device temperature and the drain current are observed. Fig. 6 shows the effect of R_{th} on temperature and current. It is evident that temperature increases as the thermal resistance is increased and correspondingly drain current reduces. It is to be noted that the temperature in this figure is the total temperature of the device including the effect of self heating. Now the self heating mode is switched off and device is simulated for temperature range obtained from self heating effect. For the good SHE model, current from both the approaches should match. Fig. 7 shows the drain current obtained from these two approaches and it can be seen that both the curves overlaps with excellent accuracy confirming the correctness of the model.

VI. Model Validation with Measured Data

BSIM6 capabilities of data matching is tested for state-of-the-art 40nm CMOS technology [10]. Fig. 8 shows the normalized drain current with respect to the gate overdrive voltage for four combinations of device dimensions, covering

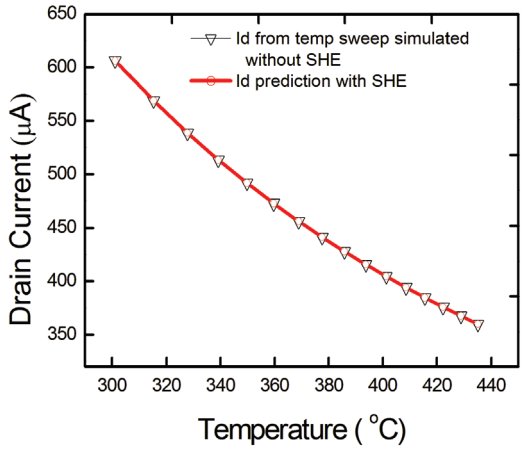

Fig. 7. Self heating model check : Comparison of drain current from two approaches.

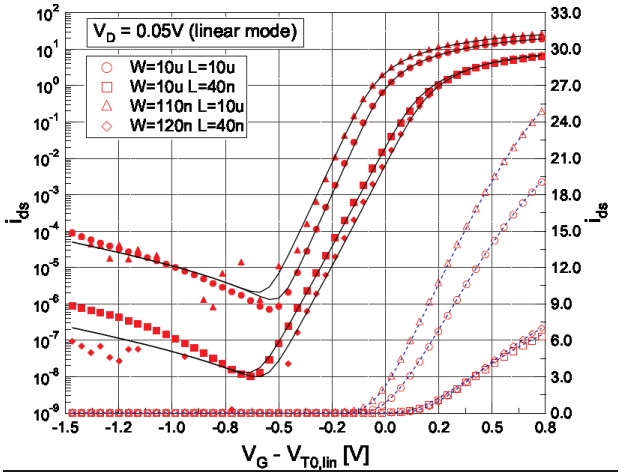

Fig. 8. Normalized drain current vs. the gate overdrive voltage for the corner devices of a 40 nm CMOS technology.

both long and short channel devices. BSIM6 is able to match the characteristics accurately both in strong and weak inversion regions as indicated by the log axis plot of the Fig. 8 . In Fig. 9, normalized drain current is plotted for different channel lengths for different gate overdrive voltages ranging from weak to strong inversion, when the device is biased in linear region. It can be observed that the simulation results are in excellent agreement with the measured data.

VII. Conclusion

Scaling has always been the driving force behind the semiconductor industries. However, every time device is scaled, it brings unpredicted challenges to the model developer. Industry standard requires model to be physical and computationally efficient at the same time, and thus requires thorough understanding of device physics. In continuation of series of its compact models, BSIM group developed BSIM6 for the bulk MOSFET. BSIM6 is symmetric around $V_{ds} = 0$, models all

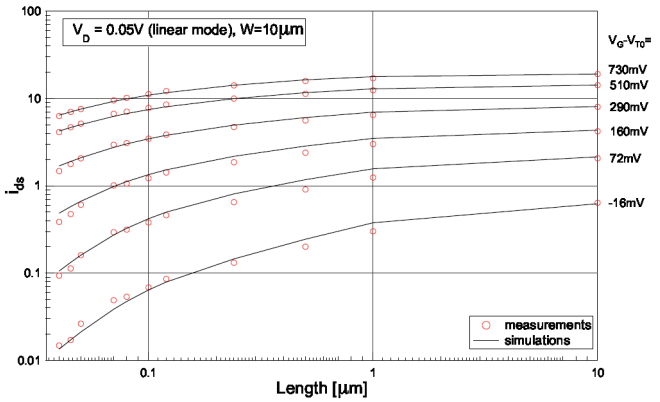

Fig. 9. The normalized drain current as a function of channel length. Model captures the scaling behavior with excellent accuracy.

the real device effects, passes benchmark test and implemented in Verilog-A in an efficient manner. Special attempts has been made to maintain symmetry and physical nature of the model and for this junction capacitance model and effective V_{ds} models of BSIM4 are adopted in modified form, thus allowing BSIM6 to pass AC and DC symmetry test successfully. Model also shows excellent matching with the physical data both in weak and strong inversion.

VIII. Acknowledgment

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References

[1] "Si2 webpage." [Online]. Available: http://www.si2.org/
[2] Y. S. Chauhan, S. Venugopalan, M. A. U. Karim, S. Khandelwal, N. Paydavosi, P. Thakur, A. Niknejad, and C. Hu, "BSIM - Industry Standard Compact MOSFET Models," in *European Solid-State Device Research Conference (ESSDERC)*, 2012.
[3] S. Venugopalan, K. Dandu, S. Martin, R. Taylor, C. Cirba, X. Zhang, A. Niknejad, and C. Hu, "A non-iterative physical procedure for RF CMOS compact model extraction using BSIM6," *IEEE Custom Integrated Circuits Conference (CICC)*, pp. 1–4, 2012.
[4] "BSIM6 Technical Manual." [Online]. Available: http://www-device.eecs.berkeley.edu/bsim/?page=BSIM6
[5] Y. S. Chauhan, M. A. Karim, S. Venugopalan, S. Khandelwal, P. Thakur, N. Paydavosi, A. B. Sachid, A. Niknejad, and C. Hu, "BSIM6: Symmetric Bulk MOSFET Model," in *Workshop on Compact Modeling, Santa Clara, USA*, 2012.
[6] "MOS Model 11 manual." [Online]. Available: http://www.nxp.com/models/simkit/mos-models/model-11.html
[7] C. McAndrew, "Validation of MOSFET model Source-Drain Symmetry," *IEEE Transactions on Electron Devices*, vol. 53, no. 9, pp. 2202–2206, 2006.
[8] "BSIMSOI Technical Manual." [Online]. Available: http://www-device.eecs.berkeley.edu/bsim/?page=BSIMSOI
[9] G. Gildenblat, *Compact Modeling: Principles, Techniques and Applications*. Springer, 2010.
[10] M.-A. Chalkiadaki, A. Mangla, C. C. Enz, Y. S. Chauhan, M. A. Karim, S. Venugopalan, A. Niknejad, and C. Hu, "Evaluation of the BSIM6 Compact MOSFET Model's Scalability in 40nm CMOS Technology," in *Conference on European Solid-State Device Research (ESSDERC)*, Bordeaux, 2012.