A Process/Device/Circuit/System Compatible Simulation Framework for Poly-Si TFT Based SRAM Design

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***Abstract*—Operation characteristics of low temperature poly silicon thin-film transistor (LTPS-TFT) based systems vary significantly with design choices and parameters (i.e., process, device, circuit and system). Due to the lack of cross-layer simulation tool, conventional designs only optimize the design layers in isolation, leading to sub-optimal solutions. We present a cross-layer simulation framework for the design of LTPS-TFT Static Random Access Memory (SRAM). The proposed simulation framework optimizes design parameters considering the entire design space and hence, greatly reduces design complexity and efforts. The benefits of our proposed framework are illustrated by case studies.**

Keywords—LTPS, poly-Si, TFT, SRAM, yield estimation, design optimization

I. Introduction

Low-temperature poly-silicon (LTPS) thin-film transistor (TFT) has received growing attention in the recent past. Due to its low fabrication cost and unique feature of flexible substrate, various emerging applications (e.g., system-on-glass display, flexible memory, and microprocessor [1-6][10]) have been reported. Among the many applications, static random access memory (SRAM) has been considered by several researchers [4-6] since it occupies most area in the chip, and the corresponding design optimization is relatively challenging.

Despite the increasing interests, current research focus has mainly been at a particular level of design abstraction (e.g., device), while treating other levels (e.g., circuit) as black boxes [7-8]. As the behavior of LTPS-TFT systems varies significantly with the design choices and options, optimizing design layers in isolation often leads to sub-optimal solutions. Efficient cross-layer simulation is highly desirable. Nonetheless, due to the high complexity and difficulty, up to date no process/device/circuit/system compatible simulation methodology is available in literature. In this work, we propose a cross-layer design and simulation framework for LTPS-TFT SRAM which captures the impacts of various design factors at different design layers. This framework substantially reduces the design complexity and enables rapid design space exploration with yield estimation at the early stages.

II. Cross-Layer Simulation Framework

A. Overview

Fig. 1 shows the proposed cross-layer simulation framework. The user inputs to this framework comprise of: process and device parameters, circuit-level design choices, and system-level specification. The process and device parameters include the average Si-grain size, trap density of grain boundary (GB), and the transistor length/width, etc. The circuit-level parameters cover the design choices of TFT SRAM such as cell structures (6T, 8T, or 10T), supply voltage, operation frequency, etc. The system specification is often defined based on the requirement to the product. In our experiment, we apply Static Noise Margin (SNM) and Read SNM (RSNM) as the criteria for reliability, and read/write time as the criteria for performance.

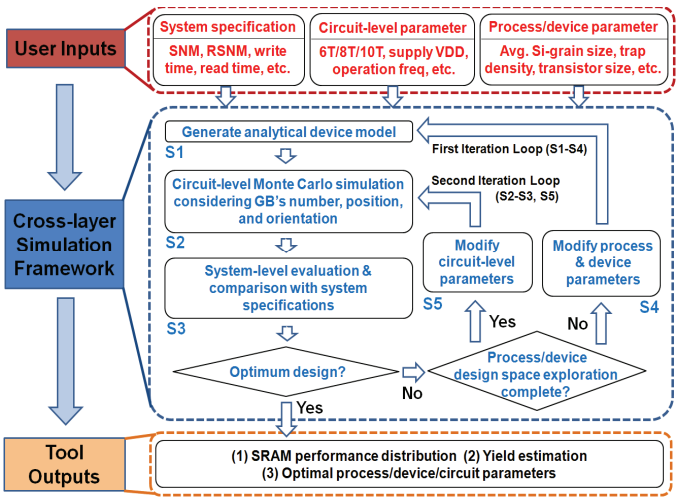

Fig. 1. Flowchart showing the proposed cross-layer simulation framework

In the framework, five simulation steps (S1-S5) form two iterative simulation loops. S1-S3 runs device, circuit, and system level simulation and evaluation, respectively. S4 and S5 adjust the design parameters at the device and the circuit level of design abstraction, respectively. The first iteration loop (S1-S4) explores the process and device level design space, including average Si-grain size, trap density, gate oxide thickness, doping profile, and transistor size. The second iteration loop (S2-S3, S5) sweeps the circuit-level design parameters, such as supply voltage and SRAM circuit configurations (6T, 8T or 10T). Note that, the design parameters modification at process/device level (i.e., S4) needs to be followed by device level simulation (i.e., S1) since the statistical database of the TFTs as well as the device model requires to be re-evaluated. On the other hand, the circuit-level parameter optimization (i.e., S5) needs no updating on device characteristics. S5 could be directly followed by S2, and the skipping of S1 would reduce the redundant operations of the framework.

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Finally, the optimal design solution that meets the constraints of all design layers while being the best fit for the system-level specification is determined. In this design framework, a validated analytical device model of LTPS-TFT [11] is used in S1. 1000 Monte Carlo circuit simulations are carried out in S2 to characterize the impact of random number, position and orientation of GBs. Statistical performance of SRAM are extracted in S3 from Monte Carlo simulations results and compared with the input of system-level specification.

B. *Statistical Poly-Si TFT characteristics*

To justify the necessity of applying the analytical device model to cross-layer simulation, statistical characteristics of the LTPS TFT devices obtained from the analytical device model [11] are shown in Fig 2 and 3. Fig. 2(a) shows how the threshold voltage (V_{th}) of unit-size LTPS-TFT varies with average Si-grain size. When the Si-grain size increases from 300nm to 1000nm, the V_{th} mean and maximum values decrease from 0.25 volt to 0.1 volt and from 0.55 volt to 0.4 volt. The variation can reach to 150% and 37%, respectively. Fig. 2(b) shows the detailed probability distribution of the transistor threshold voltage, V_{th}, for three exemplary Si-grain sizes – 300nm, 600nm, and 1000nm. It is observed that the V_{th} distribution for smaller Si-grains looks like Gaussian distribution. However, the V_{th} distribution is apparently non-Gaussian for larger Si-grains.

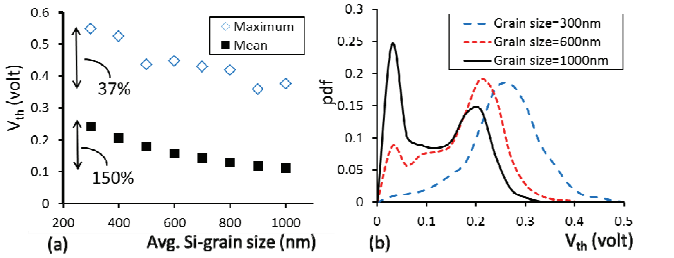

Fig. 2. V_{th} distribution of unit-size (1μm/1μm) TFTs: (a) Mean and max V_{th} of TFTs with different Si-grain size, and (b) V_{th} distribution of Si-grain size at 300nm, 600nm, and 1000nm.

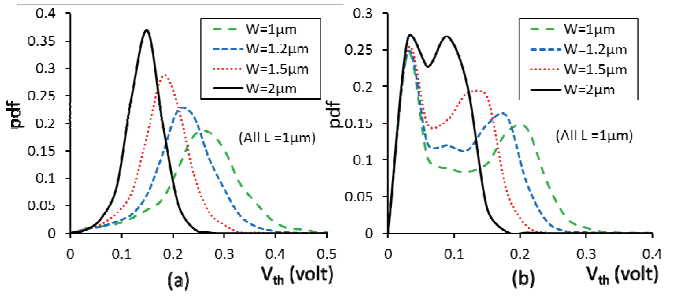

Fig. 3. V_{th} distribution for different-size (W=1μm, 1.2μm, 1.5μm, and 2μm) of TFTs: (a) Si-grain size at 300nm, and (b) Si-grain size at 1000nm.

In addition to silicon grain size, transistor size also affects the V_{th} distribution (Fig. 3). As shown in Fig. 3(a), as the Si-grain size is fixed at 300nm, all the V_{th} distributions seem Gaussian, while the mean value and standard deviation decrease with the increase of device width. Fig. 3(b) show the case with Si-grain size fixed at 1000nm. When the transistor size is comparable with Si-grain size, V_{th} distribution remarkably changes. From the simulation results, we can observe that the statistical characteristics of LTPS-TFT are complicated and affected by the design parameters at the process and the device levels.

C. *Simulated TFT SRAM characteristics of reliability and performance*

Based on the device-level statistical analysis, the framework further simulates the TFT SRAM circuitry and extracts the system-level characteristics. Fig. 4 illustrates how the reliability and performance of unit-size SRAM (i.e. α=1, β=1, refer to Eqn. 1 & 2) can be affected by the process and device level design parameters. Fig. 4(a) and (b) firstly show the static noise margin and read static noise margin (SNM and RSNM) of the SRAM with different Si-grain size. We can observe the mean values of SNM and RSNM both decrease with the increasing of Si-grain size. Even standard deviation of the critical RSNM increases at the same time. As a result, larger Si-grain size on the TFT SRAM indicates poorer reliability for the data retention.

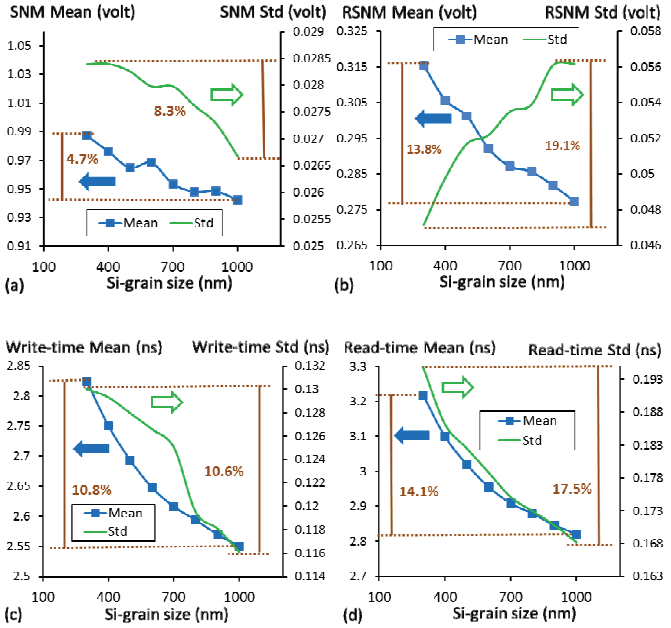

Fig. 4. Mean and standard deviation of the characteristics of a unit-size TFT SRAM (all the TFTs are with width=length=1μm) when different Si-grain sizes are applied: (a) SNM, (b) Read-SNM, (c) Write time, and (b) Read time.

$$\alpha = \frac{\mathrm{pTFT}_{\mathrm{pull-up}}}{\mathrm{nTFT}_{\mathrm{pass-gate}}} \qquad \text{Eqn. 1}$$

$$\beta = \frac{\mathrm{nTFT}_{\mathrm{pull-down}}}{\mathrm{nTFT}_{\mathrm{pass-gate}}} \qquad \text{Eqn. 2}$$

As to the performance, Fig. 4(c) and (d) show that both the write time and read time of the SRAM improve when the Si-grain size increases. This indicates that, when a larger Si-grain is selected in the process, the SRAM can operate with higher operation frequency.

The above figures, providing the information of stability and performance, can also assist the yield estimation of the

SRAM when considering the system specifications. Fig. 5 plots the individual and comprehensive SRAM yield as the function of Si-grain size. The individual yield comprises of SNM, RSNM, write operation, and read operation. The specifications applied are SNM ≧ 0.9volt, RSNM ≧ 0.2volt, and clock period=5ns. The comprehensive yield shows the percentage of TFT SRAM cells passing the four specifications. As show in Fig. 5, small Si-grain leads to low yield due to longer write/read times. On the other hand, increasing Si-grain size to some extent also reduces the yield because of lower noise margins. Note, a 600nm Si-grain corresponds to the maximum yield as high as 95%. Also note that the optimal Si-grain size varies under different design scenarios as illustrated later in the case studies.

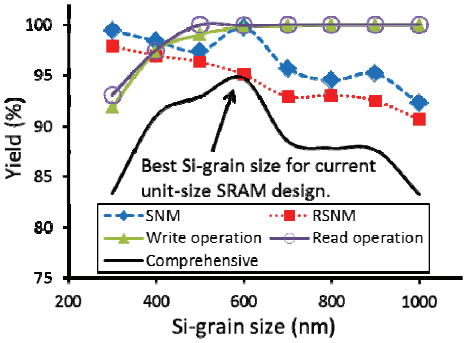

Fig. 5. Individual yields and comprehensive yield for an SRAM design.

III. Case Study

In this section, two case studies are provided to demonstrate the benefits and capability of our proposed cross-layer simulation framework. The first study explores how yield varies with Si-grain size, transistor size, and the corresponding area of SRAM cell. The second case study is used to demonstrate how the proposed simulation framework can lead to low-power high-yield SRAM design. All the yield values in the discussion refer to the comprehensive yield defined in Fig. 5.

A. Case study 1: Yield estimation with cross-layer design parameters/choices

In this case study, we include all the cross-layer design parameters to the framework to estimate the yield of the TFT SRAM. Then, by showing the varying trend with the design options and searching for the peak value, we acquire the achievable optimal yield of the product with the corresponding design parameters.

Fig. 6 shows the three design scenarios where different transistor sizing and cell area are used. It is obviously observed that the highest yield under each scenario corresponds to different Si-grain size. For TFT SRAM with transistor ratio α=1 and β=1, the optimal Si-grain size locates at around 600nm. However, for SRAMs with α=1 and β=0.83, the optimal Si-grain size is 300nm. As to the SRAM with α=1.2 and β=1, although the optimal Si-grain size is also 600nm, the Si-grain size larger than 700nm could still provide the yield higher than 93% consistently.

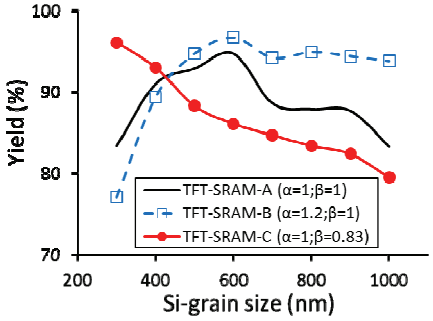

Fig. 6. Case study 1: Yield of different SRAM designs versus chosen Si-grain size for process.

In addition to Si-grain size, the SRAM cell area corresponding to transistor sizing also affect the yield of produce. Fig. 7 shows the SRAM yield versus the occupied area of the cell when the Si-grain size is fixed at 300nm (Fig. 7(a)) and 1000nm (Fig. 7(b)). Each node in the figure indicates different design scenarios for the SRAM. When comparing the two figures, it is implied that the optimal yield may varies from 83% to 96% when the SRAM cell area varies.

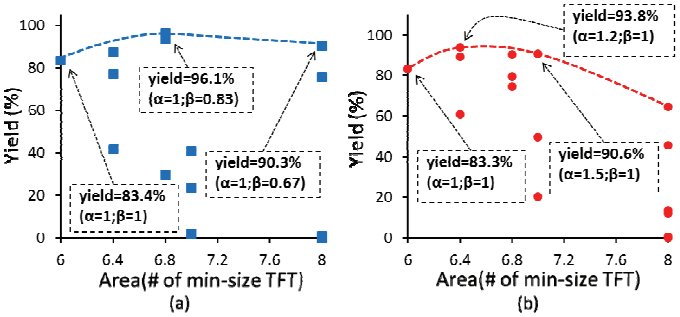

Fig. 7. Case study 1 (cont'd): Optimal SRAM designs under different Si-grain size (each point indicates a certain design scenario): (a) 300 nm, (b) 1000nm.

Fig. 8 shows how yield is jointly affected by Si-grain size, transistor sizing and area. With this 3D representation, designers can determine the best device and circuit level parameters for the highest yield.

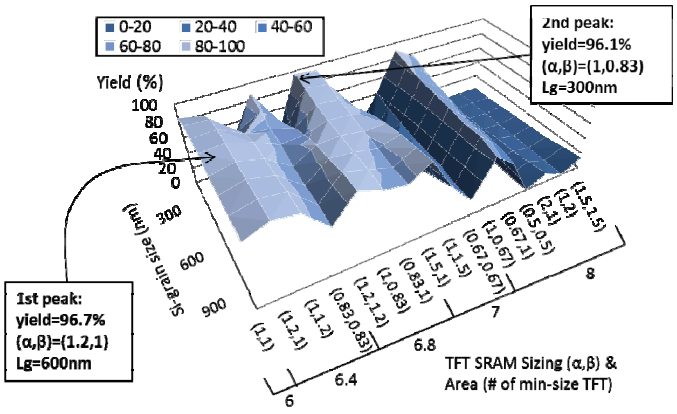

Fig. 8. Case study 1 (cont'd): Globally optimized SRAM designs including transistor sizing and Si-grain size of process.

B. *Case study 2: Low-power high-yield SRAM design with the proposed framework*

Based on the capability of searching high yield for the TFT SRAM, the proposed framework could also extent the function such as low-power design by defining the specific system requirement. For low-power design, we apply the most straightforward but efficient method: lowering supply voltage. Firstly, we assume that the required system specification for yield is no less than 95%. Fig. 9(a) and (b) shows simulation results with respect to 3V and 2.7V supply, respectively. If the design choices and parameters are located in the high-yield region (>95%), the design solutions in Fig. 9(b) consume less power than those in Fig. 9(a). Thus, through the proposed framework, we can obtain a much lower power design while maintaining the same required yield.

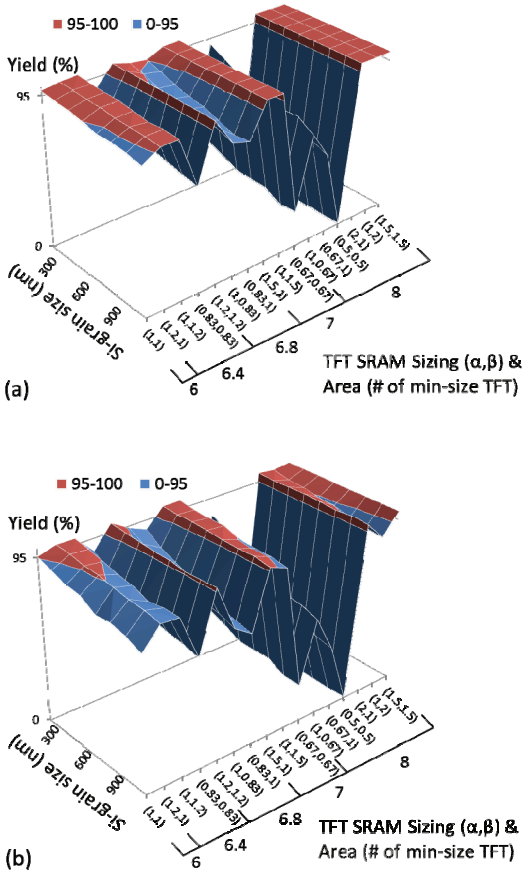

Fig. 9. Case study 2: For low-power operation, the step to filter off the designs with insufficient yield under different supply voltage (a) 3 volt, (b) 2.7 volt.

Furthermore, Fig. 10 reveals the results of energy consumption per SRAM operation for each possible design solution in the high-yield region of Fig. 9. The most energy efficient SRAM design can be easily determined from Fig. 10. The corresponding optimal design parameters and choices at different design layers can also be determined with the proposed simulation framework. These case studies validate the importance and necessity of performing cross-layer simulation and design for LTPS-TFT SRAMs.

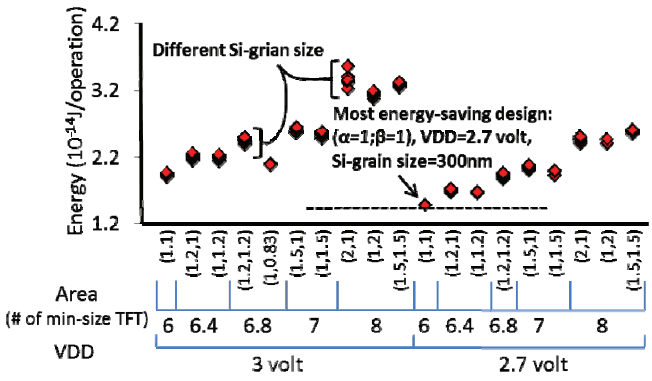

Fig. 10. Case study 2 (cont'd): Find the most energy saving designs (with corresponding process parameter and VDD) among the robust designs in Fig. 9.

IV. CONCLUSION

A cross-layer design and simulation framework is developed and presented for LTPS-TFT based SRAM. This framework takes into account the impact of various design parameters from different layers of design abstraction and enables cross-layer optimization. Two case studies were presented to show cross-layer design space exploration to optimize system yield and energy consumption.

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