

Identification and quantification of 4H-SiC (0001)/SiO₂ interface defects by combining density functional and device simulations

D.P. Ettisserry*, S. Salemi, N. Goldsman, S. Potbhare,
A. Akturk
Department of Electrical and Computer Engineering
University of Maryland
College Park, MD, USA
*deva@umd.edu

A. Lelis
U.S. Army Research Laboratory
2800 Powder Mill Road
Adelphi, MD, USA

Abstract— In this work, we use Density Functional Theory (DFT)-based electronic structure calculations, together with 2D-Device simulations and experiments, to identify and quantify mobility-limiting defects at the 4H-Silicon Carbide (0001) / Silicon Dioxide interface of a Silicon Carbide (SiC) DMOSFET channel. DFT simulations are performed on a variety of possible interfacial defects including the single Carbon interstitial and the Carbon dimer interstitial to calculate their projected Density of States (pDOS) and energy levels. A unique methodology is presented to determine the defect energy levels and corresponding defect concentrations along the channel using DFT calculations, 2D-Device simulations and device I-V measurements. By comparing the results obtained from DFT and 2D-Device simulations, we identified single Carbon interstitials to be the main contributor to mobility-limiting near-interface traps. The defect concentration was also calculated for various locations in the channel.

Keywords—density functional theory, device simulation, near interface trap, silicon carbide

I. INTRODUCTION

Silicon Carbide is already beginning to be used as a material for high-power and high-temperature Metal-Oxide-Semiconductor (MOS) electronics owing to its wide band gap, high thermal conductivity and the ability to grow a native oxide. However, the efficiency of these devices is believed to be severely limited due to channel mobility degradation caused by defect-induced electronic trap states close to the conduction band [1]. Additionally, the trapped charges are known to further reduce the mobility by Coulomb scattering the available free carriers in the inversion layer [2]. While experiments and first-principle simulations were attempted in the past to identify these defects, no agreement on the nature of these defects has been reached so far [3-8]. To our knowledge, this is the first work which self-consistently extracts the concentration and the type of any particular defect for a SiC DMOSFET.

The root of high density of interface states (D_{it}) is believed to be in the oxidation process of SiC, typically occurring at about 1100°C [9]. Some researchers, using Density Functional Theory (DFT) calculations, suggest the presence of Carbon dimer interstitial defect in the SiC substrate to be the main reason for high D_{it} [4, 5]. Attempts have also been made to quantify this defect using C-V measurements and electrostatic modeling on a lateral MOSFET [10]. On the other hand, some other theoretical studies point to C dimer interstitials in the

oxide to degrade channel mobility [3]. Recently, Spin Dependent Recombination (SDR) based experiments have suggested Si vacancy to be a prominent type of mobility-limiting defect [6]. An amorphous transition region between SiC and SiO₂, detected using TEM measurements, is also believed to be a possible reason for exceptionally low channel mobility observed in SiC/SiO₂ interfaces [7].

In this work, we determine the projected Density of States (pDOS) and the electronic levels of some of the likely near-interface defects in SiC/SiO₂ interface using Density Functional calculations. We also simulate a SiC vertical Double-diffused MOSFET (DMOSFET) using our in-house 2D-device simulator [2, 11, 12]. We then present a novel generic methodology to identify and quantify the mobility-limiting defects along the DMOSFET channel by combining Density functional and 2D-device simulations.

II. METHODOLOGY

A. Density Functional Calculations

Density functional theory puts forward a methodology to solve the multi-body Schrodinger equation in a modified form and extract the ground state properties of the system. Here, we model the SiC/SiO₂ interface system in a slab form and simulate its electronic structure using Plane-wave DFT, as implemented in the software, Quantum Espresso [13].

An abrupt SiC/SiO₂ slab with 108 atoms was constructed for simulation. A sufficiently thick layer of vacuum isolated the slab. The surface atoms were all passivated by Hydrogen atoms to eliminate the effects of dangling bonds. Moreover, no dangling Si bond was allowed at the interface, making it abrupt, as shown in Figure 1(a). In performing the calculations, the plane-wave cutoff energy was fixed at 950 eV. The exchange and correlation energy was approximated using the PBE (Perdew-Burke-Ernzerhof) scheme of Generalized Gradient Approximation (GGA). The effect of core electrons was modeled using a norm-conserving pseudopotential. The Brillouin zone sampling was done at the Gamma point. Geometric relaxation of the structure was also performed before doing the simulations.

It is well known that the PBE functional used above underestimates the bandgap. Thus a hybrid functional scheme was employed to retrieve the experimental band gap by mixing a fraction of Hartree-Fock exchange to this functional [14]. The

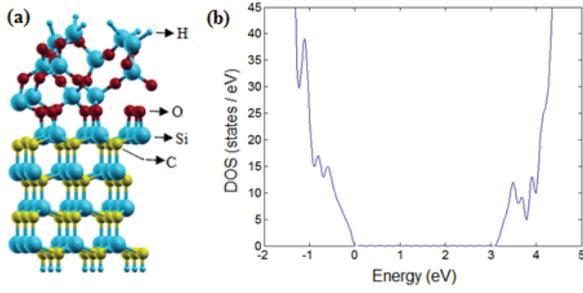


Figure 1: a) Abrupt SiC/SiO₂ interface, b) total DOS of the abrupt interface structure, showing the bandgap

abrupt interface supercell and its calculated density of states are shown in Figure 1.

Single Carbon interstitial defect: During the oxidation of SiC, carbon is believed to be removed as CO [15]. Recently, Hijikata et al. proposed emission of C into SiC substrate during oxidation [16]. Therefore, a single interstitial C atom was placed inside the SiC side of the interface and geometric optimization was performed using DFT. As a result of the atomic rearrangements, we obtained a relaxed structure containing a Si-C-C bridge [8]. We then carried out a DFT simulation of the pDOS of the impurity Carbon atom on the relaxed interface structure. The projected Density of States (pDOS) gives the contribution of orbitals of individual atom to the total DOS of the system. The calculated pDOS of the single Carbon interstitial atom is shown in Figure 2. The calculations indicate that the single C interstitial introduces three trap states in the bandgap – at 2.5, 0.45 and 0.15 eV below the conduction band (3.26 eV).

Carbon dimer interstitial defect: This defect includes double bonded carbon atoms, each of which is connected to a Si and C atom. This configuration - represented as SiC-C=C-SiC - was investigated in [4]. The formation of this defect was also proposed using quantum molecular dynamics studies [5, 17]. Subsequent to the introduction of C dimer defect into the structure and its geometric relaxation, we performed DFT simulations to determine its pDOS. The calculated pDOS is given in Figure 2. The calculations point to the introduction of trap levels at mid-gap and at 0.15 eV below the conduction band. This is at variance with the calculations in [18].

B. 2D-Device Simulation

We simulated the I-V characteristics of the SiC device using the in-house drift-diffusion based device simulator for different temperatures [2, 11, 12]. The experimental and simulated I-V plot in the low-voltage regime of a 50A vertical power SiC DMOSFET is shown in Figure 3. While the simulator simultaneously solves the semiconductor equations, it accounts for the effect of interface traps, fixed oxide charges, incomplete ionization and various factors affecting mobility. Mobility modeling includes Coulomb scattering from trapped charges and impurities, surface roughness scattering, surface phonon scattering and velocity saturation effects. Bandgap narrowing with temperature is also included.

The density of trap states in the SiC bandgap (D_{it}) is

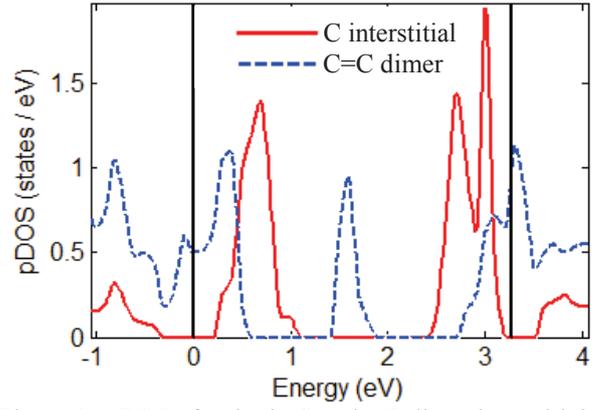


Figure 2: pDOS of a single C and a C dimer interstitial defect. Bandgap is between the vertical lines

modeled using an exponential function.

$$D_{it}(E_t) = D_{it-mid} + D_{it-edge} \exp\left(\frac{E_t - E_c}{\sigma(T)}\right) \quad (1)$$

where E_t is the trap energy level, E_c is the conduction band level and fitting parameters $D_{it-mid} = 1.35 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$, $D_{it-edge} = 1.78 \times 10^{13} \text{ cm}^{-2} \text{ eV}^{-1}$ and $\sigma(T) = 89 \text{ meV}$. The exponential function of D_{it} is representative of the experimentally determined trap DOS spectrum [1]. The total number of occupied acceptor states (N_{tot}) is calculated by integrating the product of D_{it} and state occupancy probability function $f(E_t)$ from midgap to the conduction band edge. The probability function is given as

$$f(E_t) = \frac{1}{1 + \frac{1}{2} \exp\left(\frac{E_t - E_F}{kT}\right)} \quad (2)$$

where k is the Boltzmann constant and E_F is the Fermi level.

C. Identification and Quantification of defects

As mentioned above, DFT calculations are used to extract the location of bandgap states introduced by defects in a 4H-SiC/SiO₂ interface. However, the size of the interface slab that can be simulated is severely limited by computational capacity. This makes the simulation of a practical interface containing millions of atoms and the extraction of real defect density of states impossible, even on a supercomputer. On the contrary, 2D-device simulation can give quantitative results for the total number of occupied traps at the interface, although it cannot identify the nature of defects at the atomic level. Thus, by integrating these different techniques, one could both identify and quantify defects at the SiC/SiO₂ interface.

In order to make a connection between DFT and 2-D device simulation, we model the DOS due to a specific type of acceptor trap j , at energy E_{tj} , in the upper half of bandgap to be

$$D_{itj}(E_{tj}) = N_{tj} \delta(E - E_{tj}) \quad (3)$$

where N_{tj} is the concentration of the trap. For m different types of traps at a given V_{GS} and T , the total number of occupied traps (N_{tot}) is

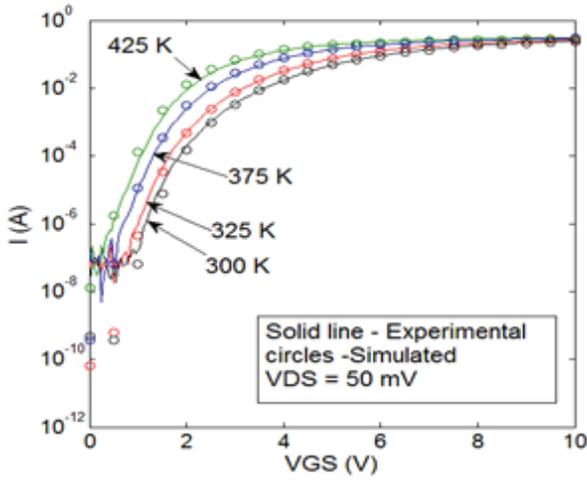


Figure 3: 2-D device simulation of a SiC MOSFET

$$\sum_{j=1}^m N_{tj} f(E_{tj}, V_{GS}, T) = N_{tot} \quad (4)$$

where N_{tj} and E_{tj} correspond to the concentration and energy level of trap type j and f is the probability function derived from Fermi statistics. N_{tot} is extracted from 2D-device simulation and experiment, while E_{tj} is calculated from DFT.

Details of the method are given as a flow chart in Figure 4. We begin by assuming that there are m distinct types of traps in the device. The entire energy space in the upper half of the band gap is sampled for appropriate trap levels. For each trap energy sample, equations of form (4) are formed by performing 2D device simulations at different voltages. This over-determined system of linear equations, shown in equation (5), is solved using the method of least squares.

$$[F]_{k \times m} [N]_{m \times 1} = [N_{tot}]_{k \times 1} \quad (5)$$

Here, $[F]$ is the matrix with trap occupancy probability functions, $[N]$ is the unknown trap concentration vector and $[N_{tot}]$ is total trap occupancy vector. We convert $[F]_{k \times m}$ to a square matrix by multiplying both sides with its transpose, $[F^T]$. We then solve for $[N]$ by Gaussian elimination.

$$[N]_{m \times 1} = ([F^T]_{m \times k} [F]_{k \times m})^{-1} [F^T]_{m \times k} [N_{tot}]_{k \times 1} \quad (6)$$

The over-determined system of equations might not have a unique solution. Thus, we find a solution such that the sum of squares of error is the least. The procedure is repeated for various temperatures. The correct trap energy set is found when its individual concentrations are invariant for different temperatures. The extracted trap levels are then compared with the DFT results to identify the specific defects.

III. DISCUSSION AND RESULTS

Using DFT calculations, the three trap energy levels induced in the bandgap by a single Carbon interstitial in SiC substrate were calculated to be 2.5, 0.45 and 0.15eV below the conduction band (CB) edge. Similarly, a Carbon dimer interstitial in SiC is found to give rise to two energy levels-one at 0.1eV below the CB edge and another in the mid-gap.

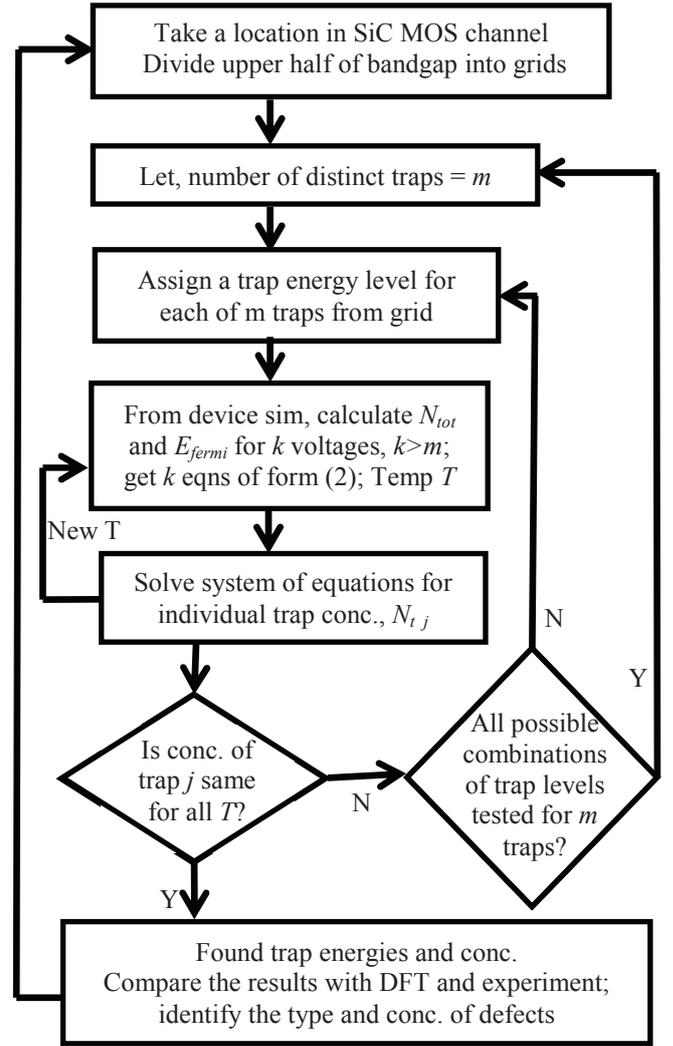


Figure 4: Methodology to identify interface defects

A 2D-device simulation of SiC power MOSFET was also performed at different temperatures. Using the methodology outlined in section II C, the trap levels were identified. The over-determined system of linear equations was formed in the gate voltage range of 1.5V to 1.7V, in steps of 5mV (forming a system of six equations). The band gap was explored for two, three and four trap levels. The least percentage error in calculated trap concentration with varying temperatures was observed for the case of two trap levels, located at 0.45 and 0.15 eV below the conduction band. By comparing with DFT calculations, this defect is likely to be single Carbon interstitial in the SiC substrate. Their concentration was calculated by summing the individual trap concentrations. We also identified states in the midgap and at 0.1 eV below CB, corresponding to C dimer defect. The results are provided in Table 1 for various points along the channel.

The basic assumption used in evaluating the defect levels and defect concentration using the method outlined above is that they remain constant over the temperatures of I-V measurement. Moreover, to form the system of equations, the

TABLE 1
Energy level, type and concentration of traps in the channel

x μm	$E_{t,1}$ eV	$N_{t,1}$ (10^{11} /cm ²)	$E_{t,2}$ eV	$N_{t,2}$ (10^{12} /cm ²)	Type of defect	Total defect conc. 10^{12} /cm ²
0.70	Mid gap	2.53	3.15	7.95	-C=C-	8.20
0.75	2.85	2.58	3.10	1.86	C	2.12
0.80	2.80	2.40	3.10	2.45	C	2.69
0.84	2.80	2.40	3.10	2.50	C	2.74
0.88	2.80	2.41	3.10	2.41	C	2.65

simulations are performed at a drain voltage of 1μV. This not only ensures that the Fermi levels are constant along the channel, but also eliminates numerical noise in the calculations. Another critical aspect is the choice of the range and spacing of gate voltage over which the over-determined system of equations is formed. The gate voltages are chosen to be at relatively low gate voltages because this is where the effect of interface traps is maximally felt. The spacing is carefully chosen in such a way that the probability of occupancy (f) changes appreciably with each increment (5mV) of the gate voltage. This prevents the system of equations having infinite solutions and reduces numerical errors.

The proposed method confines the identified defect and their concentration to the interface. Previous calculation by Basile et al. identifies the defect to be Carbon dimer interstitial with an estimated concentration of 6×10^{11} / cm² spread over 2nm into the depth of the device [10]. If we were to distribute the interfacial concentration of defect (Table 1) over 2nm, we obtain a defect concentration of 8.8×10^{11} /cm², in reasonable agreement with [10].

We have identified single Carbon interstitials to be the major contributor of trap states near CB edge. We also identified C dimer interstitial defect to be present which has also been indicated by other investigators [5, 10, 17, 18]. In addition, we calculated its concentration. It should be noted that while this study assumes the Kohn-Sham energy levels obtained from DFT simulations to be the location of trap states, similar DFT studies elsewhere propose charge transition levels of defects to be the real trap levels. Charge transition level based DFT calculations will be performed in future and the technique presented here will subsequently be applied to extract more accurate information on the nature of near-interface defects.

IV. CONCLUSION

We outlined a novel generic methodology for the identification and quantification of near-interface traps in SiC DMOSFET responsible for low channel mobility. This was done by integrating DFT simulations with 2D-device simulation of a SiC power MOSFET. DFT based investigation

of single Carbon and Carbon dimer interstitials were carried out. We identified single Carbon interstitial to be responsible for the near-interface traps. The concentration of these interstitials was calculated to be about 2.7×10^{12} /cm² at the interface. More detailed charge transition level based calculations need to be performed to identify the nature of the defects more accurately.

REFERENCES

- [1] V.V. Afanasev, M. Bassler, G. Pensl and M. Schulz, "Intrinsic SiC/SiO₂ interface states," Phys. Stat. sol (a), vol. 162, pp. 321-337, 1997.
- [2] S. Potbhare, N.Goldsman, G.Pennington, A. Lelis and J.M. McGarrity, "A quasi-two-dimensional depth-dependent mobility model suitable for device simulation for Coulombic scattering due to interface trapped charges," J. Appl. Phys, vol. 100, 044516, 2006.
- [3] J.M. Knaup et al., "Defects in SiO₂ as the possible origin of near interface traps in the SiC/SiO₂ system: A systematic theoretical study," Phys. Rev. B, vol. 72, 115323, 2005.
- [4] F. Devynck and A. Pasquarello, "Semiconductor defects at the 4H-SiC (0001)/SiO₂ interface," Physica B, 401-402, pp. 556-559, 2007.
- [5] X. Shen et al., "Excess Carbon in Silicon Carbide," J. Appl. Phys, vol. 108, 123705, 2010.
- [6] C.J. Cochrane, P.M. Lenehan, and A.J. Lelis, "Identification of a Silicon vacancy as an important defect in 4H-SiC metal oxide semiconducting field transistor using spin dependent recombination," Appl. Phys. Lett., vol.100,023509,2012.
- [7] T. Zheleva et al., "Transition layers at the SiO₂/SiC interface," Appl. Phys. Lett., vol. 93, 022108, 2008.
- [8] S. Salemi, N. Goldsman, D.P. Ettisserry, A. Akturk, and A. Lelis, "The effect of defects and their passivation on the density of states of the 4H-Silicon Carbide/ SiO₂ interface," J. Appl. Phys., vol. 113, 053703, 2013.
- [9] P. Deak et al., "The mechanism of defect creation and passivation at the SiC/SiO₂ interface," J. Phys. D: Appl. Phys., vol. 40, pp. 6242-6253, 2007.
- [10] A. F. Basile and P. M. Mooney, "Modeling of high frequency capacitance-voltage characteristics to quantify trap distributions near SiO₂/SiC interfaces," J. Appl. Phys., vol. 111, 094509, 2012.
- [11] S. Potbhare et al., "A physical model of high temperature 4H-SiC MOSFETs," IEEE Transactions on Electron Devices, vol. 55, iss. 8, pp. 2029-2040, 2008.
- [12] S. Potbhare, N. Goldsman, G. Pennington, A. Lelis, and J. M. McGarrity, "Numerical and experimental characterization of 4H- silicon carbide lateral metal-oxide-semiconductor field-effect transistor," J. Appl. Phys., vol. 100, 044515, 2006
- [13] P. Giannozzi et al., "QUANTUM ESPRESSO: a modular and open-source software project for quantum simulations of materials," J. Phys.: Condens. Matter, vol.21, 395502, 2009.
- [14] F. Devynck, F. Giustino, P. Broqvist, and A. Pasquarello, "Structural and electronic properties of an abrupt 4H-SiC(0001)/SiO₂ interface model: Classical molecular dynamicssimulations and density functional calculations," Phys. Rev. B, vol. 76, 075351, 2007.
- [15] Y. Song, S. Dhar, L.C. Feldman, G. Chung, and J. R. Williams, "Modified Deal Grove model for the thermal oxidation of silicon carbide," J. Appl. Phys., vol. 95, 4953, 2004.
- [16] Y. Hijikata, H. Yaguchi, and S. Yoshida, "Theoretical studies for Si and C emission into the SiC layer during oxidation," Materials Science Forum, vol. 679-680, pp. 429-432, 2011.
- [17] X. Shen and S. T. Pantelides, "Identification of a major cause of endemically poor mobilities in SiC/SiO₂ structures," Appl. Phys. Lett., vol. 98, 053507, 2011.
- [18] F. Devynck, A. Alkauskas, P. Broqvist and A. Pasquarello, "Energy levels of candidate defects at SiC/SiO₂ interfaces," AIP Conf. Proc. 1199, pp. 108-109, 2010.