Comparison of Raised Source/Drain Implant-Free Quantum-Well and Tri-Gate MOSFETs using 3D Monte Carlo Simulation

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***Abstract*— In this paper we examine the impact of a raised source/drain architecture on the performance of single-gate and multi-gate, high mobility channel MOSFETs. We make use of 3D Monte Carlo (MC) simulations to predict the performance of InGaAs n-type and Germanium (Ge) p-type MOSFETs. The transition from a raised source/drain Implant-Free Quantum-Well (IFQW) MOSFET to an Implant-Free Tri-gate MOSFET is expected to show both improved electrostatic behaviour and better drive current due to the larger gated channel area. We show that although significant electrostatic improvement is demonstrated in the tri-gate case, there is poor on-current performance in comparison to the IFQW MOSFET due to increased access resistance to the fin channel from the raised source/drain.**

Keywords*— *Monte Carlo, III-V, InGaAs, Germanium, FinFET, Multi-Gate, Raised Source/Drain.

I. INTRODUCTION

The 2012 edition of the International Roadmap for Semiconductors (ITRS) indicates that there is significant interest in deploying III-V/Ge channel materials at and beyond the 14nm technology node [1]. The advantages of using III-V materials in the channel of n-MOSFETs include high low field mobility and electron velocity [2,3] along with better drive current at reduced supply voltages [4]. Furthermore, recent CMOS generations have seen a transition from planar devices towards multi-gate architectures [5] due to increasing levels of leakage and statistical variability impacting device and circuit performance, yield and reliability. Various new transistor architectures have been considered to derive the maximum benefit from the high-mobility III-V materials including planar quantum-well [6-8], tri- or multi- gate [9, 10], and nanowire transistors [11-13]. Among these the tri-gate architecture offers simultaneously high channel mobility and drive current along with excellent electrostatic integrity [10].

Achieving high-doping levels (>10^{19}cm^{-3}) in high-mobility materials for source/drain regions can be very challenging but is essential for high device performance [14]. Such high doping levels have never been reported for implantation and the highest recorded doping concentrations are for in-situ doped materials [15]. This has led to the introduction of regrown raised source/drain regions for high-mobility transistors [8, 10]. Here we examine the impact that this raised source/drain region has on the drive current performance of a single-gate IFQW MOSFET against a tri-gate MOSFET.

The paper is organized as follows. Section II discusses the simulation methodology employed. Section III describes the device architecture. Section IV verifies the accuracy of the simulation methodology in reproducing experimental results. Section V presents the results of the raised source/drain analysis. Finally section VI summarizes and concludes on the main findings of the work.

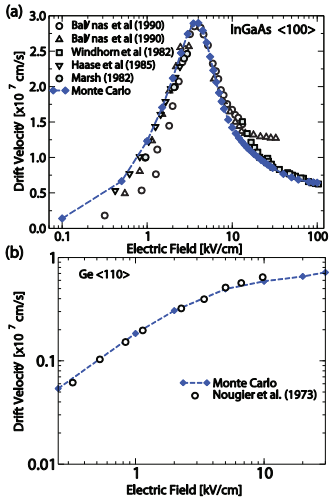

Fig. 1. Velocity-field characteristic of (a) InGaAs and (b) Ge from Monte Carlo simulation against experimental data.

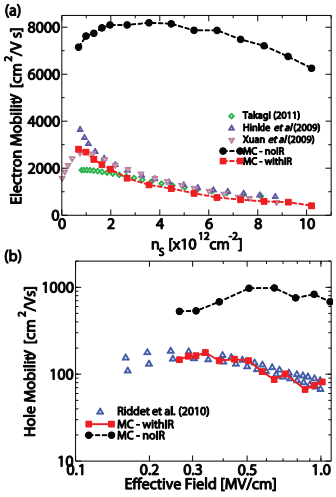

Fig. 2. Universal mobility characteristic of (a) InGaAs and (b) Ge from Monte Carlo simulation against experimental data.

II. SIMULATION METHODOLOGY

The 3D drift-diffusion (DD) and Monte Carlo (MC) modules of GARAND [16] are used in this study to provide accurate physical treatment of the sub-threshold electrostatic behaviour (DD) and the non-equilibrium transport behaviour at high field (MC). Both modules of GARAND implement efficient density-gradient quantum-corrections [17] and account for degeneracy through Fermi-Dirac statistics and modification of inelastic scattering processes [18]. The MC

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module employs the typical scattering mechanisms including acoustic, optical and polar optical phonons, ionized impurity and interface roughness scattering. The scattering parameters for these models have been calibrated to match the experimentally measured characteristics (Figs. 1-2) but in this study interface roughness scattering has been neglected to give an upper bound on the high field performance.

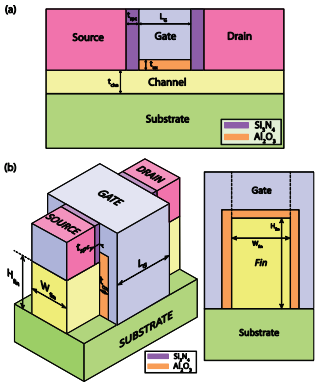

Fig. 3. Structure of (a) the Implant-Free Quantum-Well and (b) the Implant-Free Tri-gate MOSFET architectures.

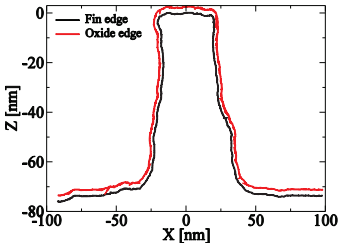

Fig. 4. Extracted fin profile for a W_{fin}=45nm tri-gate FET from Radosavljevic *et al. 2011* [10].

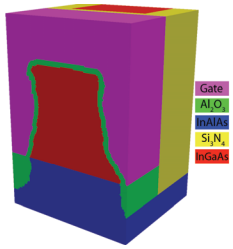

Fig. 5. Device structure with extracted fin profile W_{fin}=45nm as used in the GARAND simulator.

Table 1: IFQW and Tri-gate structure dimensions.

L_G [nm]	EOT [nm]	T_{ox} [nm]	t_{spc} [nm]
15	0.51	1.125	2

Table 2: IFQW and Tri-gate doping concentrations.

Src/Drn [cm^{-3}]	Chn. [cm^{-3}]	Subs. [cm^{-3}]
9.1×10^{19}	1.82×10^{17}	3.65×10^{18}

III. Device Architectures

For the purpose of this work the transistors have been designed to have similar structural details. The structure of the IFQW and the Tri-gate MOSFET is illustrated in Fig. 3. The MOSFET dimensions and doping are given in Tables 1-2. All devices have a high-κ Al_2O_3 gate oxide with a Si_3N_4 lateral spacer. The source and drain regions for the nMOS(pMOS) are epitaxial, in-situ doped raised $In_{0.53}Ga_{0.47}As$ (Ge), the channel is $In_{0.53}Ga_{0.47}As$ (Ge) and the substrate is $In_{0.52}Al_{0.48}As$ (Si). The IFQW transistor has a channel thickness t_{chn}= 3.75nm and the Tri-gate has a fin width of W_{fin}= 10nm, and height H_{fin}= 25nm. The channel width of the IFQW is 15nm, and for the Tri-gate it is $W_{fin}+2\times H_{fin}$= 60nm.

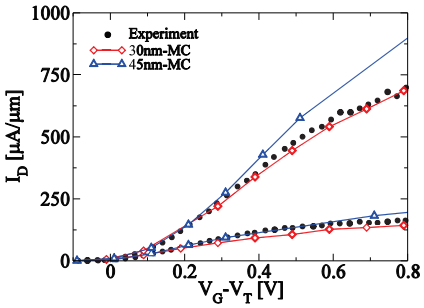

Fig. 6. Monte Carlo results of drive current against published data from Radosavljevic *et al.* [10].

IV. Experimental Verification

Before moving to the results of this study, we will verify the MC simulation against some experimental data for a III-V n-type tri-gate transistor. The structure of the tri-gate MOSFET illustrated in Fig. 3(b) replicates the structure described in the work of Radosavljevic *et al.* [10]. For this experimental comparison, we will use the structure dimensions given in [10] (see Fig 6(b) of reference) which are L_G=60nm, t_{spc}=5nm, W_{fin}=40nm, H_{fin}=50nm, EOT=12Å. Fig. 3 of [10] also presents fin profiles that have been extracted (see depiction in Figs. 4-5) and applied to the simulated structure. The DD module of GARAND is then employed to match the gate workfunction of the I_D-V_G curves at V_D=50mV and V_D=0.5V. Following this, the MC module of GARAND is used to evaluate the I_{ON} performance as shown in Fig. 6, highlighting the accuracy of MC simulation when compared to experimental results.

V. Impact of Raised Source/Drain Contacts

The I_D-V_G characteristics at a fixed I_{OFF}=0.1μA/μm for the two devices in Fig. 3 are shown in Fig. 7 for the nMOS and Fig. 8 for the pMOS. We can report from DD simulation that the SS is vastly improved from 88mV/dec (95mV/dec) in the IFQW to 68mV/dec (69mV/dec) in the Tri-gate, and DIBL improves from 85mV/V (70mV/V) to 29mV/V (23mV/V) in the nMOS (pMOS). In short, the subthreshold behaviour of the Tri-gate device is vastly superior to the IFQW MOSFET.

It is clear from Fig. 7 and Fig. 8 that the drive current at high V_G is much lower in the Tri-gate MOSFET than the IFQW. This is not expected as the increased gate control of the Tri-gate device should offer greater channel charge density and therefore increased current density. The reasons for this underperformance will be discussed in the following sections.

A. InGaAs Channel

Fig. 7 shows that below V_G=0.6V the Tri-gate outperforms the IFQW, with higher V_G the drive current is degraded as a result of higher access resistance. Examining the electron sheet density and average velocity at V_G=1V in Fig. 9 and V_G=0.6V in Fig. 11 shows that at the lower gate bias the channel velocity is significantly increased. As is expected, the Tri-gate consistently has higher channel sheet density due to a larger gated area.

It has been reported elsewhere that better relative performance of III-V MOSFETs is possible at lower supply

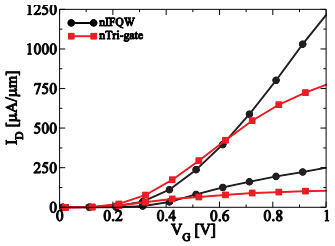

Fig. 7. I_D-V_G characteristic of the n-type IFQW and Tri-gate MOSFETs for a fixed I_{OFF}=0.1μA/μm.

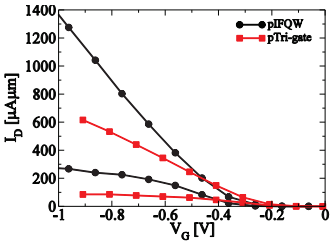

Fig. 8. I_D-V_G characteristic of the p-type IFQW and Tri-gate MOSFETs for a fixed I_{OFF}=0.1μA/μm.

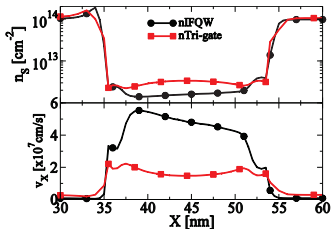

Fig. 9. Sheet electron density and electron velocity through the channel of the n-type IFQW and Tri-gate MOSFETs at V_G=1V.

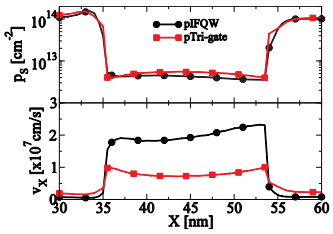

Fig. 10. Sheet hole density and hole velocity through the channel of the p-type IFQW and Tri-gate MOSFETs at V_G=0.9V.

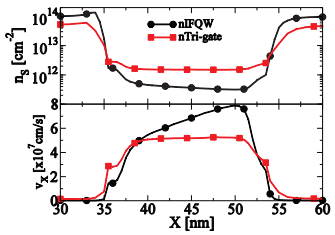

Fig. 11. Sheet electron density and electron velocity through the channel of the n-type IFQW and Tri-gate MOSFETs at V_G=0.6V.

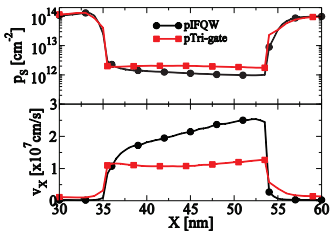

Fig. 12. Sheet hole density and hole velocity through the channel of the p-type IFQW and Tri-gate MOSFETs at V_G=0.6V.

voltages [3]. Here we can use numerical simulation to understand why this is the case.

The behaviour of the channel velocity of the InGaAs channel devices can be understood by examining the valley occupations shown in Fig.13 at V_G=1V and Fig. 14 at V_G=0.6V. At high gate bias both devices have an appreciable electron population in the heavy effective-mass L-valleys, more so in the Tri-gate, which has a correspondingly lower channel velocity. When the gate bias is reduced the electron population in the channel of both devices is highest in the light effective-mass Γ -valley, thereby increasing the channel velocity. The increased L-valley population in the channel of the Tri-gate at V_G=1V is due to the increased charge density in the channel area that in turn increases the average carrier energy through degeneracy, and makes inter-valley transfer to the L-valleys much more probable.

B. Ge Channel

Although in the Ge channel FETs there is a small increase in velocity at lower V_G, it is not nearly as pronounced as in the InGaAs FETs. Instead there is a consistent drop in channel

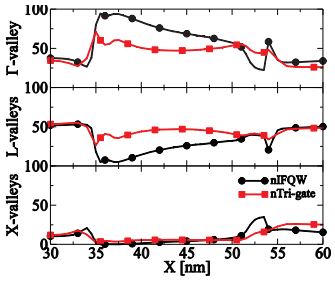

Fig. 13. InGaAs valley occupation through the channel of the n-type IFQW and Tri-gate MOSFETs at V_G=1V.

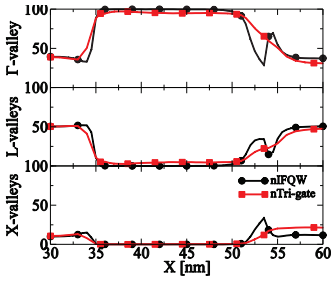

Fig. 14. InGaAs valley occupation through the channel of the n-type IFQW and Tri-gate MOSFETs at V_G=0.6V

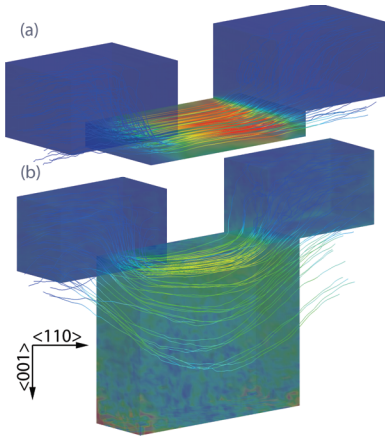

Fig. 15. Velocity vector stream tracer for holes in the p-type (a) IFQW and (b) Tri-gate MOSFETs at V_G=0.6V.

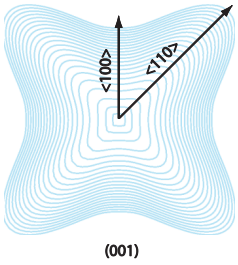

Fig. 16. Equi-energy contours on the (001) plane in **k**-space of the Ge bandstrcture for Heavy Holes (HH).

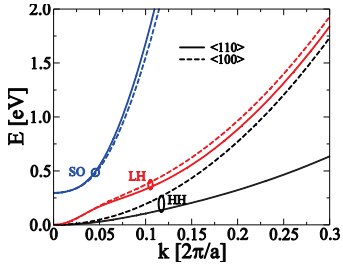

Fig. 17. E-k relation of the warped Ge bandstructure for two different transport directions.

velocity, roughly 50%, in the Tri-gate with respect to the IFQW. The drop in channel velocity of the Ge channel p-type Tri-gate we attribute to the warped bandstructure that leads to anisotropic transport behaviour.

Fig. 15 shows the velocity vector stream tracer through the channel of the IFQW and Tri-gate that represents the typical path of a carrier. We can see that in the IFQW channel the carriers are strongly confined and have minimal vertical velocity movement. This is in contrast to the Tri-gate in which the carriers move a relatively large distance vertically in the fin, particularly at the start of the channel that controls device performance.

The Ge hole bandstructure shown in Fig. 16 and Fig. 17 highlight the dependence of transport direction on the effective-mass as seen by a carrier. That is, the anisotropic nature of the bandstructure means that transport in different directions can hinder or improve the carrier velocity. In this work a (001) Ge substrate is used which leads to carriers experiencing a lighter effective mass in the <100> (equivalent to <001>) direction than in the channel plane of <110> for the HH and LH bands that dominate transport.

As a result of the Ge bandstructure in this case, carriers travelling vertically in the fin will experience higher velocity, for the equivalent energy, than in the lateral channel plane. This has the consequence of distributing the carriers further away from the source/drain regions, and reducing the lateral velocity.

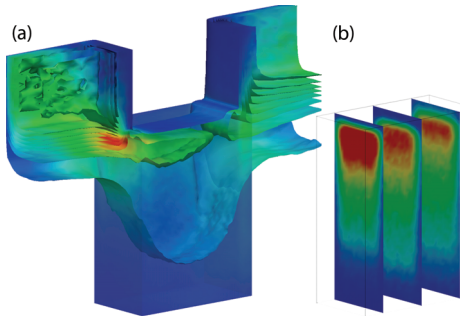

Fig. 18. (a) Electron equi-concentration contours coloured by current density through the fin channel of raised source/drain tri-gate MOSFET. (b) Current density slices through the fin channel of the raised source/drain tri-gate MOSFET.

C. Channel Population

Having now discussed the relative channel velocity issues of the high-mobility channel materials in a Tri-gate, we have some understanding why the Tri-gate underperforms relative to the IFQW. There is a further reason that applies to both n- and p-type Tri-gates causing the lack of performance. If we examine the current density profiles, shown for the n-type InGaAs device in Fig. 18, we can see that only the upper third of the fin is really populated. The raised source/drain architecture is very successful in providing carriers to a surface channel design such as the IFQW, but with a fin it struggles to provide carriers for the full fin area. This inability to provide adequate carriers to the full fin cross-section greatly restricts the performance and suggests that an improved source/drain design is required to achieve full fin activation.

VI. Conclusions

We have shown in this paper that to take the full advantage of Tri-gate MOSFETs with high-mobility channels an improved source/drain design is required that can populate the full fin cross-section for current transport. We have demonstrated that high-mobility channel MOSFETs offer higher relative performance at low applied voltages. With a raised source/drain design, the IFQW MOSFET is a better choice as it offers superior drive current performance. The Tri-gate design has significant improvements in terms of electrostatic control but a better design of the source/drain is required to attain the full drive current performance. The coupled 3D GARAND DD and MC numerical simulation approach has also demonstrated strong predictive capabilities for future MOSFET technologies by reproducing published experimental data for the III-V tri-gate MOSFET.

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