Addressing Key Challenges in 1T-DRAM: Retention Time, Scaling and Variability - Using a Novel Design with GaP Source-Drain

Ashish Pal, Aneesh Nainani and Krishna C. Saraswat
Center of Integrated Systems, Stanford University, Stanford, CA,USA
Email: apal@stanford.edu

***Abstract*—We propose a vertical gate all around 1-transistor DRAM cell with silicon channel and gallium phosphide source drain (GaP-SD) as a viable alternative to the present 1T-1C DRAM technology. The valence band offset at GaP and Si interface helps to store more holes in the transistor body and thus improves the retention time by 2 order over conventional Si-SD 1T DRAM. By examining body thickness variability, we conclude that GaP-SD memory cell can withstand the performance degradation due to device variability to meet the ITRS retention time requirements. Finally the GaP-SD memory cell is optimized for scaled dimensions upto 20nm body thickness to establish its superiority at lower technology nodes.**

I. Introduction

As the scaling of conventional 1T-1C DRAM has become increasingly difficult, there has been a significant interest to find a suitable alternative. The 1T-DRAM [1] is of special interest because it eliminates the capacitor, but suffers in drawbacks due to poor retention time and scalability. In this paper, we propose a vertical 1T-DRAM cell with single gate all around Si channel and gallium phosphide source drain (GaP-SD) to improve its performance. Fig. 1(a) shows the proposed device and the corresponding 2D-cross section (Fig. 1(b)). The proposed cell can be realized on bulk Si and thus avoids the costly conventional SOI based 1T-DRAM. Use of single gate eliminates the layout penalty associated with having a back contact for conventional 1T-DRAM, thus making the cell more compact and achieving an 4F2 cell design. Finally, improved retention time and scalability are achieved by replacing Si source/drain with GaP source and drain. GaP is nearly lattice matched to Si with demonstrated defect free growth on Si by MOCVD and MBE [2]–[4]. Electrical characterization results of the GaP-Si interface using GaP-Si heterojunction diode and silicon transistor with GaP source/drain also support this fact [5]. GaP has a high valence band offset to Si (VBO) (Fig. 2) [6]. This VBO helps in storing more holes and in confining them efficiently inside the Si channel by providing high barriers at source and drain, thereby increasing the retention time.

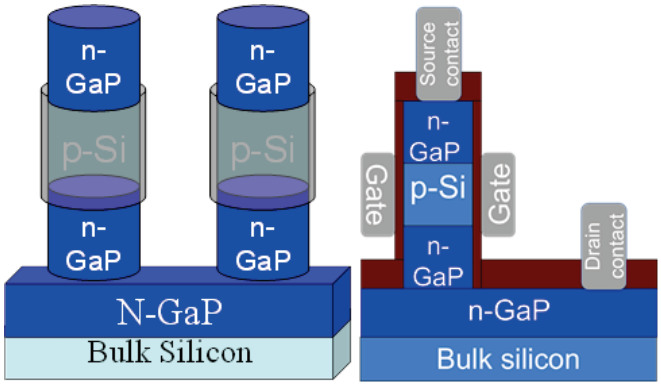

Fig. 1. Proposed Vertical GaP source drain (GaP-SD) 1TDRAM memory cell (b) 2D structure used in simulation

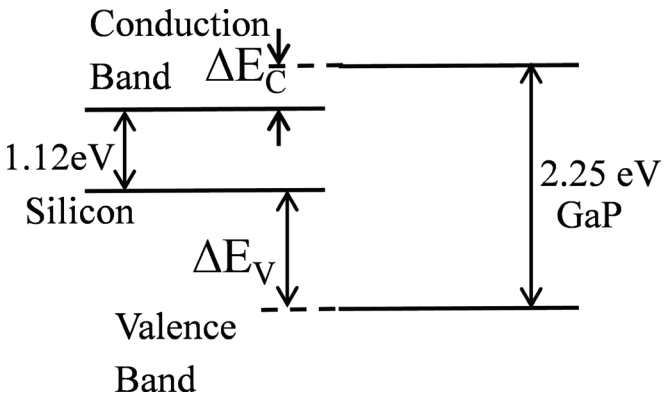

Fig. 2. Band line up between GaP and Si. ΔE_C is ~0.1 V and ΔE_V is ~1V

II. Simulation Setup

2-D Poisson equations with hydrodynamic models are used to calculate the retention time improvement of the proposed cell. The cell dimensions [7] and voltages are listed in Table 1. A sense margin of 10μA/μm is assumed to be required to distinguish between logic state '0' and '1'. Since the proposed cell has a single gate (needed for 4F2 design), a BJT-latch based programing method [8] is chosen rather than the conventional impact ionization which makes use of two separate gates and also consumes higher power. Fig. 3 shows the BJT latch characteristics for GaP-SD and conventional Si-SD cell. Both devices show similar latch-up time. However, due to the band-offset at channel-source and channel-drain junctions, GaP-SD device is capable to store more holes inside the channel than the Si-SD device. Thus at V_{GS}= -2V, the

978-1-4673-5736-4/13/$31.00 ©2013 IEEE

TABLE I
1T DRAM CELL SPECIFICATIONS

Dimensions/Specs	Value
L_G	55nm
T_{Si}	54nm
T_{Ox}	5.6nm
Read Bias	V_{GS}=-2V V_{DS}=1.2V
'0' I_{Read} (25°C)	$\sim 0.2\mu A/\mu m$
'0' I_{Read} (85°C)	$\sim 2\mu A/\mu m$
Target '1' I_{Read}	$\sim 12\mu A/\mu m$
Target ΔV_T (85°C)	$\sim$ 0.275V

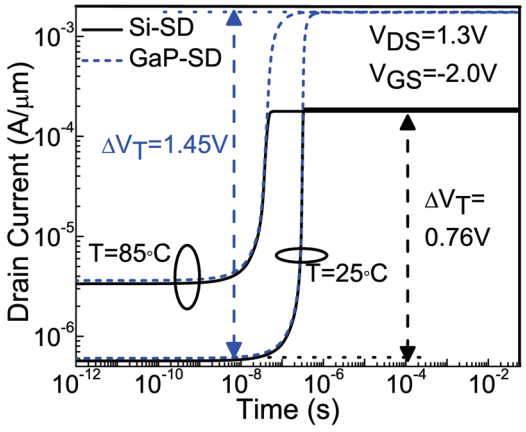

Fig. 3. BJT Programing results in higher V_T shift for GaP-SD device than Si-SD device

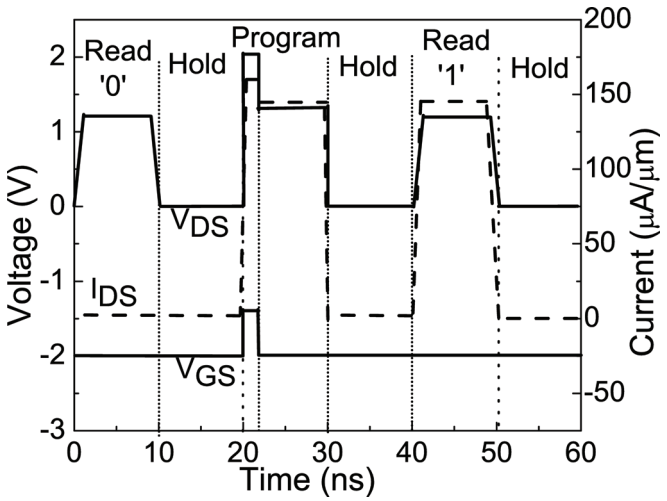

Fig. 4. Timing diagram showing bias conditions for program, read and hold state.

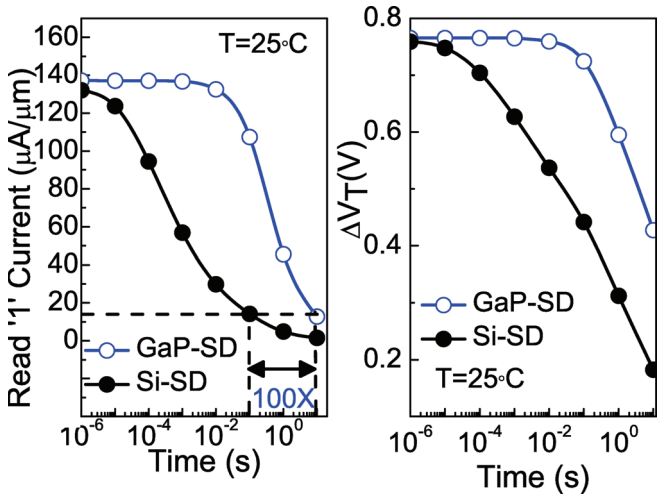

Fig. 5. Variation of read '1' state current and threshold voltage shift with time shows 100X improvement of retention time for GaP-SD device at room temperature.

highest achievable V_T-shift (ΔV_T) for Si-SD cell is $\sim$0.75V, whereas GaP-SD device achieves a ΔV_T of $\sim$1.45V. This emphasizes the importance of VBO at the GaP-Si interface.

III. PERFORMANCE COMPARISON

A. Retention Time

We compare the retention time of GaP-SD and Si-SD device for the same programmed V_T-shift and program power. The voltages and pulse sequences for programming and reading are shown in Fig. 4. No voltage is applied on the source and drain during the hold state. Fig. 5 and 6 show the V_T-shift and logic '1' state read current for room temperature (25°C) and 85°C operation respectively. The Si-SD device has been programmed to its full capacity at 25°C to have the maximum retention time. So the major leakage mechanism for Si-SD cell is leakage at the channel-source and channel-drain p-n junctions. As a result, it loses its charge much quicker and shows a retention time of only $\sim$100ms at 25°C. However for the GaP-SD device, primary charge leakage mechanism is SRH generation-recombination as the p-n junction leakage is greatly limited by the band offsets at the GaP-Si heterojunction (Figure 2). This results in $\sim$10s of retention time for GaP-SD device, a 100X improvement over the conventional Si-SD device. The impact ionization rate increases at higher temperature and leads to reduced latch-up time and enhanced hole generation rate. As the Si-SD device has been programmed to its full capacity at 25°C, it cannot store the excess holes generated at 85°C. Moreover, the higher SRH recombination rate at 85°C reduces the stored hole density much quicker. This results in 10X reduction in the retention time of Si-SD device (10ms at 85°C). On the other hand, the VBO at GaP-Si interface helps the GaP-SD cell to store extra holes at 85°C inside the Si channel and results in a higher V_T-shift (Fig. 6). These additional holes at 85°C compensate for the higher SRH recombination to some extent. As a result the retention time of GaP-SD device at 85°C is about 1.5s - a reduction of 6.5X from retention time at 25°C. So it can be concluded that the GaP-SD cell is more temperature robust than the Si-SD

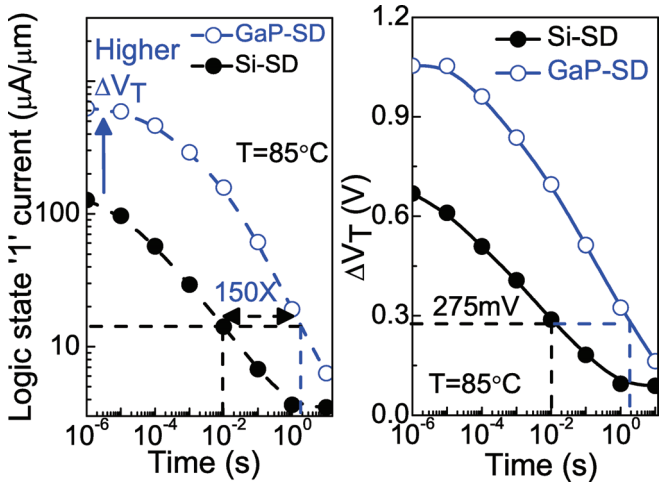

Fig. 6. Variation of read '1' state current and threshold voltage shift with time shows 150X improvement of retention time for GaP-SD device at elevated temperature(85°C).

memory cell.

B. Variability

For any practical applications, a DRAM array should have more than 98% cells working (have a V_T-shift > 275mV at 85°C to distinguish between state '1' and '0' in our design) even in the presence of device variability. For SOI-based 1T-DRAM device, the major parameters contributing to variability are T_{Si}, T_{BOX} and random dopant fluctuation (RDF) [9]. Our proposed cell eliminates the use of BOX and the associated variability. Also since we use a gate all around structure, our design does not utilize any channel doping and thus eliminates the variability effect of RDF. Elimination of two major sources of variability makes our proposed GaP-SD memory cell more robust to process variations. In the absence of T_{BOX} and RDF, T_{Si} becomes the important source of the variability in this device. Fig. 7 shows the effect of the body thickness variability on cell state '1' read current at T=85°C assuming a Gaussian distribution for T_{Si} with sigma=5% T_{Si}. The retention time of Si-SD cell need to be reduced to 0.1ms (almost 2 order reduction) to have 98% cells with a V_T-shift of higher than 275mV. However for our proposed GaP-SD 1T-DRAM, 99.8% cells meet the ΔV_T specification at 64ms thus satisfying both requirements of ITRS and practical applications.

C. Scalability

To reduce the cell area and hence to increase the density, the width of the silicon (T_{Si}) needs to be scaled. However, T_{Si} scaling increases the barrier height at source-channel p-n junction and thus reduces the feedback factor (β) in the BJT-based programing. To keep the latch-up time similar, the impact ionization factor (M) needs to be enhanced. Thus scaling of T_{Si} also calls for simultaneous gate length scaling (assuming same cell operating voltage). Fig. 8 shows the BJT latch-up effect for scaled devices with T_{Si}=30nm and 20nm. Reduction of T_{Si} severely limits the charge storage capability (hence maximum V_T shift) for Si-SD devices. But T_{Si} scaling does not affect the maximum V_T-shift for the GaP-SD cell to a great extent because of the higher storage capacity of the quantum well formed by GaP at source-drain with silicon channel (Fig. 8). Due to reduced V_T-shift, the Si-SD 1T-DRAM will have much inferior performance at these technology nodes. On the other hand, proposed GaP-SD cell retains enough performance even at these scaled T_{Si}. Figure 9 summarizes the retention time and variability performance of GaP-SD memory cell at these scaled technology nodes. For 30nm T_{Si}, our designed cell shows a retention time of 2s and 0.5s at T=25°C and 85°C respectively. Consideration of T_{Si} variability shows that 99% of cells will be in working

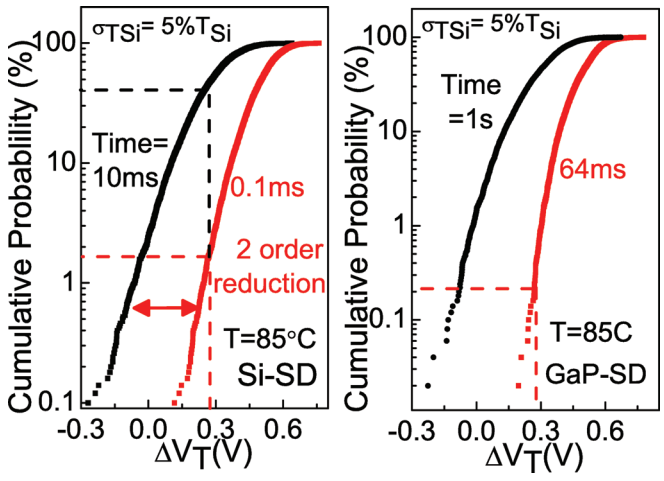

Fig. 7. Variability consideration of T_{Si} shows that retention time of Si-SD memory cells further reduces by ~2 order to achieve 98% cells working, whereas 99.8% GaP-SD memory cell will meet the ITRS specification of 64ms retention time at 85°C. 275mV of ΔV_T is used as a target to distinguish between logic state '1' and '0'.

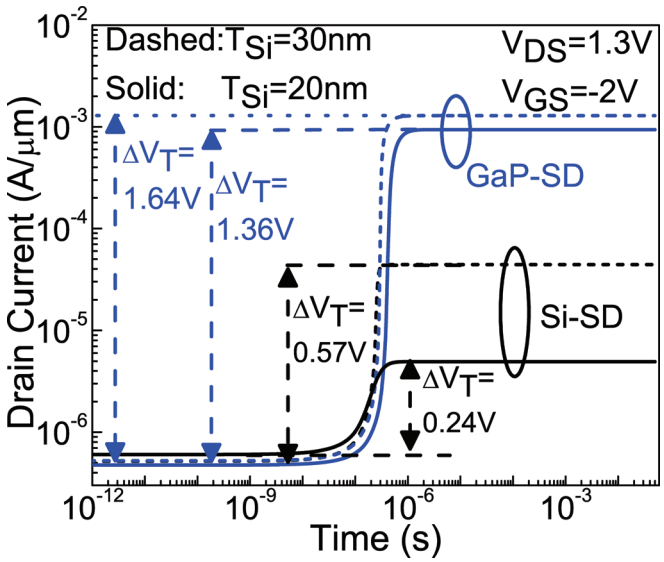

Fig. 8. Effect of T_{Si} scaling on charge storage ability of GaP-SD and Si-SD cell.

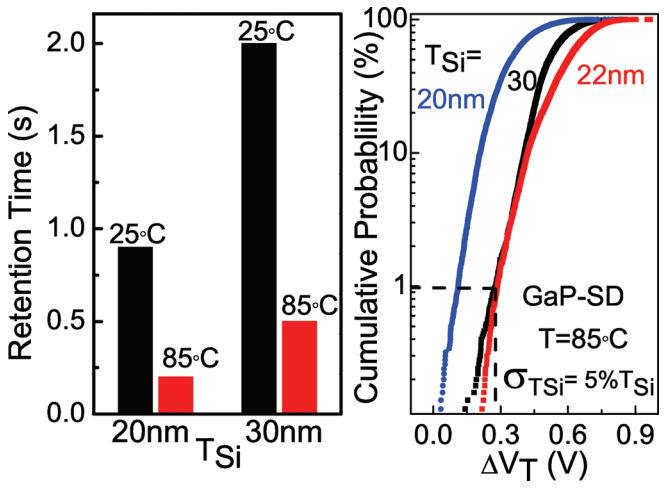

Fig. 9. Retention time and effect of T_{Si} variability for scaled GaP-SD devices at T_{Si}=30nm and 20nm

TABLE II
SPECIFICATIONS FOR OPTIMIZED SCALED 1T DRAM CELL

T_{Si}(nm)	30	20
L_G(nm)	35	30
T_{Ox}(nm)	5.6	5.1
T_R at 25°C (s)	2	0.9
T_R at 85°C (s)	0.5	0.2
Working Cell at 64ms	99%	73%
Modified T_{Si} for 99% working cell	30nm	22nm

condition (i.e. will have V_T-shift higher than 275mV) at 85°C). Although the designed cell for T_{Si}=20nm has only 73% working cells, slight modification in operating voltages (such as applying a positive hold voltage) or design can considerably improve the performance. As shown in figure 9, increase of T_{Si} to 22nm (keeping other device parameters same) will result in similar performance as of the cell with 30nm T_{Si} (99% working cells), thus matching the industry standard as well as ITRS specification. Table II shows the dimensions and performance matrices of the optimized GaP-SD memory cells at 30nm and 20nm T_{Si}.

IV. CONCLUSION

We proposed a vertical, single gate-all-around GaP source-drain 1T-DRAM cell. Our designed cell is realized on bulk Si substrate, and achieves 4F2 feature size and hence is ideal for high density DRAM industry. Simulations show that our cell has a retention time of 10s and 1.5s at T=25°C and 85°C respectively, thus having a 100X and 150X improvement over the similar Si-SD 1T-DRAM cell. Consideration of T_{Si} variability shows that 99.8% of proposed cells will meet ITRS requirement of 64ms of retention time. We also showed that our proposed cell can be scaled upto $\sim$ 20nm T_{Si}, showing 0.2s retention time at 85°C and having enough performance to withstand device variability.

ACKNOWLEDGMENT

This work was supported by the Stanford University Initiative for Nonvolatile Memory Materials and Devices (NMTRI), FCRP Center on Materials, Structures, and Devices and by a Stanford Fellowship.

REFERENCES

[1] S. Okhonin, M. Nagoga, J. Sallese, and P. Fazan, "A SOI capacitor-less 1T-DRAM concept," in *IEEE International SOI Conference*, 2001, pp. 153 –154.

[2] K. Volz, A. Beyer, W. Witte, J. Ohlmann, I. Nemeth, B. Kunert, and W. Stolz, "GaP-nucleation on exact Si (0 0 1) substrates for III/V device integration," *Journal of Crystal Growth*, vol. 315, no. 1, pp. 37 – 47, 2011.

[3] T. J. Grassman, J. A. Carlin, B. Galiana, L.-M. Yang, F. Yang, M. J. Mills, and S. A. Ringel, "Nucleation-related defect-free GaP/Si(100) heteroepitaxy via metal-organic chemical vapor deposition," *Applied Physics Letters*, vol. 102, no. 14, p. 142102, 2013.

[4] T. J. Grassman, M. R. Brenner, S. Rajagopalan, R. Unocic, R. Dehoff, M. Mills, H. Fraser, and S. A. Ringel, "Control and elimination of nucleation-related defects in GaP/Si(001) heteroepitaxy," *Applied Physics Letters*, vol. 94, no. 23, p. 232106, 2009.

[5] A. Pal, A. Nainani, Z. Ye, X. Bao, E. Sanchez, and K. Saraswat, "Electrical characterization of GaP-Silicon interface for memory and transistor applications," *IEEE Transactions on Electron Devices,*, vol. 60, no. 7, pp. 2238–2245, 2013.

[6] I. Sakata and H. Kawanami, "Band discontinuities in gallium phosphide/crystalline silicon heterojunctions studied by internal photoemission," *Applied Physics Express*, vol. 1, no. 9, p. 091201, 2008.

[7] J.-S. Kim, S.-W. Chung, T.-S. Jang, S.-H. Lee, D.-H. Son, S.-J. Chung, S.-M. Hwang, S. Banna, S. Bhardwaj, M. Gupta, J. Kwon, D. Kim, G. Popov, V. Gopinath, M. Van Buskirk, S.-H. Cho, J.-S. Roh, S.-J. Hong, and S.-W. Park, "Vertical double gate Z-RAM technology with remarkable low voltage operation for DRAM application," in *Symposium on VLSI Technology (VLSIT)*, 2010, pp. 163–164.

[8] S. Okhonin, M. Nagoga, E. Carman, R. Beffa, and E. Faraoni, "New generation of Z-RAM," in *IEEE International Electron Devices Meeting (IEDM)*, 2007, pp. 925–928.

[9] M. H. Cho and T.-J. K. Liu, "Variation study and implications for BJT-based thin-body capacitorless DRAM," *IEEE Electron Device Letters*, vol. 33, no. 3, pp. 312–314, 2012.