Quantum Confinement Point of View for Mobility and Stress Responses on (100) and (110) Single-Gate and Double-Gate nMOSFETs

Anson C-C Wang, Edward Chen, Tzer-Min Shen, Jeff Wu, and Carlos H. Diaz
TCAD Division, Taiwan Semiconductor Manufacturing Company (TSMC)
No. 168, Park Ave. 2, Hsinchu Science Park, Hsinchu County, Taiwan
E-mail: chenjhm@tsmc.com

***Abstract*—Impact of quantum confinement on electron mobility and its stress responses for (100) and (110)-orientated single-gate (SG) and double-gate (DG) nMOSFETs is studied. Unstrained electron mobility in (110) DG nMOSFETs is found to be significantly higher than that of (110) SG devices. This paper discusses another physical explanation to the experimentally observed higher electron mobility in (110) FinFET sidewall channels as compared to that observed in planar (110) devices. It is also found that the electron mobility increases faster under uniaxial tensile stress for (110) devices than for (100) ones. The higher mobility in (110) DG devices is attributed to the lighter confinement effective mass of Δ4 valleys and the non-parabolicity of Δ2 valleys along the <110> directions. With high enough tensile strain, DG nMOSFETs with (110) surface orientation are expected to outperform these on (100).**

Keywords-quantum confinement, mobility, stress response, single-gate and double-gate nMOSFETs

I. Introuduction

Multi-gate transistors have entered the scaling path recently due to their better electrostatic control than that of planar bulk FETs [1]. The higher electron mobility is experimentally observed in (110) FinFET sidewall channels as compared to the expectation based on (110) planar data [2], [3]. The observation has been studied using full band structure calculation with triangular well approximation and attributed to the non-parabolicity of Δ2 valleys [3]. However, the use of triangular well approximation leads to overestimation of the electric filed and sub-band energy splitting in FinFETs, and overlook of the key difference of quantum confinement between planar FETs and FinFETs. In this paper, impact of quantum confinement on electron mobility and its stress responses for (100) and (110)-orientated single-gate (SG) and double-gate (DG) nMOSFETs is comprehensively studied. The sub-band energy and inversion charge distribution in quantum wells clearly explains the underlying physics for both subjects.

II. Simulation Methodology

The multi-sub-band Monte Carlo (MSMC) method accounting for silicon's six degenerate Δ valleys is adopted in this work [4]. In addition to the standard parameters of effective mass approximation (EMA) [5], the Δ2 confinement effective mass along the [110] direction is modified from its nominal $0.19m_0$ value to $0.23m_0$ in order to capture the non-parabolicity of Δ2 sub-band [6]. The first two eigen-energies are able to achieve good agreement with the linear combination of bulk band (LCBB) quantization model [7]. The important scattering mechanisms including coulomb, phonon, and surface roughness scattering are taken into account in the simulations [5]. Most of phonon scattering parameters are taken from the "standard" parameter set in Ref. [8] except D_{ac} value increased from 9 eV to 13 eV to have a better fitting of electron inversion mobility [9]. A Gaussian spectrum of the surface roughness is assumed in the simulation. The correlation length of surface roughness (Λ_{sr}) is fixed at 10 Å and the r.m.s. value of surface roughness (Δ_{sr}) is taken as the fitting parameter for the different wafer orientations. The scattering parameters are listed in TABLE I. For the strain effect, the analytical expressions derived by Ungersboeck *et al.* [10] are used to calculate the effective mass change and valley splitting under mechanical stress. Nevertheless, these considerations are not sufficient to reproduce experiments of the uniaxial stress response on (100) SG nMOSFETs [11]. To obtain good agreement with the experimental result, surface roughness scattering reduction with increasing tensile strain is assumed [5], [12]. This assumption has been substantiated by recent *ab initio* calculations, which revealed that strain reduces Δ4 state occupancy, thereby lessens surface roughness scattering in the channel [13].

TABLE I. Scattering parameters used in MSMC simulations for electron inversion layer.

Phonon:	
Acoustic D_{ac} [eV]	13
Optical D_{op}	from [8]
Optical phonon energy	from [8]
Surface roughness (Gaussian spectrum):	
Δ_{sr} (Å)	6.2 (100), 6.6 (110)
Λ_{sr} (Å)	10

III. Result and Discussion

Fig. 1 shows simulated electron mobility vs. effective field on (100) and (110) SG nMOSFETs with various doping concentration. The effective field is defined by

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$$E_{eff} = (q/\varepsilon_{Si})(N_{dep} + \eta N_{inv}) \tag{1}$$

where q is the elementary charge, ε_{Si} is the permittivity of Si, and N_{dep} and N_{inv} are the depletion and inversion charge concentration per unit area. η is taken as 1/2 and 1/3 for (100) and (110) SG nMOSFETs, respectively, to align with the universal relationship [14], [15].

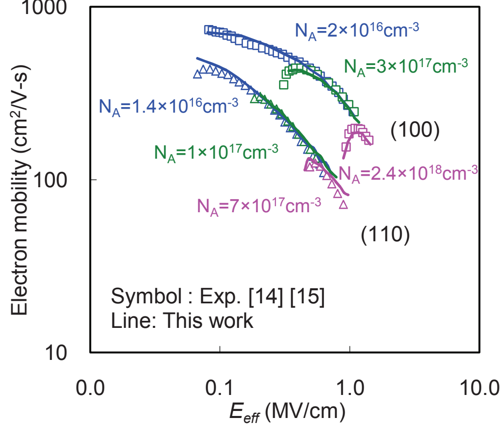

Fig.1 Simulated (100) and (110) SG electron mobility vs. effective electric field with various doping concentration compared with experiments [14], [15].

The correlation length r.m.s. value Δ_{sr} = 6.2 Å and 6.6 Å are used for (100) and (110) cases, respectively. This indicates (110) suffers stronger surface roughness scattering than that on (100) [16]. Fig. 2 shows the simulated electron density vs. depth from Si/SiO_2 interface for $N_{inv} \approx 10^{13}$ cm^{-2}.

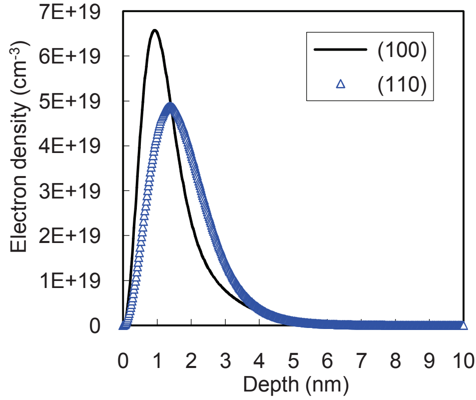

Fig.2 Simulated (100) and (110) electron density vs. depth from Si/SiO_2 interface when $N_{inv} \approx 10^{13}$ cm^{-2}.

The deeper carrier centroid of (110) SG compared to that of (100) SG can be explained by the sub-band energies in Fig. 3. The ground state of (100) SG is Δ2 which has a deeper energy level than that of the ground state for (110) SG, which is Δ4. This is because that (100) has a larger confinement effective mass of $0.916m_0$, than that of (110), which is $0.315m_0$. Although the ground state of (100) is below Fermi energy while that of (110) is above, both ground states have similar population rate since the ground state of (110), Δ4, has twice the degeneracy of the ground state of (100), Δ2. The large transport effective mass difference between Δ2, $0.19m_0$, and Δ4, $0.553m_0$, explains the mobility ratio of ~2 between (100) and (110) SG nMOSFETs.

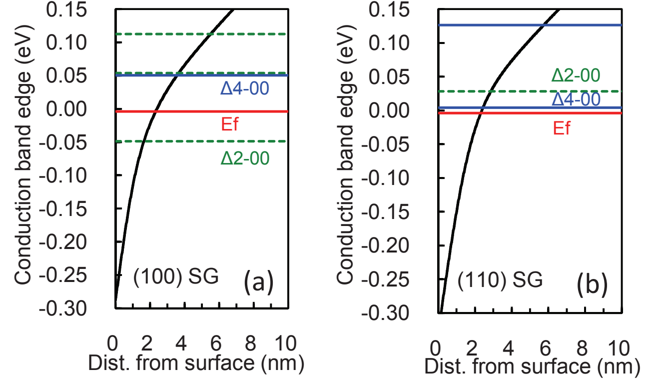

Fig.3 Sub-band distributions for **(a)** (100), and **(b)** (110) SG nMOSFETs when $N_{inv} \approx 10^{13}$ cm^{-2}.

The same parameters as SG with the channel doping concentration of 3×10^{17} cm^{-3} are used for DG simulation. Fig. 4(a) and Fig. 4(b) show the simulated (100) and (110) DG electron mobility vs. N_{inv} with Si thickness (T_{Si}) of 20 nm, respectively.

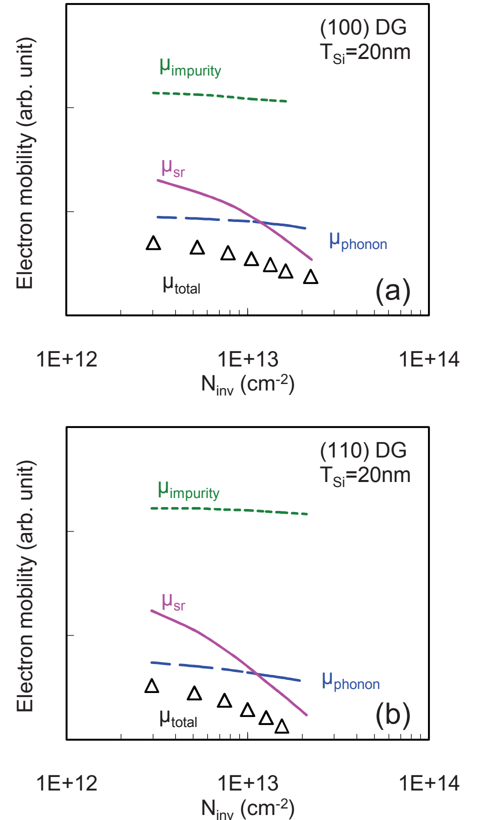

Fig.4 Electron mobility vs. N_{inv} for **(a)** (100), and **(b)** (110) DG nMOSFETs with T_{Si} =20 nm.

The DG mobility and charge distribution (Fig. 7) are similar to those of the SG case for both (100) and (110) with T_{Si} = 20 nm. The same simulations for (100) and (110) DG with T_{Si} = 6 nm are shown in Fig. 5(a) and Fig. 5(b), respectively.

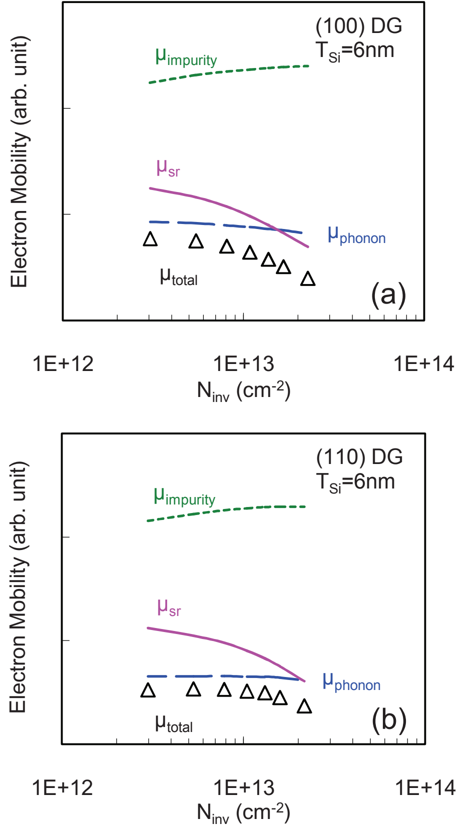

Fig.5 Electron mobility vs. N_{inv} for **(a)** (100), and **(b)** (110) DG nMOSFETs with T_{Si} = 6 nm.

A clear increase of electron mobility of the (110) DG can be seen while T_{Si} decreases to 6 nm. When $N_{inv} \approx 10^{13}$ cm^{-2}, DG $\mu_{(110)}$ increased by ~1.7× from that of the (110) SG, while the mobility for (100) DG only increased by ~1.2×. Instead of the expected ~2× lower mobility when using (110) surface channel vs. (100), in thin body DG devices such as FinFETs, the (110) surface channel results in much less mobility loss vs. (100) SG. To explain this finding, the corresponding sub-band energy levels for $N_{inv} \approx 10^{13}$ cm^{-2} are plotted in Fig. 6(a) and Fig. 6(b). The dominant Δ2 valleys are still in the triangular well for the (100) DG, while Δ4 valleys for the (110) DG are pushed out of the triangular well due to the light confinement effective mass. Consequently, the inversion charge distribution of the (110) DG is pushed further away from Si/SiO_2 interfaces as shown in Fig. 7(b). Therefore, the surface roughness scattering is greatly reduced in this case. In addition, the Δ2 non-parabolicity effect also increases the Δ2 occupancy for the (110) DG as compared to (110) SG as shown in Fig. 9(b), and contributes the mobility enhancement.

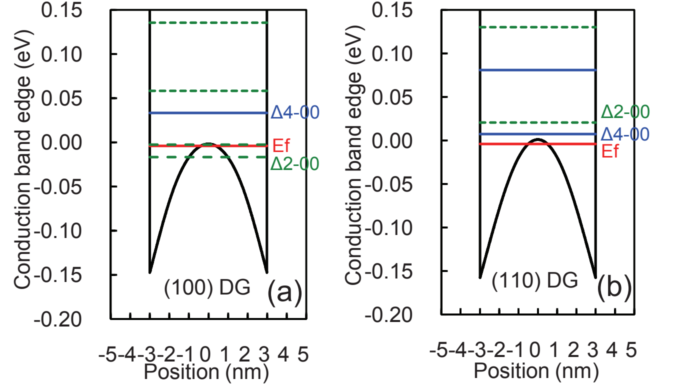

Fig.6 Sub-band distributions for **(a)** (100), and **(b)** (110) DG nMOSFETs with T_{Si} = 6 nm when $N_{inv} \approx 10^{13}$ cm^{-2}.

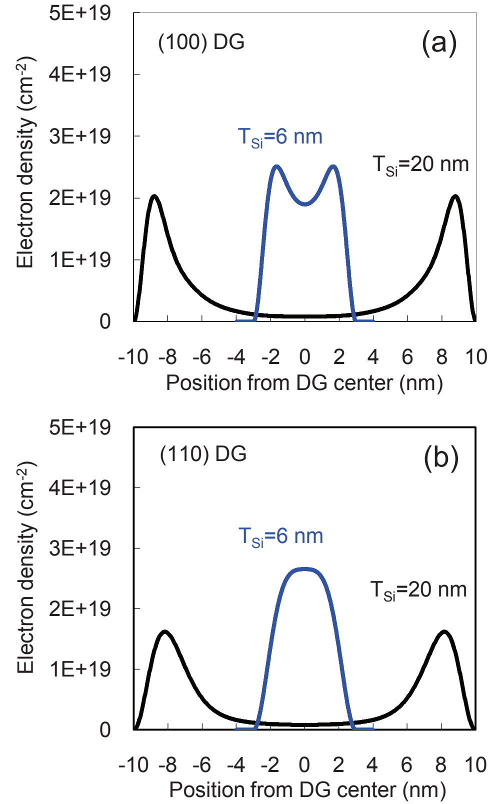

Fig.7 The charge distributions for **(a)** (100), and **(b)** (110) DG nMOSFETs with T_{Si} = 20 (black line) and 6 (blue line) nm. All charge distributions are plotted for $N_{inv} \approx 10^{13}$ cm^{-2}.

Finally, electron mobility vs. uniaxial longitudinal stress extracted when $N_{inv} \approx 10^{13}$cm^{-2} for (100) and (110) SG and DG nMOSFETs are shown in Fig. 8. The corresponding carrier transfer with the stress is shown in Fig. 9. From the figures, SG and DG show the similar behavior for both (100) and (110) cases, which means they have the similar stress responses if normalized to their individual unstrained mobility. Although (100) SG has superior mobility than (110) SG in the applicable stress range, DG nMOSFETs with (110) channel surface are

expected to outperform these on (100) orientation under high enough tensile strain.

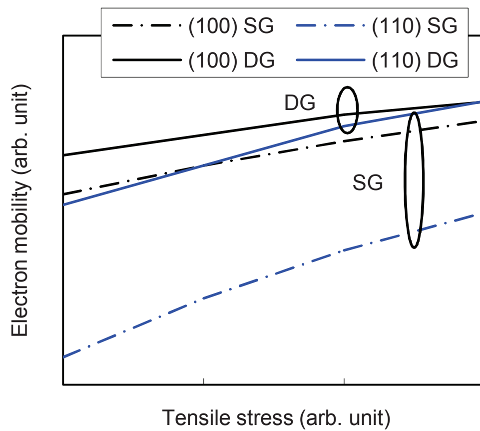

Fig.8 The electron mobility vs. the uniaxial stress (arb. unit) along the longitudinal direction for (100) and (110) SG and DG (T_{Si} = 6nm) nMOSFETs when $N_{inv} \approx 10^{13}$ cm^{-2}.

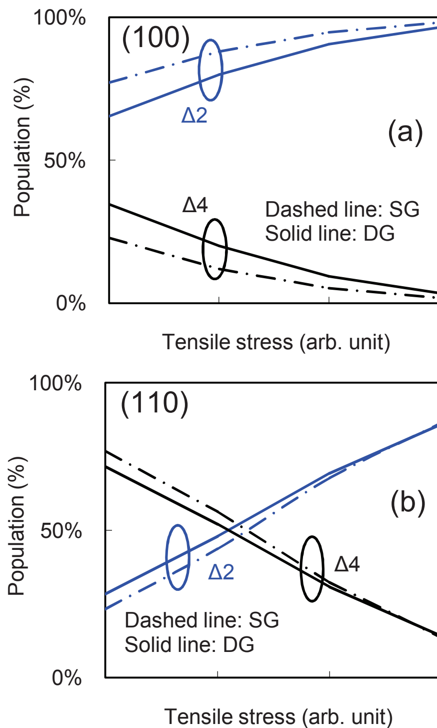

Fig.9 The carrier population rate vs. longitudinal tensile stress for **(a)** (100), and **(b)** (110) SG and DG (T_{Si} = 6nm) nMOSFETs when $N_{inv} \approx 10^{13}$ cm^{-2}.

IV. CONCLUTION

Impact of quantum confinement on electron mobility and its stress responses for (100) and (110)-orientated SG and DG nMOSFETs is studied in the paper. The higher mobility in (110) DG devices is attributed to the light confinement effective mass of Δ4 valleys and the non-parabolicity of Δ2 valleys along the <110> directions. Under high enough tensile strain, DG nMOSFETs with (110) channel surface are expected to outperform these on (100) orientation.

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