Impact of Back-end-of-line on Thermal Impedance in SiGe HBTs

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***Abstract*—In this paper, self-heating of a state-of-the-art SiGe:C BiCMOS Heterojunction Bipolar Transistor (HBT) is studied by means of 3D thermal TCAD simulations. Steady-state, large signal and small signal transient simulations are performed on different device structures to investigate the impact of back-end layers on thermal impedance (Z_{TH}). In addition, the simulation results are verified by DC and low frequency measurements and found to be in excellent agreement.**

***Index Terms*—Heterojunction Bipolar Transistors (HBTs), Numerical simulation, Thermal impedance, Electrothermal effects, Semiconductor device measurements**

I. Introduction

It is well known that the state-of-the-art HBTs perform well in microwave frequency nonlinear circuits such as high power amplifiers and oscillators. High speed applications like car radar modules (24.1 and 77 GHz), wireless LAN (40/60 GHz) system [1] as well as 100 Gb/s data communications [2] require consequent improvement of device and technology performances. Continuous improvements of SiGe HBT technology come to be suitable for this kind of applications due to their speed and integration aspects. Higher device performance is mainly achieved with downscaling of device dimensions and by improving the device architecture. But the increase in power density in the transistor results in high levels of self-heating, which changes the DC bias and low frequency behavior of the device [3].

Moreover the trench isolation technology reduces parasitic components and provides high-frequency performance [4]. But the low thermal conductivity of the oxide used in trench wall affects the heat dissipation [5]. Thermal effects are exacerbated in small area devices with trench isolated structures due to heat confinement towards the Silicon substrate. Therefore a not-negligible heat flow will appear upwards through the back-end-of-line. The influence of the back-end process layers and metallic interconnects on Z_{TH} needs to be evaluated for advanced high-speed and RF HBTs in order to model accurately the self-heating effect.

In this work, 3D simulation results supported by measurement data are employed to quantify the impact of backend layout and technology on Z_{TH} of state-of-the-art SiGe HBTs. The paper is organized as follows. In section II, device structure and simulations strategy is described. DC and low frequency measurements are presented in section III. Finally, the simulation results are compared to measurements as given in section IV.

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II. Thermal Simulations Strategy

The bipolar test structure analyzed in this work was fabricated by STMicroelectronics with SiGe BiCMOS9MW technology [6]. The key figures of this technology are: breakdown voltages, BV_{CEO} = 1.6 V, BV_{CBO} = 5.5 V, transit frequency f_T = 230 GHz and maximum oscillation frequency f_{max} = 290 GHz. A TEM picture of the internal transistor with drawn emitter window L_E x W_E = 10 x 0.27 µm^2 is shown in Fig. 1a [6].

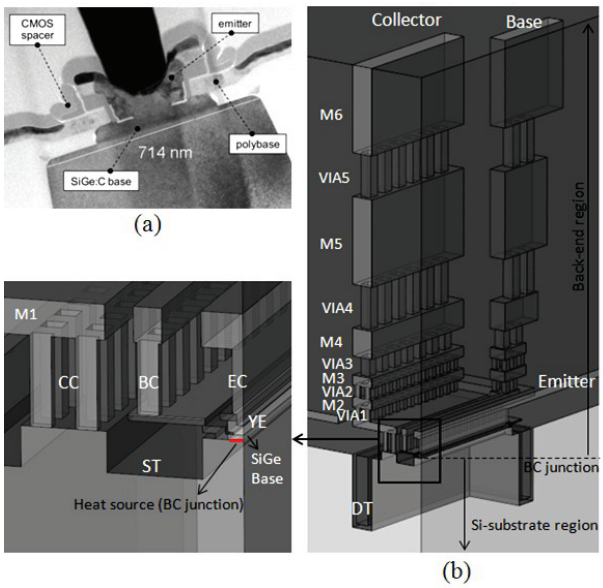

Fig. 1: (a) TEM picture of BiCMOS9MW SiGe HBT with drawn emitter window L_E x W_E = 10 x 0.27 µm^2; (b) a complete structure of the same technology built in "Sentaurus Structure Editor"; M – metal layer, VIA – metal VIA layer, ST – shallow trench, DT – deep trench, YE – Y-shaped emitter, EC, BC and CC – emitter, base and collector contacts respectively.

The simulations are based on merely thermal finite-element-method (FEM) performed by Sentaurus device simulator version E-2010.12 [7]. The structure of a CBEBC transistor with drawn emitter window L_E x W_E = 10 x 0.27 µm^2 is built on a semi-infinite Si-cube. Due to the inherent

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symmetry of the transistor, only one quarter of a structure is simulated and the rest portions are virtually recreated by imposing adiabatic conditions over the symmetry planes. In a first attempt, the transistor structure is simplified by neglecting the back-end part. We have considered only the "lower part" (L) starting from base-collector (BC) junction down to the Si-substrate region. This region also includes trench isolation walls: (i) the SiO_2–Poly Silicon–SiO_2 deep trench isolation (DTI) and (ii) SiO_2 shallow trench isolation (STI) (see Fig. 1b, lower part). Within the simulator environment, the heat source is represented as a rectangular parallelepiped (at the BC junction) with length and width equal to L_E and W_E respectively. The vertical thickness is the same as the base-collector depletion region where the power dissipation takes place. In order to investigate the influence of the back-end structure on device self-heating, different process layers are successively added. These are SiGe–base, poly Si–base, Y–shaped Si emitter, emitter poly Si, metal (copper) contacts for emitter, base and collector and finally back–end metal layers. These back–end metal layers consist of five metallic vias and six metal layers. The surrounding region of metal layers is filled with SiO_2. A complete device structure including all layers is shown in Fig. 1b. The internal transistor with emitter, base and collector contacts is shown in the enlarged image.

We have considered the material properties and physical parameters like thermal conductivity κ and lattice heat capacity C_L as defined in Sentaurus device simulator. In this simulation, we only investigate the thermal phenomena inside the device i.e. there is no electrical dependency. The temperature distributions due to device self-heating are evaluated by solving lattice heat flow equations.

The transistor is fabricated on a Si – substrate and most of the region in the back-end part is filled with silicon dioxide. Hence, except the heat flow through the metal, major thermal diffusion takes place towards the wafer backside. The introduction of deep trenches restricts the lateral heat flux flow and directs it vertically. Due to the poor thermal conductivity of the trench wall, the heat flow from the heat source is mostly confined within the trench-enclosed region and thereby increases the temperature of the active device. Thus, the trench-enclosed silicon substrate plays the major role in thermal phenomena. On the other hand, the κ of silicon varies significantly with temperature compared to other materials. Therefore, we have considered the temperature dependence of κ for silicon. We assume constant value of κ for poly Si, Cobalt, SiO_2 and Copper. The temperature dependence of κ for silicon is given by the following expression:

$$\kappa(T) = \frac{1}{\kappa_a + \kappa_b T + \kappa_c T^2} \qquad (1)$$

Here κ_a, κ_b and κ_c are the temperature coefficients and the values are given as follows: $\kappa_a = 0.03$ cmKW^{-1}, $\kappa_b = 1.56 \times 10^{-3}$ cmW^{-1} and $\kappa_c = 1.65 \times 10^{-6}$ cmK^{-1}W^{-1}. The κ at 300 K of all materials employed for the simulations are reported in the Table I. Various pre-processing steps were accomplished to obtain a fast and accurate simulation. Optimizations of mesh refinement have been carried out to overcome meshing issues resulting from the presence of extremely thin layers and interfaces between different materials The applied power density (P_{diss}) at the heat source has a significant impact on Thermal resistance (R_{TH}) due to the temperature dependent of κ. The P_{diss} at the BC junction for a particular bias condition is calculated from measurements and the data is fed in the simulator.

TABLE I
THERMAL CONDUCTIVITIE AND LATTICE HEAT CAPACITY

material	κ at 300 K [W/K cm]	C_L at 300 K [J/K cm^3]
Silicon	1.54	1.63
Germanium	0.60	1.67
Silicon dioxide	0.014	1.67
Emitter polysilicon	1.50	1.63
Trench polysilicon	1.50	1.63
Base polysilicon	1.50	1.63
cobalt	1.00	3.74
copper	3.85	3.42
Silicon germanium	1.54 [Si], 0.60 [Ge]	1.63 [Si], 1.67 [Ge]
	Analytical law accounting for the mole fraction [7]	

Steady-state, large signal and sinusoidal transient simulations are performed from 100 kHz to 100 MHz. The magnitude and phase of Z_{TH}s as a function of frequency is extracted with the methodology described in [8]. The simulations are performed using a PC equipped with a 3.46 GHz 12-core processor and a 24 GB RAM. A typical mesh accounting for all the geometrical details of a "complete structure" comprises about 2 x 10^6 3D elements. A steady-state solution is evaluated in about 10 min where a sinusoidal transient simulation at 10 MHz frequency with 5 cycles takes about 265 min.

III. LOW FREQUENCY MEASUREMENTS

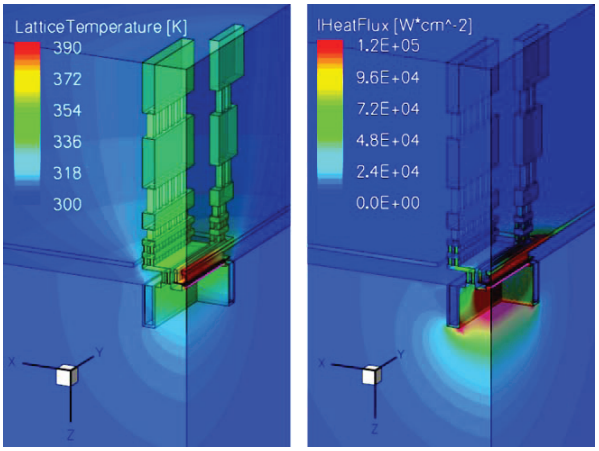
DC measurements are carried out at different ambient temperatures (T_{amb}) and R_{TH} of the device is extracted with the methodology described in [9]. *S*-parameter measurements were performed in the frequency range from 100 kHz to 3 GHz at 300K T_{amb} using the Anritsu-MS2026B vector network analyzer. The applied DC biases are base-emitter voltage V_{BE} = 0.95V, collector-emitter voltage V_{CE} = 1.5V and the RF power = -30 dBm. This bias condition is close to the peak f_T where self-heating is pronounced. Following the approach presented in our previous work [10], Z_{TH} has been extracted in the region around thermal cut-off frequency.

IV. RESULTS AND DISCUSSION

A steady state thermal simulation result is shown in Fig. 2 where the lattice temperature $T_{lattice}$ (Fig. 2a) and the heat flux F_{heat} (Fig. 2b) distribution inside the complete structure are given when applying a DC power of 40 mW/μm^2 at the heat source. It can be noticed that the heat is concentrated mainly in the active region around the BC junction. The low κ of STI and DTI results in the heat confinement in the trench enclosed region giving rise to a higher thermal gradient. Moreover, a significant heat flow can be seen through metal interconnects. The simulations are performed on six different structures, identified with the symbols as follows: L: lower part (BC junction to Si-substrate), YE: L + SiGe base and Y shaped

emitter, E: YE + emitter contact, EBC: E + base and collector contacts, 2M: all up to 2nd metal layer and 6M: all up to 6th metal layer.

Steady-state simulations are performed for all structures by applying 40 mW/μm^2 power density. R_{TH}s of all these structure are plotted in Fig. 3 and compared to measurements. The structure "L" is taken as the reference. Significant decreases in R_{TH}s are found when different back-end layers are added. For the complete structure 6M, R_{TH} decreases about 10% due to the heat flow through metal layers. A good agreement is achieved between the 6M structure simulations and measurement results.



(a) (b)

Fig 2: (a) $T_{lattice}$ and (b) F_{heat} distribution inside the transistor at steady state condition with applied power density = 40 mW/μm^2: ¼ of the complete structure with CBEBC configuration; the dimension of the heat source (L_ExW_E = 10x0.27μm^2).

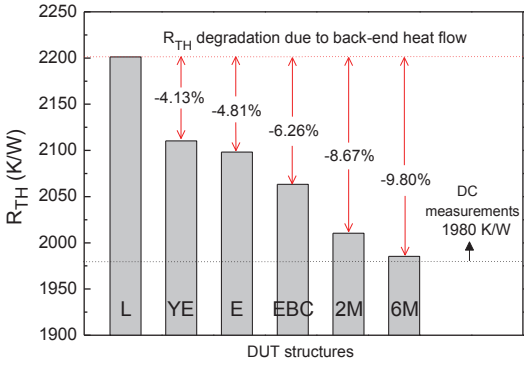


Fig 3: R_{TH}s of different structures (L, YE, E, EBC, 2M and 6M): extracted from TCAD simulations and compared to measurements.

Large signal transient simulations are performed for all structures applying a power pulse with a width = 5μs and power density = 40 mW/μm^2. Initially the simulation environment is set to 300K. The junction temperature variations (ΔT_J) for all structures are compared in Fig. 4. In order to investigate the impact of back-end in transient domain, the key parameter thermal capacitance (C_{TH}) needs to be evaluated. ΔT_J is modeled using an electro-thermal network. When a transient power is applied to the device, theoretically an infinite number of thermal time constants are necessary to represent the thermal response of the material due to the distributed nature. It was shown in previous work [11], that transient self-heating could not be properly modeled with a conventional single pole (R_{TH}-C_{TH}) network; therefore a distributed network is needed. Using the recursive network, as presented in [11], the thermal capacitance parameter C is extracted. The parameter C (C_{TH} in the plot) of all these structures are plotted in Fig. 5 and compared to measurements. Significant increases in C_{TH}s are found when different back-end layers are added. For the complete structure 6M, the C_{TH} increases about 53% with respect to structure L. A good agreement is achieved between the complete structure simulations and measurement results.

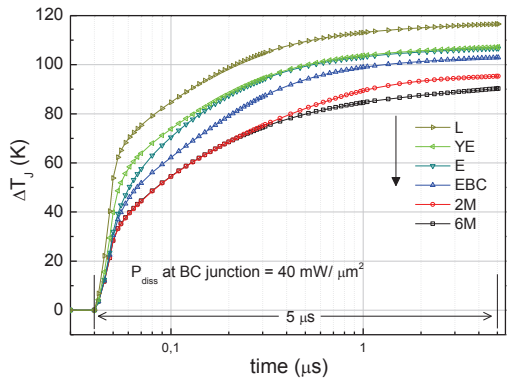


Fig 4: The transient junction temperatures for different device structures: applied pulse = 40 mW/μm^2 power density and 5μs width; the dimension of the heat source L_E x W_E = 9.88 x 0.15 μm^2.

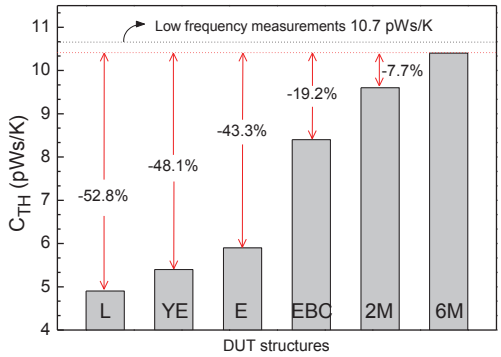


Fig 5: C_{TH}s of different structures (L, YE, E, EBC, 2M and 6M): extracted from TCAD simulations and compared to measurements.

In Fig. 6 and 7, the magnitude and phase of Z_{TH}s are compared between measurements and numerical simulations in the frequency range 100 kHz – 100 MHz. Investigating the magnitude, it can be seen that the slope of the roll-off changes when back-end process layers are added e.g. for the structure L, the slope is nearly -5 dB/dec which increases to nearly -9 dB/dec for the 6M structure. This "complete structure" simulation result is in good agreement with measurement results where a -10 dB/dec slope is found.

At very low frequency the Z_{TH} is mainly defined by the R_{TH} which is inversely proportional to κ. The copper interconnects are highly conductive (κ = 3.85 W/Kcm at 300°K) but on the other hand, the surrounding region is filled with very low conductive SiO_2 (κ = 0.014 W/Kcm at 300°K) and the dimensions of the vias are very small. Therefore, the heat flow through the copper results only in a small decrease of R_{TH}.

As frequency increases, the decay of the Z_{TH} slope is due to the C_{TH}. The C_{TH} is a function of the temperature rise associated with a given quantity of applied energy. It is also a function of material properties: the product of material's specific heat (C_p), density (ρ) and volume. The C_p of Silicon, SiO_2 and Copper is 0.703 J/gK, 1.0 J/gK and 0.385 J/gK respectively. The major regions of back-end layers are fabricated with materials like SiO_2 which has a larger C_p than Silicon. Thus, the addition of back-end regions exhibits a reasonable contribution to C_{TH}. Furthermore, the device upper surface cannot absorb permanent heat flux since this surface is adiabatic and has less influence at steady state, while the back-end region can store some energy during transient state. From this analysis, we can deduce that it affects more on C_{TH} and, therefore, Z_{TH} in the frequency domain.

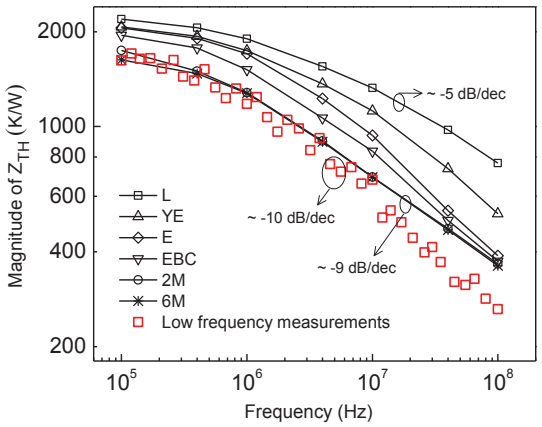


Fig 6: Variations of the magnitude of Z_{TH} when different back-end layers are added: comparison between measurements and simulations.

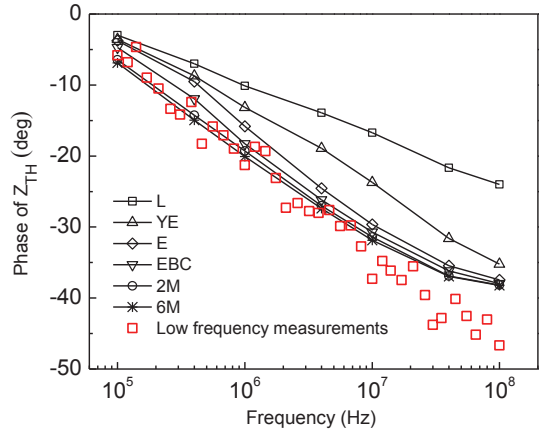


Fig 7: Variations of the phase of Z_{TH} when different back-end layers are added: comparison between measurements and simulations.

V. Conclusions

3D thermal TCAD simulations are performed on a state-of-the-art SiGe:C BiCMOS HBT. The impact of the back-end layers on thermal parameters (R_{TH} and C_{TH}) and also on the Z_{TH} in the frequency domain is evaluated. The simulation results are validated through DC and low frequency measurements. It has been found that the heat flow through the metal contacts causes about 10% decrease in R_{TH} and nearly 53% increase in C_{TH} due to the back-end structure. Therefore, the extraction methodology of thermal parameters should include the impact of the back-end structure in order to provide accurate transistor models.

Acknowledgment

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References

[1] M. Schwerd, M. Seck, T. Huttner, T. Bottner, S. Drexl, B. Hasler, A. Mitchell, H. Heineder, H. Korner, V. Kubrak, M. Schrenk, and R. Lachner, "A manufacturable 0.35 /spl mu/m 150 GHz f/sub T/ SiGe:C bipolar RF technology," in 2003 Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems, 2003. Digest of Papers, 2003, pp. 10–13.

[2] M. Moller, "High-speed electronic circuits for 100 Gb/s transport networks," in Optical Fiber Communication (OFC), collocated National Fiber Optic Engineers Conference, 2010 Conference on (OFC/NFOEC), 2010, pp. 1–3.

[3] O. Sevimli, A. E. Parker, A. P. Fattorini, and S. J. Mahon, "Measurement and Modeling of Thermal Behavior in InGaP/GaAs HBTs," Ieee Trans. Electron Devices, vol. 60, no. 5, pp. 1632–1639, 2013.

[4] D. L. Harame, J. H. Comfort, J. D. Cressler, E. F. Crabbe, J. Y.-C. Sun, B. S. Meyerson, and T. Tice, "Si/SiGe epitaxial-base transistors. II. Process integration and analog applications," Ieee Trans. Electron Devices, vol. 42, no. 3, pp. 469–482, 1995.

[5] D. J. Walkey, T. J. Smy, C. Reimer, M. Schröter, H. Tran, and David Marchesan, "Modeling thermal resistance in trench-isolated bipolar technologies including trench heat flow," Solid-State Electron., vol. 46, no. 1, pp. 7–17, Jan. 2002.

[6] A. Chantre, P. Chevalier, T. Lacave, G. Avenier, M. Buczko, Y. Campidelli, L. Depoyan, L. Berthier, and C. Gacquière, "Pushing conventional SiGe HBT technology towards Dotfive terahertz," in Microwave Integrated Circuits Conference (EuMIC), 2010 European, 2010, pp. 21–24.

[7] Synopsys Inc. Mountain View, "TCAD Sentaurus User Guide E-2010.12, 2010." .

[8] A. K. Sahoo, S. Fregonese, M. Weis, N. Malbert, and T. Zimmer, "A Scalable Electrothermal Model for Transient Self-Heating Effects in Trench-Isolated SiGe HBTs," Ieee Trans. Electron Devices, vol. 59, no. 10, pp. 2619–2625, 2012.

[9] M. Pfost, V. Kubrak, and P. Brenner, "A practical method to extract the thermal resistance for heterojunction bipolar transistors," in 33rd Conference on European Solid-State Device Research, 2003. ESSDERC '03, 2003, pp. 335–338.

[10] A. K. Sahoo, S. Fregonese, T. Zimmer, and N. Malbert, "Thermal Impedance Modeling of Si-Ge HBTs From Low-Frequency Small-Signal Measurements," Ieee Electron Device Lett., vol. 32, no. 2, pp. 119–121, 2011.

[11] A. K. Sahoo, M. Weiß, S. Fregonese, N. Malbert, and T. Zimmer, "Transient electro-thermal characterization of Si–Ge heterojunction bipolar transistors," Solid-State Electron., vol. 74, pp. 77–84, Aug. 2012.