Performance Advantage and Energy Saving of Triangular-Shaped FinFETs

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Abstract—**Detailed comparisons of FinFETs with triangular and rectangular fins were performed using numerical simulations. Although, with the same leakage current (I_{off}), the on current (I_{dsat}) of the triangular fin is less than that of the rectangular one, the 3-stage ring oscillator (RO) with triangular fins runs faster than the one with rectangular fins and consumes less energy due to better short channel control and smaller parasitic capacitance. In addition, with the triangular shape, the two side-channel surfaces are no longer (110) and benefit from reduced negative bias temperature instability (NBTI). All these make the FinFET with a triangular fin a smart choice.**

Keywords- FinFET, Tri-Gate, Triangular Fin, Rectangular Fin, CMOS, Low Energy Device.

I. INTRODUCTION

As the CMOS technology advances to 22nm and below, the FinFET or Tri-Gate is chosen to replace conventional planar CMOS [1]. C. Auth et al. of Intel [1] revealed the TEM picture of their 22nm Tri-Gate PMOS with the fin shape close to triangle, as shown in Fig. 1, instead of rectangle as most of people are familiar with. This triangular-shaped FinFET has drawn a lot of attentions and discussions about its (dis)advantages and even feasibility. S. Maeda et al. [2] reported that, for a FinFET built on a (100) wafer with <110> channel direction, NBTI is worsened as compared with planar CMOS built on the same wafer with the same channel orientation due to higher interface trap density on (110) fin sidewall surfaces. With tilted sidewalls, i.e. triangular fin, the NBTI impact is alleviated. Recently, K. Xiu and P. Oldiges [3] reported that, with slightly tilted side walls, the electron mobility increases slightly while the hole mobility degrades.

Synopsys has issued a simulation report [4] based on Intel's triangular-shaped FinFET. Simulation results show that, with the same I_{off}, the triangular fins provide 6% and 9% less I_{dsat} of NMOS and PMOS, respectively, than the rectangular ones. However, the triangular fin has better short channel control, i.e., smaller drain-induced barrier lowering (DIBL) and sub-threshold swing (SS).

Based on the previous Synopsys report [4], this study extends the investigation on other aspects of the FinFET, including the effective drive current (I_{eff}) [5], parasitic capacitance, and delay time of 3-stage RO, to evaluate the impact of fin shape on the AC performance of FinFET in details. The SWB template and calibrated SProcess and SDevice models and parameters by Synopsys in this application note [4] were also used. Mixed-mode simulations [6] for 3-stage RO were done using a 25600-core super computer at 177 TFLOPS [7].

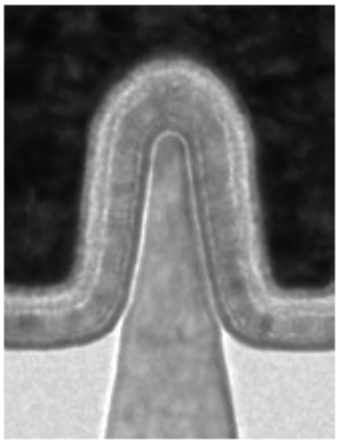

Figure 1. TEM of the FinFET with a triangular fin [1].

II. DEVICE AND MIXED-MODE RING OSCILLATOR SIMULATIONS

A. Device Structure and Electrical Characteristics

Figure 2 shows the FinFET structures explored in this work: (a) rectangular (W_{top}=15nm) and (b) triangular (W_{top}=5nm) fins. Detailed contact (backend) structure was also included as shown in Fig. 3. Table I lists the key dimensions of the FinFET used in the simulations. Figure 4 shows I_D-V_G characteristics of NMOS and PMOS. The triangular fins give 6% and 9% less I_{dsat} for NMOS and PMOS, respectively, than the rectangular fins. However, the triangular fins show better short channel control, i.e. smaller SS and DIBL, which reduces

the difference in I_{eff} (=(I_H+I_L)/2) [5], as shown in Fig. 5, and results in a direct impact on the inverter delay. Due to smaller SS, the triangular fins give higher I_L than the rectangular fins, thereby reducing the I_{eff} difference to 0.1% and 5% for NMOS and PMOS, respectively. Figure 6 is the summary of the comparison.

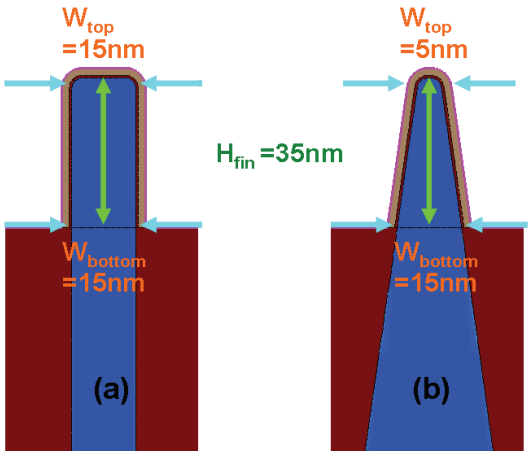

Figure 2. 2D cross-sectional views of the FinFETs with (a) rectangular fin and (b) triangular fin used in this study [4].

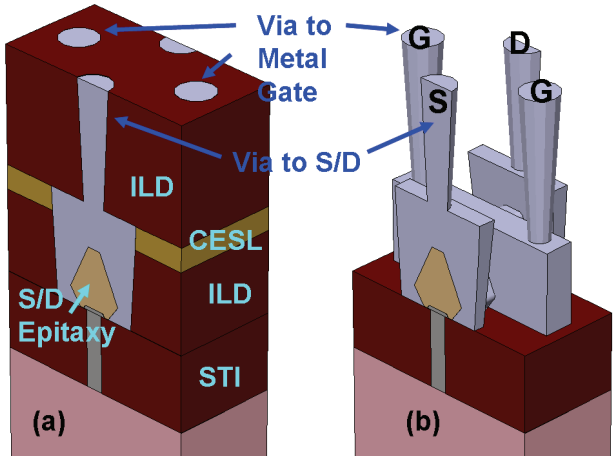

Figure 3. 3D views of the FinFET including backend process used in simulations [4]: (a) full structure and (b) removing ILD and CESL.

TABLE I. KEY DIMENSIONS OF FINFETS DEFINED IN SIMULATIONS.

Key Dimensions	
L_g	25nm
W_{top}	5nm, 15nm
W_{bottom}	15nm
H_{fin}	35nm
EOT	0.9nm
Fin Pitch	60nm

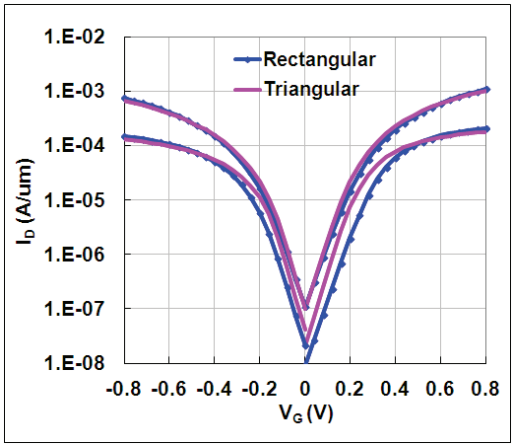

Figure 4. Predicted I_D-V_G characteristics of NMOS and PMOS with different fin structures (V_D = 0.05V and V_D = 0.8V).

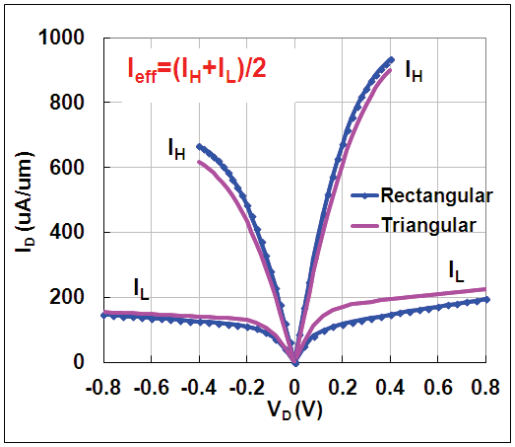

Figure 5. Predicted I_H and I_L for I_{eff} evaluation. (V_G = 0.4V and 0.8V for I_L and I_H, respectively)

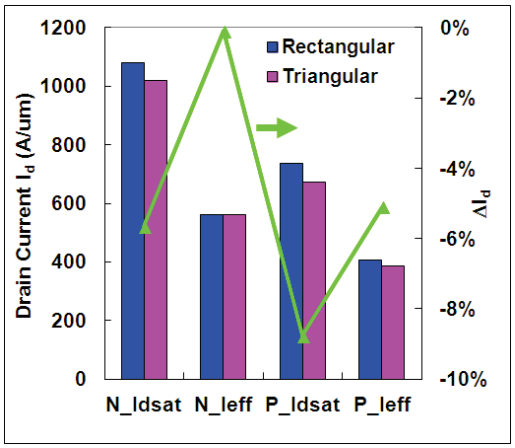

Figure 6. Drain current, I_{dsat} and I_{eff}, comparison chart for NMOS and PMOS with different fin structures.

B. Capacitance Evaluation and Ring Oscillator Simulations

The gate capacitance (C_{gg}) of the FinFET was extracted and the results are shown in Fig. 7. Due to the 3D fin shape, the triangular fins give 7% and 4% less C_{gg} of NMOS and PMOS, respectively, than the rectangular ones. Although C_{gg} does not affect the DC performance significantly [8], it has a direct impact on the AC performance as well as the speed of the circuits. Sentaurus Device mixed-mode simulations [6] were used to simulate the 3-stage RO to assess the speed. Fig. 8 shows the schematics of the inverter and 3-stage ring oscillator. Since the full device structure including contacts was used in the SDevice mixed-mode simulations [6], the impact from the parasitic capacitance can be evaluated more accurately. The simulated node outputs of the RO are given in Fig. 9 and delay time comparison is shown in Fig. 10, where the rise time t_r and fall time t_f were extracted at $V_{out}=1/2V_{DD}$ and the delay time t_d was defined as $t_d=(t_r+t_f)/2$. As can be seen, the triangular fin shows a 3% less t_d than that of the rectangular case due to smaller C_{gg}. As the supply voltage V_{DD} scales, the speed advantage of triangular fin becomes more prominent as shown in Fig. 11. For power evaluation, the switching energy (SE) is also evaluated using the definition in [8],

$$\text{Switching Energy} \quad SE = V_{DD} \cdot \int_0^T I_{DD}\, dt \qquad (1)$$

where T is a cycle time or period, and the simulation result is given in Fig. 12. Fig. 12 shows SE vs. V_{DD}. Similar to t_d, as V_{DD} scales, the SE difference between the two fins becomes larger but not as much as t_d. From these results, we conclude that the triangular fin benefits from better short channel control and smaller gate capacitance C_{gg}, resulting in smaller RO delay and switching energy. As V_{DD} scales, this advantage becomes more prominent.

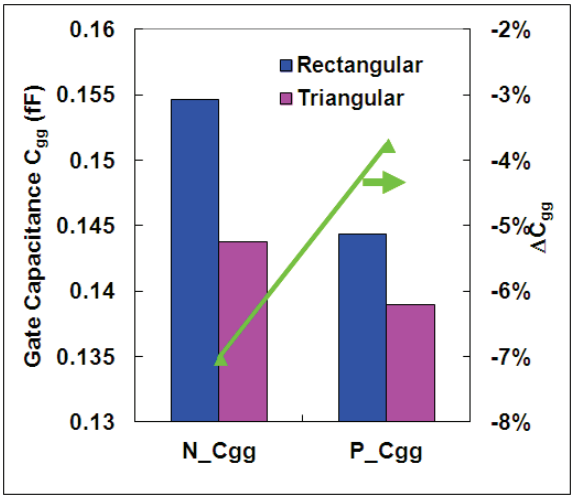

Figure 7. Gate capacitance comparison for NMOS and PMOS. The curve shows the triangular gate capacitance lowering with respect to the rectangular counterpart.

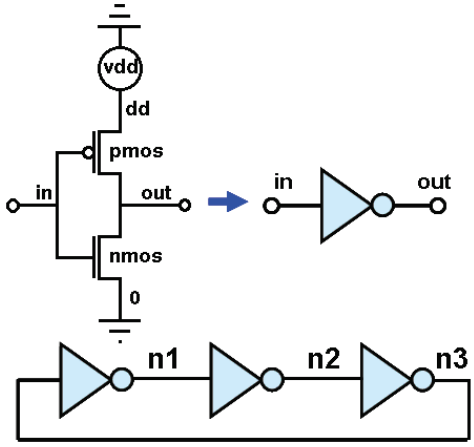

Figure 8. Schematics of the inverter and 3-stage ring oscillator used in Sentaurus Device mixed-mode simulations [6].

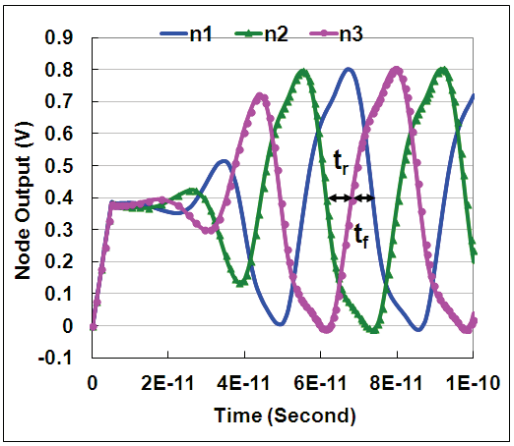

Figure 9. Simulated node outputs of 3-stage RO shown in Fig. 8.

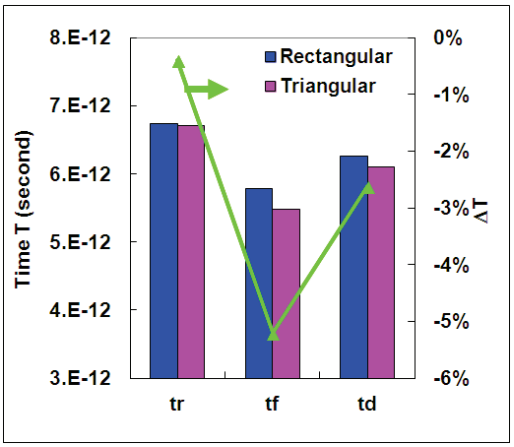

Figure 10. Predicted rise times (t_r), fall times (t_f) and average delays (t_d). The curve shows the delay improvement from the triangular fin with respect to the rectangular counterpart.

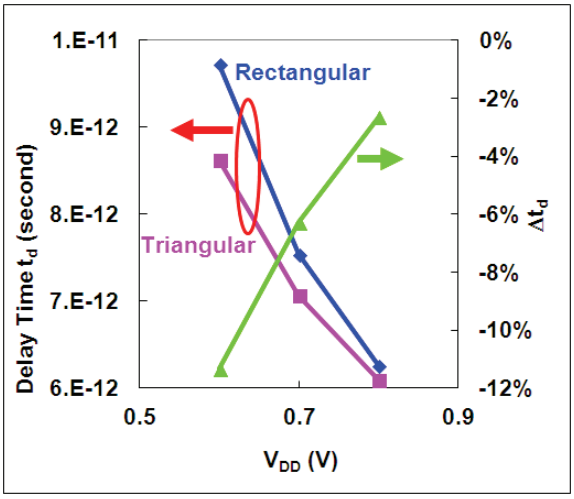

Figure 11. Predicted delay time vs. V_{DD}. The green curve with solid triangles shows the delay improvement from the triangular fin with respect to the rectangular counterpart.

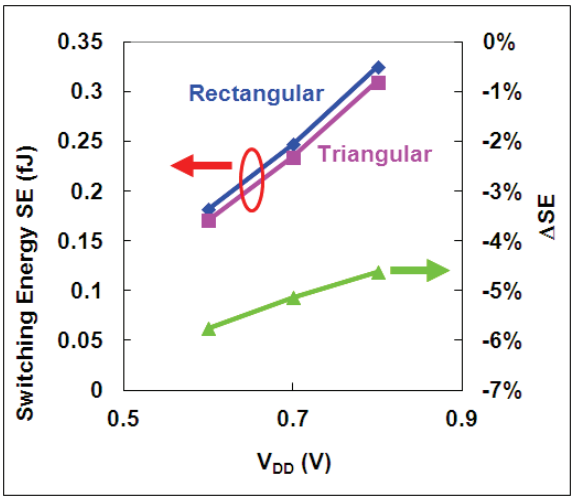

Figure 12. Predicted switching energy vs. V_{DD}. The green curve with solid triangles shows the energy reduction from the triangular fin with respect to the rectangular counterpart.

III. Conclusion

The FinFET with rectangular fin has a higher on current than triangular fin. However, the triangular fin shows better short channel control and smaller gate capacitance, resulting in smaller RO delay and switching energy consumption. As the supply voltage scales, these advantages become more prominent.

TABLE II. Advantages of the FinFET design with triangular fin as compared with rectangular one.

Advantages of Triangular Fin	
Channel length L_g	25nm
Short Channel Control	Better
Gate capacitance C_{gg} reduction	7% (NMOS) 4% (PMOS)
Delay time t_d reduction @ V_{DD}=0.8V	3%
Delay time t_d reduction @ V_{DD}=0.6V	11%
Switching energy SE reduction @ V_{DD}=0.8V	5%
Switching energy SE reduction @ V_{DD}=0.6V	6%

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