

Unified Compact Modelling Strategies for Process and Statistical Variability in 14-nm node DG FinFETs

X. Wang^{1*}, B. Cheng¹, A. R. Brown², C. Millar², C. Alexander², D. Reid², J. B. Kuang³, S. Nassif³, A. Asenov^{1,2}

¹ Device Modelling Group, School of Engineering, University of Glasgow, Oakfield Avenue, Glasgow G12 8LT, UK

² Gold Standard Simulations, Ltd., Rankine Building, Oakfield Avenue, Glasgow G12 8LT, UK

³ IBM Austin Research Lab., Burnet Road, Austin, TX 78758, USA

* Tel: +44 141 330 2964, e-mail: Xingsheng.Wang@glasgow.ac.uk

Abstract—This paper presents a principal component analysis (PCA)-based unified compact modelling strategy for process-induced and statistical variability in 14-nm double gate SOI FinFET technology. There is strong interplay between process and statistical variability in FinFET technology and failure to capture the correlations between them can lead to an inaccurate estimation of overall statistical variability with errors of up to 30%. Therefore a new unified compact modelling strategy for variability, based on comprehensive atomistic simulations within the CD corner space, is presented. First, an extended uniform compact model is built to capture CD process variation using a set of parameters, and then statistical variability is extracted using another small set of ‘statistical’ parameters. Later, the response of the extracted statistical parameters over the CD space is characterised, and finally used in a PCA method to generate the unified compact models capturing both process and statistical variability over the whole CD variation space.

Keywords—compact model; FinFET; interplay; PCA; process variability; statistical variability

I. INTRODUCTION

After the first introduction of the 3-D FinFET architecture at the 22-nm node by Intel [1], it is widely considered as a major candidate for 14-nm node mainstream technology by many technology providers. FinFETs deliver excellent electrostatics and short-channel-effect control, enabling power savings, and by tolerating low channel doping can reduce the dopant-induced variability. Still, a number of challenges are facing FinFET technology, such as deteriorated parasitics and width quantization. When new variability sources are brought to fin profile patterning such as fin-width variation due to fin-edge roughness (FER), together with traditional variability sources including random discrete dopants (RDDs), gate edge roughness (GER), and possible metal gate granularity (MGG), statistical variability is still of great concern for FinFET process and performance [2][3]. Additionally, the susceptibility of FinFETs to variations in key critical dimensions (CD), such as fin-width, complicates the variability issue [4]. It is found that unlike bulk planar technology, a strong interplay between statistical variability and systematic process-induced CD variation exists in FinFET technology [4]. Compact modelling of statistical variability can provide an advantage in evaluating the statistical effect of microscopically different transistors on circuit performance. However it is a considerable challenge for compact models to accurately replicate the transistor statistical

variability behaviour using analytical formulae [5]. The strong dependence of statistical variability on CD process variation further challenges the traditional statistical compact modelling strategies. Using a ‘principal component analysis’ technique, this paper will present the development of novel unified compact modelling strategies taking into account coherently the interplay between process-induced and statistical variability.

II. DEVICE DESCRIPTION AND SIMULATION METHODOLOGY

The variability study and compact modelling strategy development is carried out on a 14-nm node SOI double-gate FinFET which is designed and optimised using the GSS atomistic simulator Garand [6]. The FinFET process on SOI substrate is simpler than on bulk substrate, since the fin patterning is achieved by etching down to the buried oxide (BOX). As shown in Figure 1(a), the fin-height is defined by the silicon layer thickness on the BOX, which results in much less fin-height variation compared to bulk FinFETs [7]. The device parameters are shown in Fig. 1(b) featuring 20-nm physical gate length and 0.8-nm EOT. High- κ material is used for the gate stack, and mid-gap workfunction TiN is adopted as the gate metal. An effectively undoped channel (10^{15} cm^{-3}) and high source/drain conformal doping $3 \times 10^{20} \text{ cm}^{-3}$ are adopted in the simulations. The spacer thickness is optimised with respect to short-channel effects and series resistance. The drift-diffusion simulations are calibrated against comprehensive Monte-Carlo simulations, shown in Fig. 2. After calibration, the source-side velocity is matched for drift-diffusion simulations and Monte Carlo simulations for a series of devices. Density gradient quantum corrections are essential due to the thin fin body.

Supposedly identical close pairs of nanometre-scale devices show differences in key figures of merit, which is due to intrinsically random effects beyond the process control. Statistical variability sources have been extensively studied by experimental data and simulations, including random dopants (RDDs), gate and fin line edge roughness (LER), and metal gate granularity (MGG) [3]. In the statistical simulations RDDs are assigned based on the local continuous doping using a rejection technique; LER is generated by Fourier synthesis using Gaussian autocorrelation function parameterized by LER of 2-nm and correlation length of 30-nm, and uncorrelated random traces are assumed for both gate and fin-width; MGG

This work is in part supported by Scottish Funding Council through project “Statistical Design and Verification of Analogue Systems (StatDes).”

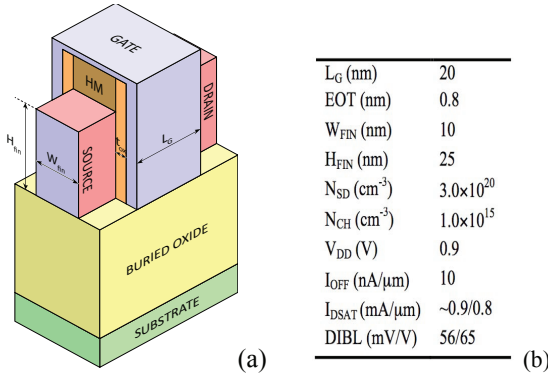


Figure 1. (a) The schematic view of double-gate SOI FinFET, and (b) the device parameter set in the simulations and the performance characteristics at 85°C.

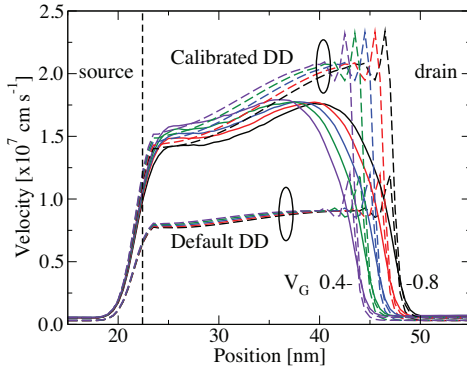


Figure 2. The average carrier velocity in the channel obtained from Monte Carlo (solid lines) and Drift-Diffusion (dashed lines) simulations of a series of scaled FinFETs.

models the work-function variation due to different polycrystalline metal grain orientations. Two metal grain orientations are modelled with WF difference of 0.2V with 0.4/0.6 probabilities, and average metal grain diameter of 5-nm is used in the simulations. Ensembles of 1000 microscopically different atomistic devices for each uniform device are simulated using GSS cluster simulation technology.

III. INTERACTIONS BETWEEN PROCESS AND STATISTICAL VARIABILITY IN FINFETs

In this section, the statistical variability of 14-nm DG SOI FinFETs obtained from 3-D atomistic simulations is presented. The statistical variability of key figures of merit is extracted and monitored. First the statistical variability of nominal design ($L_G=20$ nm, $W_F=10$ nm, $H_F=25$ nm) is examined. While the figures of merit in the combined RDD and LER simulations, relevant to gate-last process show close correlation, the drain induced barrier lowering (DIBL) (and even I_{ON} to some degree) in the combined RDD, LER and MGG simulations representing gate-first technology, is de-correlated with the rest of the figures of merit as shown in Figure 3. Threshold voltage is inadequate to fully capture subthreshold variation [8]. Therefore the error could be significant when just considering threshold voltage fluctuation in a compact model.

Key critical dimensions for FinFETs include gate length L_G , fin width W_F , and fin height H_F . The CD process variations (3σ) from nominal design corresponding to process corners are assumed to be: $\Delta L_G = \pm 2$ nm; $\Delta W_F = \pm 2$ nm; $\Delta H_F = \pm 3$ nm. Comprehensive statistical simulations were carried out at each CD process corners and the results covering the CD variation space were reported in [4]. The FinFET performance is dramatically affected by process deviations. Shown in Fig. 4 the on -current is proportional to fin height, and also strongly depends on the gate length and fin width. The on -current increases by 48% from the slow corner ($L_G=22$ nm, $W_F=8$ nm, $H_F=22$ nm) to the fast corner ($L_G=18$ nm, $W_F=12$ nm, $H_F=28$ nm). Meanwhile, the statistical variability is heavily dependent on process variation, clearly shown in Fig. 5 by σV_T changing from 21.8mV to 34.6mV and σI_{ON} increasing by $\sim 40\%$ from the slow to fast corner. Therefore, the statistical variability is greatly affected by the FinFET CD process variations.

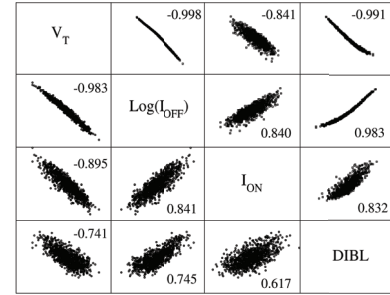


Figure 3. The scatter plot of the key FinFET figures of merit for the nominal device. The upper-right is for statistical variability sources representing gate-last; the bottom-left represents gate-first process [4].

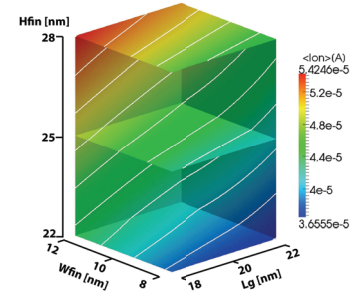


Figure 4. The I_{ON} response to the key CD process variations [4].

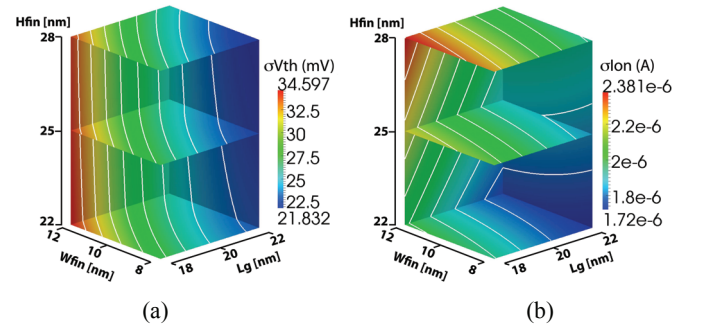


Figure 5. The statistical variability of (a) V_T and (b) I_{ON} in the key CD process variation space [4].

IV. VARIABILITY COMPACT MODELLING

The compact model sits at the heart of the process design kit (PDK) for circuit simulation and verification [9]. *Mystic* [6] is used to extract uniform and statistical compact models. First the nominal compact model is extracted to represent the uniform device of nominal design. As shown in Fig. 6, the nominal uniform model accurately replicates I_D - V_G characteristics of devices with a series of gate lengths around the nominal design. In order to capture the statistical variability, direct extraction using a small set of carefully selected model parameters based on the nominal uniform model usually provides an effective and accurate method in bulk planar MOSFET technology [5]. The excellent fitting is achieved with average error 2.3%. This statistical compact modelling strategy is applied to SOI FinFETs for the range of process variations. However, this traditional method fails to accurately capture full variability at process corners. With statistical variability of V_T and I_{ON} illustrated in Fig. 7, using the traditional statistical compact modelling strategy, the error of σV_T can reach more than 30% and the error of σI_{ON} goes above 20%. The reasons include the incapability of the uniform model to cover process variation, especially fin width. Additionally it ignores the dependence of statistical variability on CD process variation. Therefore, a novel statistical compact modelling strategy is required taking care of the correlation between the statistical variability and the process variation.

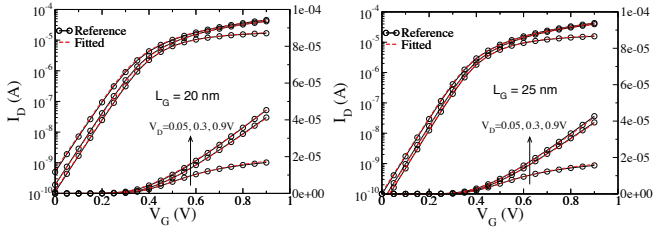


Figure 6. Uniform model card accuracy in reproducing I_D - V_G transfer characteristics of nominal design.

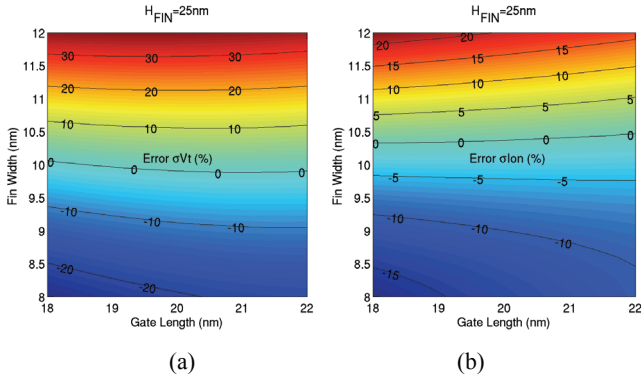


Figure 7. Error plots of standard deviations of (a) V_T and (b) I_{ON} in the process variation space using simple direct approach at $V_D = 0.9$ V.

V. PRINCIPAL COMPONENT ANALYSIS METHOD

In this section, we present a novel statistical compact modelling strategy using the principal component analysis (PCA) technique, taking into account the process variation and the interplay of statistical variability and process variability. Shown in Fig. 8, the key steps of this unified method includes,

first, the extended uniform model extraction for CD process variation using a small set of parameters based on the nominal uniform model; second, the statistical extraction using another small set of parameters at process corners and following statistical generation of model parameters using PCA.

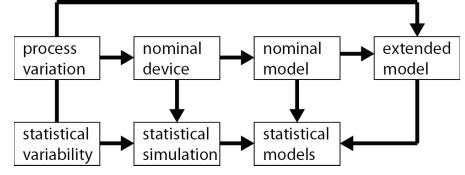


Figure 8. The unified compact model strategy.

At first, based on the uniform model originally extracted for nominal design, the extended uniform model is extracted using a small set of model parameters (Group I). Shown in Fig. 9 these model parameters are smoothly responding to CD variations. Extraction of statistical compact model parameters from atomistic simulations at each corner is carried out using another small set of ‘statistical’ parameters (Group II). The covariances of statistical parameters can also be smoothly fitted using quadratic functions in CD space (Fig. 10).

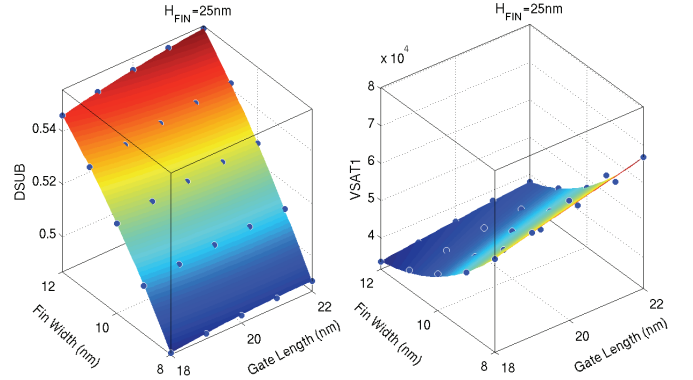


Figure 9. The response of fitting parameters (Group I) to CD variation.

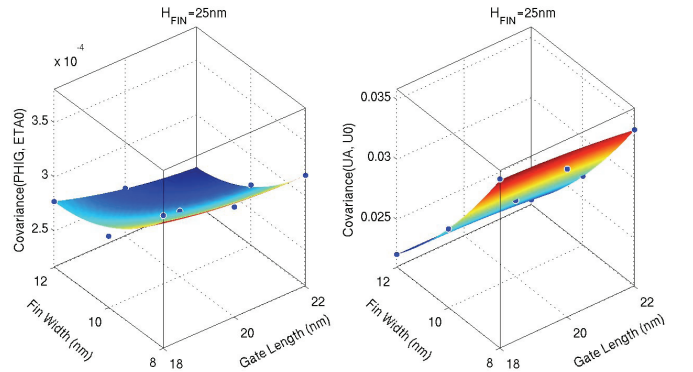


Figure 10. The response of covariance of fitting parameters (Group II) to CD variation.

PCA method decomposes the random multivariants into independent components based on their covariances. It can be achieved by eigenvalue decomposition as follows:

$$U'SU = L \quad (1)$$

where S is the covariance matrix; U is the orthogonal matrix; L is the eigenvalue diagonal matrix after orthogonal transformation. Then, statistically generated parameters are obtained from L and U assuming independent component distributions. In this unified statistical compact modelling strategy, given a CD point, the covariance matrix is fed into PCA, and finally the statistical parameters are generated for this CD point. Shown in Fig. 11, two generated parameters are plotted in normal quantile-quantile (QQ) against the extracted parameters. PCA is known to easily replicate a normal distribution, but fail to reproduce skewed distributions.

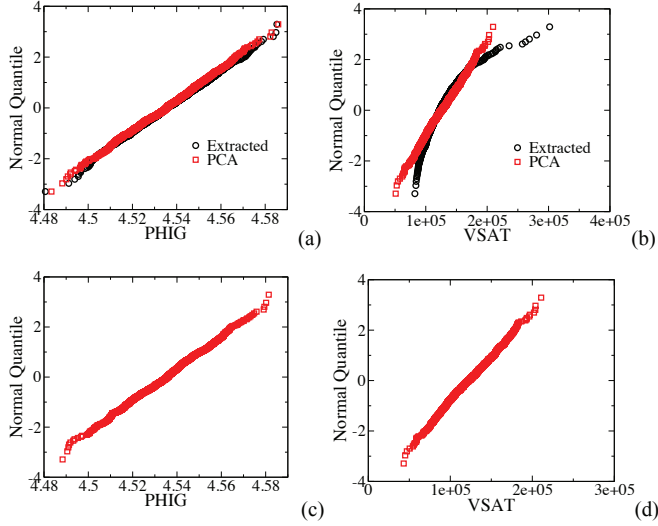


Figure 11. The QQ plots of generated parameters (Group II) and extracted parameters at nominal design (a) and (b); The QQ plots of generated parameters at an arbitrary CD point ($L_G=19\text{nm}$, $W_F=11\text{nm}$, $H_F=26\text{nm}$), (c) and (d).

Fig. 12 compares the correlations among model parameters obtained by PCA with those from direct extraction. Most of them are well maintained. Fig. 13 compares the distribution and correlation of major figures of merit of devices, including threshold voltage, on-current, and DIBL. The variability magnitudes of these figures of merit are well captured despite some tail-value departure of I_{ON} and DIBL, and the correlations are also decently maintained.

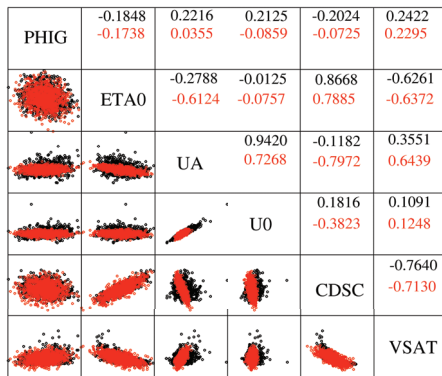


Figure 12. The correlations between parameters from extraction (black) and PCA generation (red) at nominal design. Numbers are corresponding correlation coefficients.

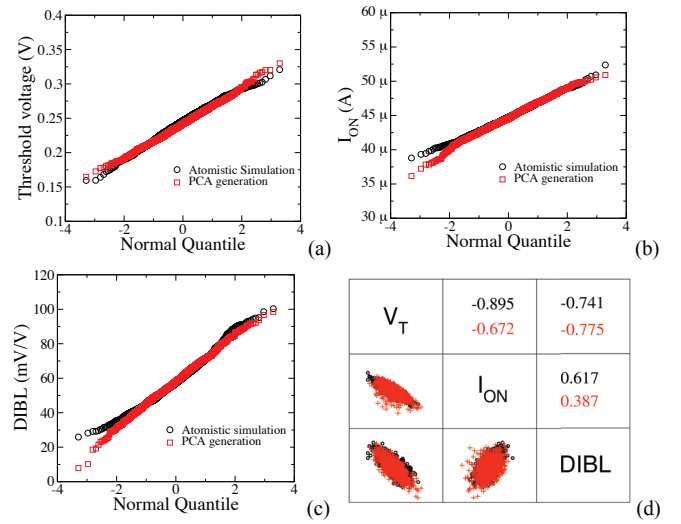


Figure 13. QQ plots of figures of merit from atomistic simulations and PCA generation (a), (b), (c) and their correlations (d) at nominal design.

VI. CONCLUSIONS

In this paper we present a PCA-based unified statistical compact modelling strategy coherently taking into account the interplay of statistical variability and process-induced CD variations. Satisfactory accuracy is achieved. It provides a simulation framework to evaluate variability impact on the circuit performance and yield for FinFET technology.

REFERENCES

- [1] C. Auth, C. Allen, A. Blattner, et al., "A 22nm High Performance and Low-Power CMOS Technology Featuring Fully-Depleted Tri-Gate Transistors, Self-Aligned Contacts and High Density MIM Capacitors" in *VLSI Tech. Sym.*, 2012, pp.131-132.
- [2] T. Matsukawa, S. O'uchi, K. Endo, et al., "Comprehensive analysis of variability sources of FinFET characteristics," in *VLSI Tech. Sym.*, 2009, pp.118-119.
- [3] X. Wang, A. R. Brown, B. Cheng, and A. Asenov, "Statistical variability and reliability in nanoscale FinFETs," in *Proc. IEEE International Electron Devices Meeting*, 2011, pp.103-106.
- [4] X. Wang, B. Cheng, A. R. Brown, et al., "Interplay Between Process-Induced and Statistical Variability in 14-nm CMOS Technology Double-Gate SOI FinFETs," *IEEE Trans. Electron Devices*, to be published.
- [5] B. Cheng, D. Dideban, N. Moezi, C. Millar, G. Roy, X. Wang, S. Roy and A. Asenov, "Statistical Variability Compact Modelling Strategies for BSIM4 and PSP," *IEEE Design and Test of Computers*, Vol. 27, No. 2, pp. 26-35, Mar./Apr. 2010.
- [6] Garand, *Mystic*, 2013, <http://www.goldstandardsimulations.com/>
- [7] D. Fried, T. Hoffmann, B.-Y. Nguyen, S. Samavedam and H. Mendez, "Comparison study of FinFETs: SOI vs. Bulk - Performance, Manufacturing Variability and Cost", SOI Industry Consortium Report, October 2009.
- [8] X. Wang, F. Adamu-Lema, B. Cheng, A. Asenov, "Geometry, Temperature, and Body Bias Dependence of Statistical Variability in 20-nm Bulk CMOS Technology: A Comprehensive Simulation Analysis," *IEEE Trans. Electron Devices*, Vol.60, No.5, pp.1547-1554, May 2013.
- [9] C.K. Lin, C. Hsiao, H.C. Tseng, M.-C. Jeng, "A Comprehensive Solution for Process Variation Characterization and Modelling," in *Proc. SISPAD*, 2012, pp.197-200.