Unified FinFET Compact Model: Modelling Trapezoidal Triple-Gate FinFETs

Juan Pablo Duarte, Navid Paydavosi, Sriramkumar Venugopalan, Angada Sachid and Chenming Hu
Dept. of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA, USA

Phone: +1-510-664-4425, e-mail: jpduarte@eecs.berkeley.edu

***Abstract*—A unified FinFET compact model is proposed for devices with complex fin cross-sections. It is represented in a normalized form, where only four different model parameters are needed. The proposed model accurately predicts the current-voltage characteristics of different FinFETs structures such as Double-Gate (DG), Cylindrical Gate-All-Around (Cy-GAA), or Rectangular Gate-All-Around (Re-GAA) FinFETs. In addition, for the first time, Trapezoidal Triple-Gate (T-TG) FinFETs are accurately modelled. Short-Channel-Effects (SCE) sub-models have been also implemented in the presented work. The model has been verified with TCAD data.**

I. Introduction

The downscaling of planar transistors has brought several detrimental effects such as increment of leakage currents and enhancement of Short-Channel-Effects [1] [2]. In this context, FinFET devices (Fig. 1) have been recently adopted by the industry as a substitute of conventional bulk planar transistors [3] [4]. The adoption of FinFETs solves several problems of planar transistors by improving the electrostatic control of the gate over the entire semiconductor channel, resulting in an increment of on-current and a reduction of Short-Channel-Effects.

Accurate and fast compact models for transistors are one of the main pillars in circuit simulators. Indeed, compact models represent an interface between circuit designers and device technology. The Compact Model Council (CMC) has chosen BSIM-CMG [5] [6] as the first and only industry-standard compact model for FinFETs. The core model used in BSIM-CMG is based on the solution of a rectangular shape DG-FinFET.

The typical rectangular cross-section of FinFETs is hardly found on industry FinFETs. Indeed, whether intentional or due to manufacturing variation, industry FinFET cross-sections are non-uniform and similar to Trapezoidal shapes [3] [4]. In order to capture fin shape effects on device performance, a compact model for FinFETs with complex cross-sections is important and timely. In this work, a unified FinFET compact model is proposed for devices with complex fin cross-sections as those shown in Fig. 2. FinFETs structures such as Double-Gate, Cylindrical Gate-All-Around, Rectangular Gate-All-Around and Trapezoidal Triple-Gate FinFETs, are all modelled under the same frame work. Fig. 3 shows the general structure of the proposed compact model. A single unified core model is used for different FinFET structures and only model parameters are different for each FinFET structure, which are pre-calculated for each device type and dimension. The proposed core model is complemented with Short-Channel-Effects sub-models mainly obtained from BSIM-CMG [5] [6].

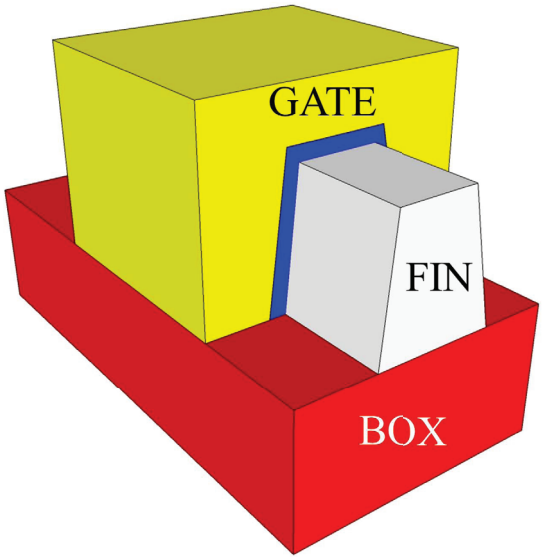

Fig. 1: A 3-dimensional schematic of a Triple-Gate FinFET with a Trapezoidal fin cross-section.

II. Unified FinFET Compact Model

Several compact models have been proposed for FinFETs with complex cross-sectional shapes. The work presented in [7] developed compact models for different undoped or lightly doped FinFETs shapes utilizing a combination of the compact models for DG [8] and Cy-GAA FinFETs [9]. In [10], a compact model for undoped or lightly doped FinFETs was extended to model FinFETs with different cross-sectional shapes by obtaining an equivalent channel thickness for each structure. Another compact model has been recently proposed for FinFET devices with different cross-sectional shapes [11], [12], where new models for doped FinFETs were developed in a universal model framework. In this work, based on the approach presented in [11], a new normalized unified FinFET core model is proposed. The new normalized charge model is obtained from the solutions of the Poisson equation for DG and Cy-GAA FinFETs, which leads to a single closed form relationship between the mobile charge and the applied terminal voltages given as follows [11]:

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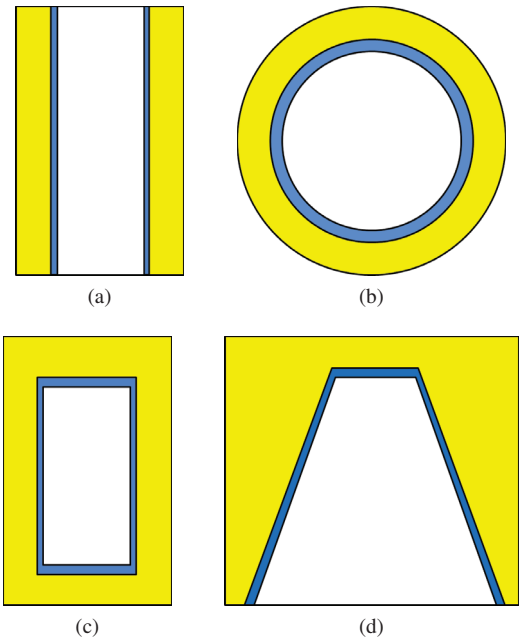

Fig. 2: Schematic channel cross-section of various Multiple-Gate FinFETs that can be simulated using the proposed Unified FinFET Compact Model. (a) Double-Gate (DG). (b) Cylindrical Gate-All-Around (Cy-GAA). (c) Rectangular Gate-All-Around (Re-GAA). (e) Trapezoidal Triple-Gate (T-TG).

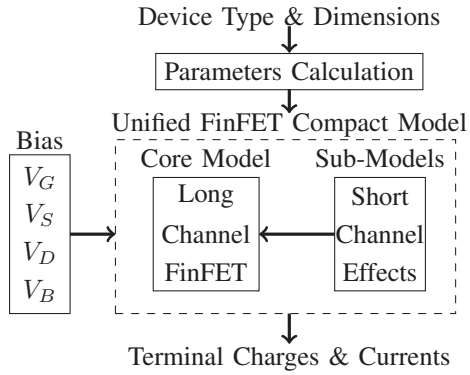

Fig. 3: Schematic structure of the proposed compact model.

$$v_G - v_o - v_{ch} = -q_m + \ln\left(\frac{-q_m q_t^2}{e^{q_t} - q_t - 1}\right) \tag{1}$$

where v_o and q_t are represented by:

$$v_o = v_{FB} - q_{dep} - \ln\left(\frac{2qn_i^2 A_{ch}}{v_T C_{ins} N_{ch}}\right) \tag{2}$$

$$q_t = (q_m + q_{dep}) r_N \tag{3}$$

In the previous equations, v_G and v_{ch} are the normalized gate and channel potentials expressed by:

$$v_G = \frac{V_G}{v_T} \tag{4}$$

$$v_{ch} = \frac{V_{ch}}{v_T} \tag{5}$$

q_m and q_{dep} are the normalized mobile and depletion charges:

$$q_m = \frac{Q_m}{v_T C_{ins}} \tag{6}$$

$$q_{dep} = \frac{-qN_{ch}A_{ch}}{v_T C_{ins}} \tag{7}$$

r_N is given by:

$$r_N = \frac{A_{Fin} C_{ins}}{\varepsilon_{ch} W^2} \tag{8}$$

A_{ch} is the area of the channel, N_{ch} is the doping in the channel, W is the channel width, and C_{ins} is the insulator capacitance per unit length. The normalized drain current is obtained from the solution of the Poisson-carrier transport equation [12] and it is represented by:

$$i_{DS} = \left[\frac{q_m^2}{2} - 2q_m - q_H \ln\left(1 - \frac{q_m}{q_H}\right)\right]\Bigg|_{q_{m,S}}^{q_{m,D}} \tag{9}$$

where q_H is equal to:

$$q_H = \frac{1}{r_N} - q_{dep} \tag{10}$$

The drain current normalization is given by:

$$i_{DS} = \frac{-I_{DS} L}{\mu_m v_T^2 C_{ins}} \tag{11}$$

Note that only four different model parameters are needed for the modelling of FinFET devices: A_{ch}, N_{ch}, W, and C_{ins}. Using these parameters, a FinFET with simple cross-section, such as DG FinFET, can be accurately modelled for different channel doping concentrations as shown in Fig. 4. The model parameters used for DG FinFETs are given as follows [11]:

$$A_{ch} = H_{Fin} T_{Fin} \tag{12}$$

$$P_{ins} = 2H_{Fin} \tag{13}$$

$$C_{ins} = \frac{P_{ins}\varepsilon_{ins}}{EOT} \tag{14}$$

$$N_{ch} \tag{15}$$

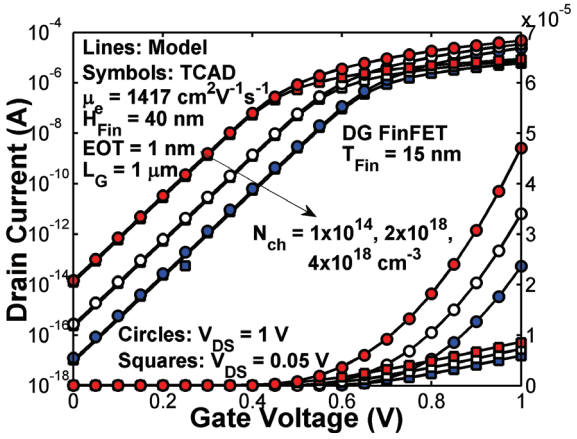

Fig. 4: Drain current versus gate voltage of DG FinFETs.

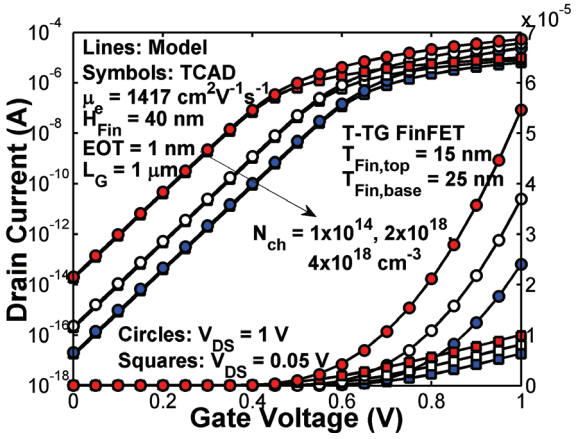

Fig. 5: Drain current versus gate voltage of T-TG FinFETs.

III. Trapezoidal Triple-Gate Model

A Trapezoidal Triple-Gate FinFET is a good example of a FinFET with a complex cross-section. Indeed, the industry transistors reported in [3] and [4] have fin cross-sections similar to trapezoidal shapes. The proposed model can be used to model these type of devices through the use of the following four model parameters:

$$A_{ch} = H_{Fin}\frac{(T_{Fin,top} + T_{Fin,base})}{2} \tag{16}$$

$$P_{ins} = 2\sqrt{\frac{(T_{Fin,base} - T_{Fin,top})^2}{4} + H_{Fin}^2} + T_{Fin,top} \tag{17}$$

$$C_{ins} = \frac{P_{ins}\varepsilon_{ins}}{EOT} \tag{18}$$

$$N_{ch} \tag{19}$$

Using these parameters, T-TG FinFETs can be accurately modelled as shown in Fig. 5, where a T-TG FinFET has been doped at different doping concentrations as it is used in chips with multi-threshold voltage levels.

In the case of a channel dimension variation the model can accurately predicts the trend of current changes (Fig. 6). Note that a $T_{Fin,top}$ variation is more important for the on-current than a $T_{Fin,base}$ variation. In addition, the off-current linearly varies as function of $T_{Fin,top}$ or $T_{Fin,base}$, as expected.

IV. Short Channel Effects

Short-Channel-Effects sub-models have been implemented in the presented work (Fig. 3). They are mainly adopted from BSIM-CMG [5] including: saturation velocity, parasitic source and drain resistances, mobility degradation due vertical field, threshold voltage (V_{TH}) roll-off, etc. The degree of V_{TH} roll-off has been modelled through the characteristic field penetration length, which is proposed as follows:

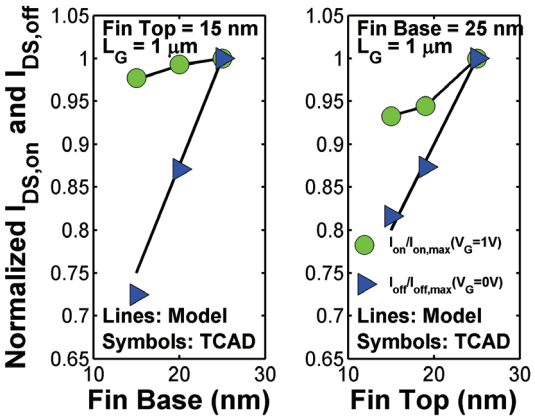

Fig. 6: Normalized ($I_{DS}/I_{DS,MAX}$) on (circles) and off (triangles) drain currents.

$$\lambda = \sqrt{\frac{\varepsilon_{ch}A_{ch}}{C_{ins}}} \tag{20}$$

It can be used for different types of FinFETs and it captures the V_{TH} roll-off dependence on model parameters as shown by Fig. 7. In order to reduce SCEs, the proposed characteristic field penetration length clearly states that the area of the fin must be minimized and the insulator capacitance must be maximized.

The proposed model accurately models experimental short channel FinFETs as shown by Fig. 8 which compares the proposed compact model including SCE sub-models and the data from a fabricated short channel T-TG FinFET on SOI.

V. Conclusion

A unified FinFET compact model has been developed for devices with complex fin cross-sections. It only requires four different model parameters to represent device characteristics. The proposed work models, for the first time, Trapezoidal Triple-Gate FinFETs. Good agreement of proposed model with TCAD and experimental data demonstrates the physical

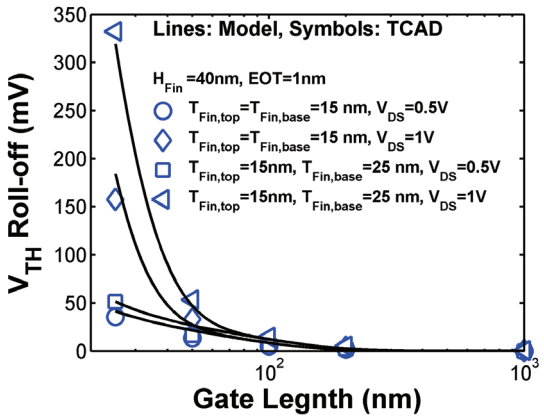

Fig. 7: V_{TH} Roll-off of two T-TG FinFETs with different cross-section dimensions.

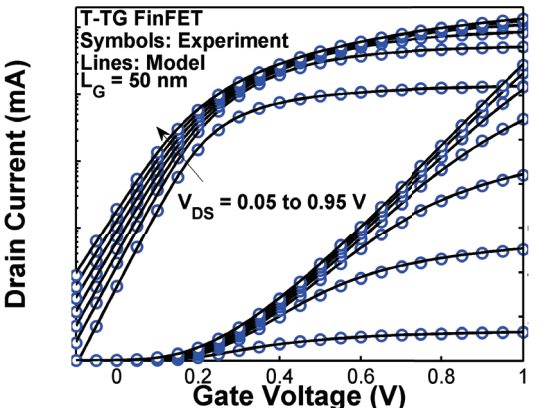

Fig. 8: Drain current versus gate voltage of a short channel multiple-fin T-TG FinFET.

predictability and scalability of the model for FinFETs with complex cross-sections.

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