Process Window Definition for Power MOSFET by Transient Avalanche Device Simulation

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Abstract—**A mixed-mode transient simulation model has been developed to simulate device avalanche performance under Unclamped Inductive Switching (UIS) condition with self-heating involved, which can quantify process variation tolerance to satisfy both DC and energy requirements. Two simulation approaches: single half-cell and asymmetric full-cell were used to enable us to investigate unbalanced current and field crowding behavior during UIS when process window is varied. We use the TCAD simulation model and methods to evaluate the influence of design variation. This also serves as guidance for setting process windows, ensuring device robustness is least affected by process variation.**

Keywords-Avalache current, avalanche ruggedness, trench Power MOSFET, Unclamped Inductive Switching(UIS), process window

I. INTRODUCTION

The avalanche ruggedness of power MOSFETs under unclamped inductive switching (UIS) is a major requirement in many automotive and switching power supply applications which involve inductive loads. Avalanche ruggedness improvement has been discussed over many years and is still receiving considerable attentions nowadays, especially since device Rdson and pitch is becoming smaller and manufacturing cost reductions are required. When pitch continues to reduce, the trade-off between low on-resistance, fast switching and high energy capability are becoming more and more severe. High volume manufacturing requires clearly defined process windows to produce high yielding, fast and rugged Power MOSFETs for consumer and especially automotive applications. Process variation can have much stronger impact on device UIS performance than on the normal DC electrical performance, which becomes an increasing important design concern in state-of-the-art trench MOSFET design. In most of recent simulation publications [1]-[5], different simulation methods have been discussed to help understand UIS and improve design, but not many have discussed defining process window control or understanding process variation impact on UIS by visualizing electrons and holes behavior in TCAD. A few process variations that have been addressed include epitaxial layer and gate oxide thickness, but no literature has been reported for the misalignment and other combined effects of process window variation resulting in an asymmetric structure and the impact on UIS performance.

In this paper, we developed a mixed-mode circuit-device UIS simulation which provides an established methodology for incorporating accurate finite-element (FEM) level semiconductor device models in a UIS circuit, and obtain physically accurate predictions of circuit and device behavior under manufacturing process variation window. Simulation results have been compared and validated by measured data. In Section II, we use TCAD simulations to demonstrate physical mechanism involved during UIS events, and visualize the electrons and holes behavior as the charging pulse width and peak current increase from device pass to fail. UIS waveforms are studied. In Section III, we present detail of the numerical simulation results to address some normal manufacturing wafer process and design variation windows that affect UIS capability. These include: trench depth window, trench and contact critical dimension (CD) variation window, contact alignment window, contact depth window and their combined effects. Conclusions are given in Section IV.

II. ACCURATE MIXED-MODE UIS SIMULATION

Fig. 1 shows the UIS test circuit diagram. Mixed-mode transient simulation is performed on the same circuit diagram by taking account of circuit parasitic components, device die size, package thermal impedance, and device self-heating effects. In this paper, we simulate a typical International Rectifier 40V device. The devices simulated in this section are default center process without process variation. Fig. 2 shows the simulated UIS transient voltage and current waveforms for a 40V device from pass to fail with L=20μH and starting ambient temperature 175ºC. Device junction temperature (Tmax) is also extracted during the UIS transient event. The peak junction temperature happens at the middle of the discharge pulse width. The simulation predicts device thermal destruction at a junction temperature around 450ºC. With gate charging pulse width increase, device current and junction temperature keep increasing. Once the peak junction temperature exceeds 450ºC, device fails with a deformed Vds curve, and the peak current before failure is recorded as UIS peak current IAS. The junction destructive temperature is determined by the doping concentration of the epitaxial layer and in our case is 450ºC [1], [5], which indicate a good device design with pure thermal failure. TCAD simulation predicts failure current for devices well match the measured data average values across different die sizes as shown in Fig. 3.

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Fig. 4 shows simulated figures captured at the beginning of avalanche at the peak current for two gate charging pulse widths when device pass and fail. With gate charging pulse width increase, device peak impact ionization location (Fig. 4 (a) (b)) moves from trench bottom toward channel/Epi junction until the junction breaks. When the channel/Epi junction breaks, large amount of electron current (Fig. 4 (c) (d)) sweeps through channel, and device fails. Hole current (Fig. 4 (e) (f)) is collected by source with some crowding at the bottom of trench where impact ionization happens, while majority passes through part of the channel where parasitic bipolar base present. Default center process is designed to shift the latch-up of bipolar to current densities beyond the thermal destruction point.

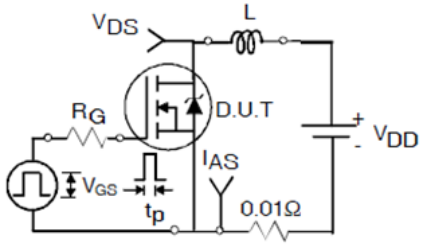


Figure 1 Circuit diagram of UIS.

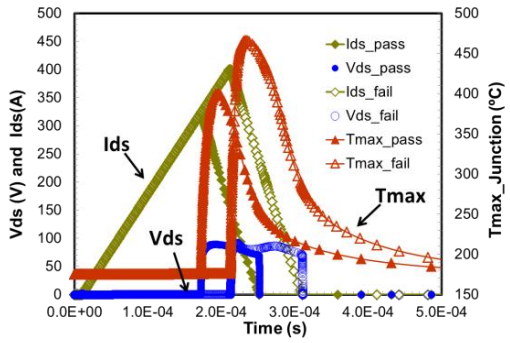


Figure 2 Simulated UIS waveforms and extracted junction temperature.

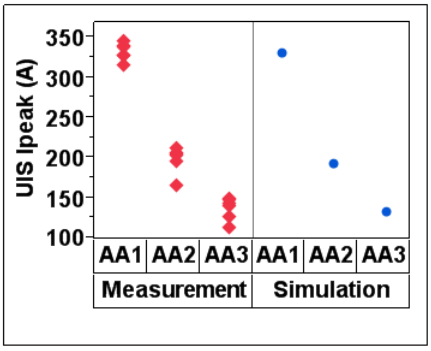


Figure 3 Simulated UIS peak current compared with measured data for devices with different die sizes.

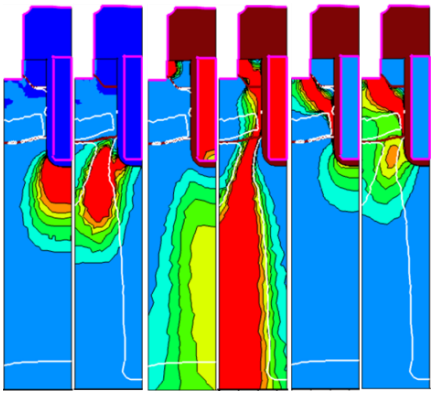


Figure 4 Simulation figures for default process, captured at the beginning of avalanche at the peak current, showing impact ionization (a) (b), electron current (c) (d), and hole current (e) (f) for shorter pulse passing case (a) (c) (e) and longer pulse failure case (b) (d) (f).

III. Process Variation Windows Impact on UIS Avalanche Ruggedness

A. *Trench Depth Window*

In the simulation, we assume a trench depth variation window from -20% to +20% which is larger than measured manufacture window from -10% to +10%. Fig. 5 shows IAS increases with trench depth increase, and simulated values have good qualitative match with measured average data. To reveal the physical mechanism involved, Fig. 6 shows the heat dissipating flows for devices with different trench depth at the same gate charging pulse. Figures are captured at the beginning of avalanche when the peak current happens. Heat is generated at the impact ionization location and is dissipated along the channel (trench sidewall). With trench depth increases, the hotspot moves vertically away from the channel/Epi junction, which helps to reduce the heat residue in the channel, thus resulting in an overall lower junction temperature (Fig. 5). Therefore, device with a deeper trench can sustain longer charging pulse before the junction reaches thermal breakdown.

B. *Contact Alignment Window*

A full cell structure has been used here to investigate the contact alignment window impact on UIS. Fig. 7 shows the simulated electro-static potential contours for contact misalignment from 0 to 28% at the same gate charging pulse. As misalignment increases, one side of the channel gets shorter and body becomes weaker. On this side of the trench, the parasitic bipolar tends to be triggered easier due to a shorter bipolar base width and reduced built-in potential across base and emitter. The holes generated by impact ionization flow through p-body region of the NMOS thus creating a potential drop in the base region of the parasitic bipolar transistor. If this potential drop exceeds the built-in potential of the base-emitter diode the BJT will turn-on, i.e. latch up. Since a BJT has a negative temperature coefficient of breakdown voltage, latch-up is self-amplifying, thus concentrating the current on a small region of the device. As the built-in potential reduces, large electron current sweeps through one side of the channel,

accelerating the junction thermal breakdown (Fig. 8). Also the unbalanced current flow and field crowding will cause hot spots in the weak cell, and the positive feedback will bring the destruction of the whole device. Fig. 9 shows that as contact misalignment increases, parasitic bipolar built-in potential for the same gate pulse reduces, which results in a decreasing UIS peak current (IAS).

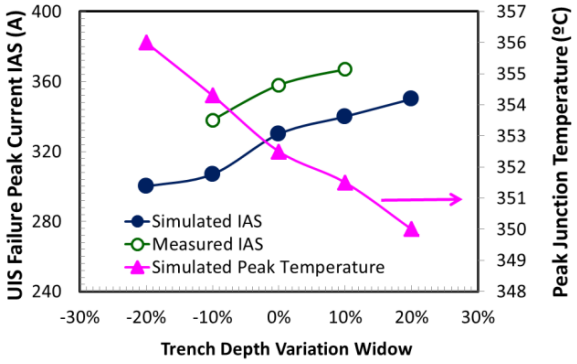
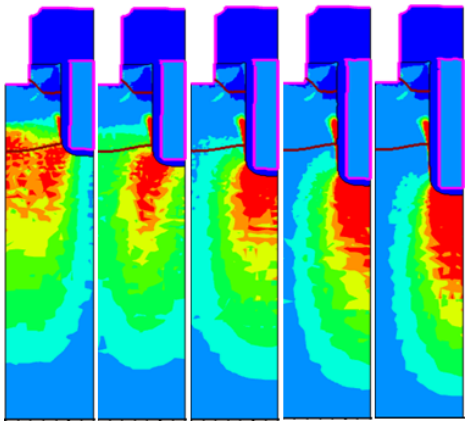
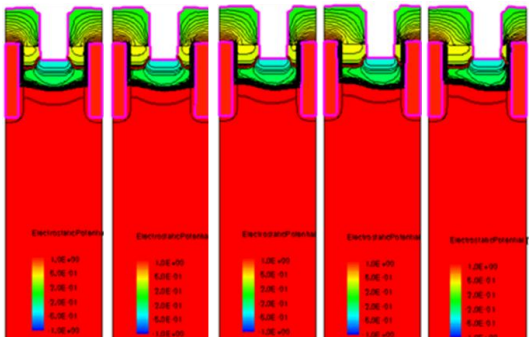


Figure 5 Simulated and measured UIS peak failure current IAS, and extracted junction temperature for trench depth variation window. Junction temperatures for different trench depth are extracted at the same gate charging pulse.



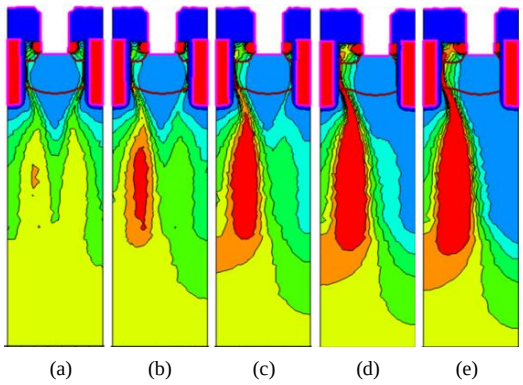
(a) (b) (c) (d) (e)

Figure 6 Simulation heat flow for trench depth window captured at the beginning of avalanche. (a) -20%, (b) -10%, (c) default, (d) +10% (e) +20%.



(a) (b) (c) (d) (e)

Figure 7 Simulated potential contours in p-body (bipolar base) for contact alignment window by using asymmetric full-cell method, from (a) 0, (b) 8%, (c) 16%, (d) 24%, and (e) 28%.



(a) (b) (c) (d) (e)

Figure 8 Simulated electron current flow for contact alignment window by using asymmetric full-cell method, from (a) 0, (b) 8%, (c) 16%, (d) 24%, and (e) 28%.

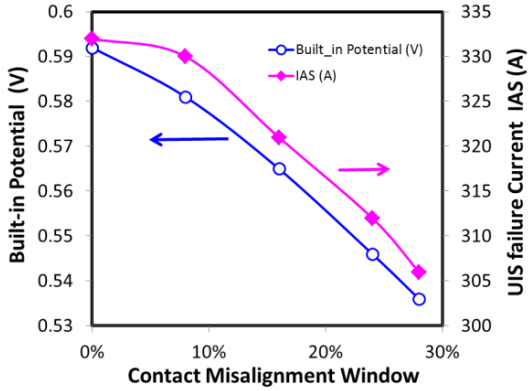


Figure 9 Simulated UIS peak current IAS and extracted built-in potential for different contact alignment window. The built-in potential is extracted from base-emitter diode of the parasitic BJT for the same gate charging pulse.

C. *Trench Width and Contact Width CD Window*

Trench width and contact width critical dimension (CD) have strong impact on device UIS avalanche ruggedness. Fig. 10 shows the simulated IAS response to trench width and contact width variation window. As trench width or contact width increase, device IAS increases. In wider trench or wider contact case, Boron doping concentration is higher and diffuses closer to the channel, resulting in a higher built-in potential and wider base width of the parasitic bipolar, thus improving UIS performance. With the help from simulation, we can better quantify design rule impact on device UIS performance.

D. *Contact-Etch Depth Window*

Fig. 11 shows simulated IAS increase with contact depth increase. Deeper contact places the high dose Boron implant deeper and moves the body/Epi junction deeper. With contact depth increase, the impact ionization location moves laterally away from the channel/Epi junction, resulting in an overall lower junction temperature compared to shallower contact

depth for the same charging pulse (Fig. 11). Also, deeper contact brings higher boron doping near parasitic bipolar base resulting in a higher built-in potential across base and emitter, making it harder to trigger the bipolar effects.

E. Process Windows Combination

Combined effects from variation of actual process windows are simulated in TCAD, with results collected in Table 1. The window boundary covers the best and worst case, representing the device-to-device variation across a wafer during normal manufacturing. Fig. 12 shows the excellent match between simulation and measured data achieved from different locations

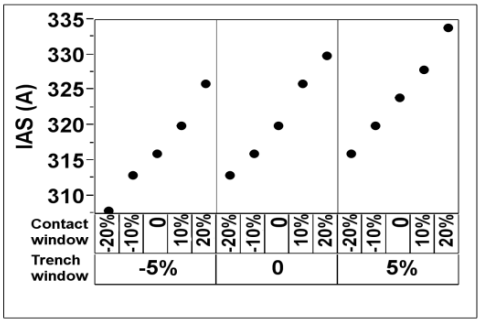


Figure 10 Simulated UIS peak failure current (IAS) response to different contact width and trench width window.

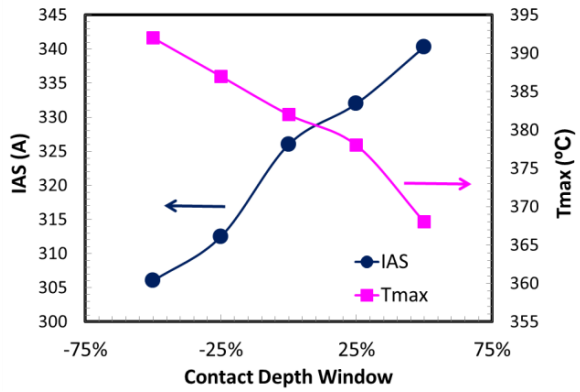


Figure 11 Simulated UIS peak failure current IAS and extracted junction temperature for different contact depth window.

TABLE 1 IAS DEPENDENCE ON COMBINED PROCESS WINDOWS

Contact Alignment Window	Trench Depth Window	Trench CD Window	Contact CD Window	Contact Depth Window	IAS (A)
0	+10%	+5%	+20%	+25%	346
0	0	+5%	+20%	+25%	340
0	0	+5%	+20%	0	334
0	0	-5%	+10%	0	320
0	0	-5%	-20%	-25%	300
+12%	0%	+5%	+20%	+25%	331
+12%	0%	+5%	+20%	0	326
+12%	0%	-5%	+10%	-25%	293
+12%	-10%	-5%	-20%	-25%	288

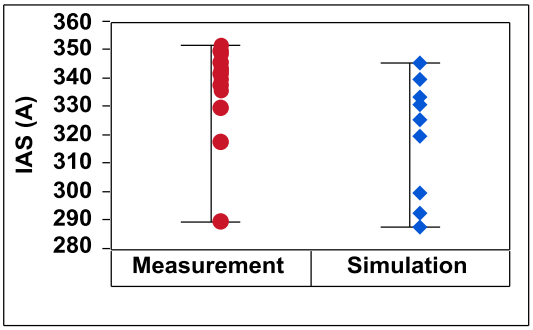


Figure 12 Comparison between simulation and measurement. Simulated IAS has taken account of combination effects of process variation windows; measurement has been done across the wafer.

of a wafer. It demonstrates that simulation can reproduce the variation across a wafer by taking into account some of the critical process variation windows. The in-house developed simulation can either be used to define the required process windows for a certain UIS performance or to evaluate process sensitivity for different designs.

IV. CONCLUSION

In summary, we have developed an accurate mixed-mode 2D transient simulation module to evaluate device UIS avalanche performance, demonstrating physical mechanisms inside devices during UIS transient events. It has been shown that TCAD simulation is an effective tool for evaluating variations that may occur during normal manufacturing and defining a suitable process window to ensure a robust UIS. This method is helpful for defining a new platform (new structure and new process) before engineering fabrication, shortening the development cycle and reducing cost.

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