Physics of Optimized High Current ESD Performance of Drain Extended NMOS (De-NMOS)

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Abstract—**In this abstract, the impact of the gate and substrate biasing on the 3D current crowding behavior in the drain extended devices has been correlated with the shape of the N-Well. Role of am-bipolar current flow in an optimized device structure for designing an efficient ESD protection device has been discussed by utilizing the self ballasting mechanisms under high current injection**

I. Introduction

Poor ESD performance of De-NMOS is a major reliability concern for designing high voltage drivers in low voltage technologies which need ESD protection techniques (fig. 1) [1-4]. A fundamental requirement of the design strategy for ESD protection needs co-ordination between the ESD protection cells and the safe operation area as the efficacy of the protection devices depend both on the "turn-on" behavior of the parasitic bipolar in the structure and also dispersion of localised (J.E) Joule heating [4,6]. In brief, the physics behind the filamentation in a gated n-FET structure need accurate modeling of the parasitic bipolar turn-on first in 2D and subsequently one need to address the critical 3D aspect [3,4].

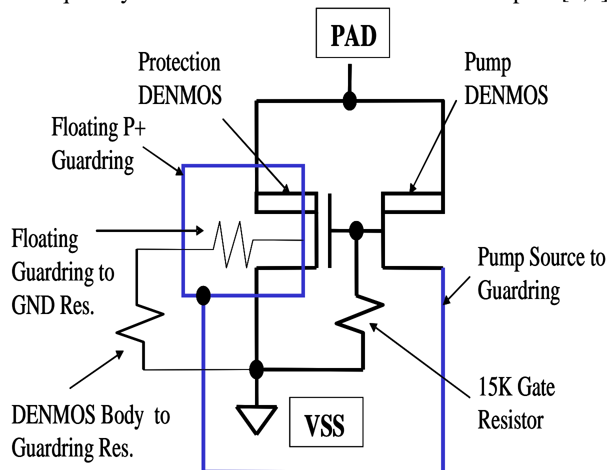

Fig1. Schematic showing biased and Substrate Biased High Voltage Protection Cell

Sequential turn-on of the bipolar and its transition from surface to bulk bipolar eventually triggers localization at the edge of the drain contact (fig. 2). More-over, the turn-on behavior of an array of 2D planar bipolar transistors triggers the onset of filamentation which leads to 3D localization (fig. 3) [4-10]. It is activated *first* (i) by the space-charge modulation of holes near the pinch-off region (-the 1st snapback) and *subsequently* (ii) by regenerative avalanche injection (-the 2nd snapback - phenomenon similar to 1D effect- base-push out effect) (fig. 1) [2-15].

Further-more, the non-linear physics behind the filamentation involves complex interaction between the circuit and the device, which leads to thermal runaway as it triggers dumping of stored inductive energy in a localized area of the silicon (fig. 3). Ultra-fast electo-thermal interaction, which involves self heating due to the scattering limited transport of carriers in the device, triggers decay of current in the protection circuit across the inductive load, comprising of package inductance[8,10]. The maximum temperature (T_{max}< 1687) determines the safe area of operation of the protection element (fig. 3) [10].

In-short, the electro-thermal runaway due to localized heating effects can be summarized through a (safe operating area) SOA window, in which the bipolar turn-on which reduces the margin of SOA and one can prevents an early filamentation by preventing regenerative bipolar turn-on (fig. 4) [3].

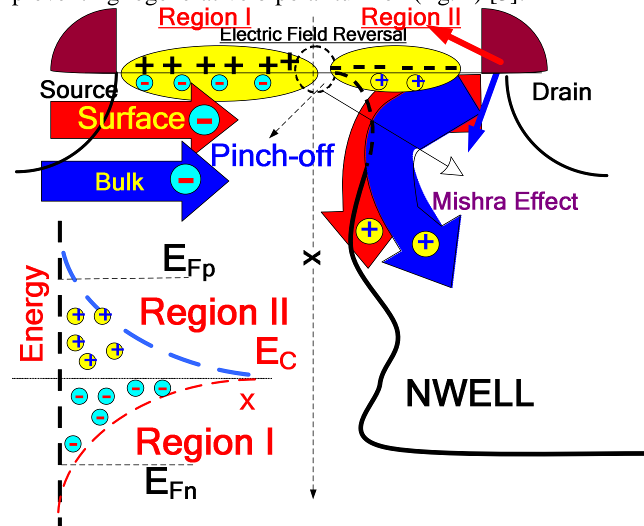

Fig 2 Twin paths of electron injection. *Bipolar turn-on and Electrostatics* near the pinch-off characterize

Therefore, full scale chip level simulation of filamentation in the ESD protection devices across the chip should be based on extraction of physics based scalable compact models for studying the circuit and device interaction during filamentation [16]. Now, understanding the subtle implications of biasing on the 2D electrostatics and its impact on the holistic 3D physics is critical for such an extraction methodlogy [4]. In this work, we revisit the physics behind bipolar snap-back and co-relate the damage due to 3D localization. Further-more, we investigate the high current

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behavior due to gate and substrate biasing in an optimized N-WELL structure.

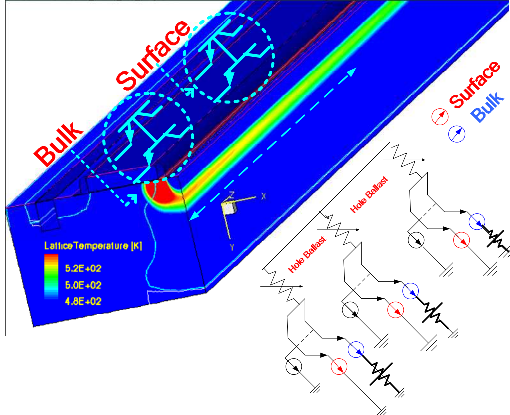

Fig . 3. Physics of 3D localization showing improvement under biasing. *Bipolar process can be explained due to activation of surface bipolar and subsequent movement to bulk*

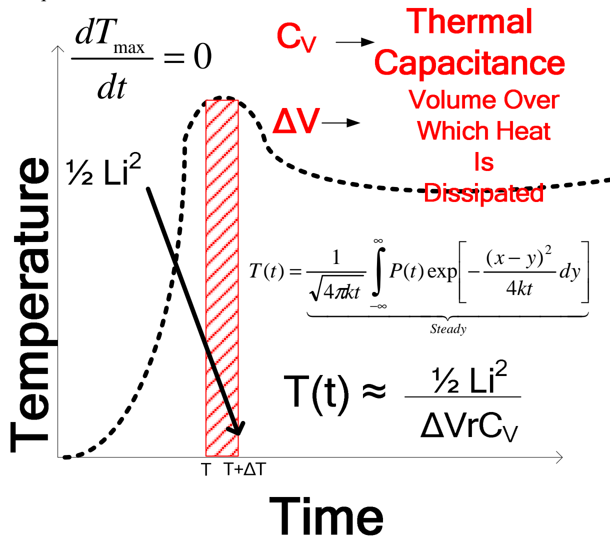

Fig.4 Peak temperature related to 2D and 3D localization. Stored *inductive energy* dissipated over *localized volume.*

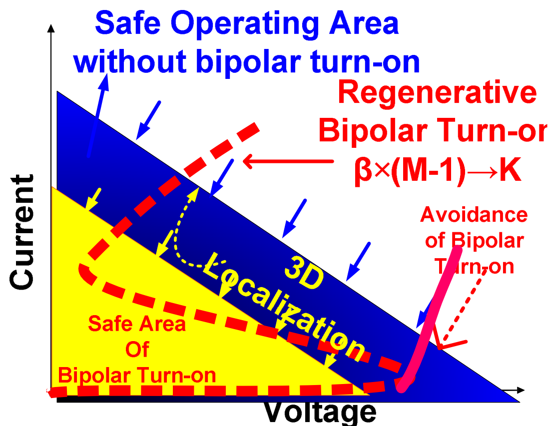

Fig. 5 Safe Area of bipolar turn-on. However beyond the *safe area of turnon*, bipolar snapback triggers strong *3D localization due to* Electro-thermal Instability.

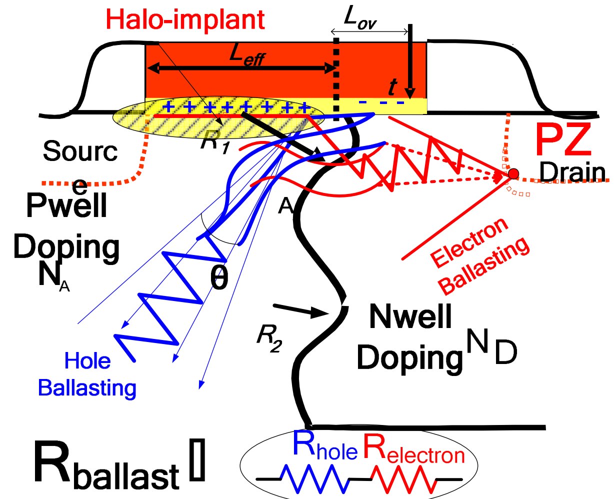

Fig.6 Current crowding of holes and electrons leads to *formation of ballast*

II. Electrostatics Of 2D Current Crowding Near Pinch-Off

A. Role of E-field polarity & Chanel Electrostatics Near the Pinch-Off under high current injection

Now, the fundamental understanding of snapback in the FET structures is related to the fact the holes are first attracted towards the gate around the pinch-off near the drain region. As the direction of electric field flips, it causes the holes to crowd, which is subsequently pushed towards the substrate – '*Mishra Effect*' [3]. Therefore, the buildup of potential prior to the first bipolar snapback can be explained primarily due to flow of holes (fig. 6) across the substrate and the regenerative high current physics of the parasitic bipolar is largely determined by the substrate resistance (the p-well implant N_A) (fig. 5) and the turn-on behavior is related to ambi-polar current flow [16].

B. Physics of High Current Ballasting Effect- Holes near Pinch-off & Electrons near the drain contact

Therefore, the current crowding phenomenon leads to current-controlled buildup of voltage, which determines the ballasting behavior in the high current regime (as the device exhibits resistive features) (fig. 6). The ballasting behavior is initially due to *2D phenomenon* in the array of planar bipolar and subsequently, the in-homogeneity spreads across the 3D. Also, the 2D electrostatic coupling under the gate is determined by the background doping concentration across the *surface*, which critically influences the microscopic-features of bipolar snapback (figs. 2 & 6). The DeNMOS can be *drain engineered* to tune its bipolar snapback features and thus filamentation behavior under an ESD event.

One way of targeting, the *drain engineering* across the HV - NWELL in the drain extended NMOS device, is through the optimized overlap of the gate and the NWELL, which also impacts the RESURF (fig. 6). By cleverly designing, the well overlap one can regulate the flow of avalanche generated carriers which as discussed earlier *controls the snapback features*. The peak electric-field established at sharp

curvatures across the N-WELL profile due to the implants plays a critical role in determining the breakdown features of the device. More-over, the charges imaged by the gate and the body determine the peak electric field both at the gate edge and within the body [1-4].

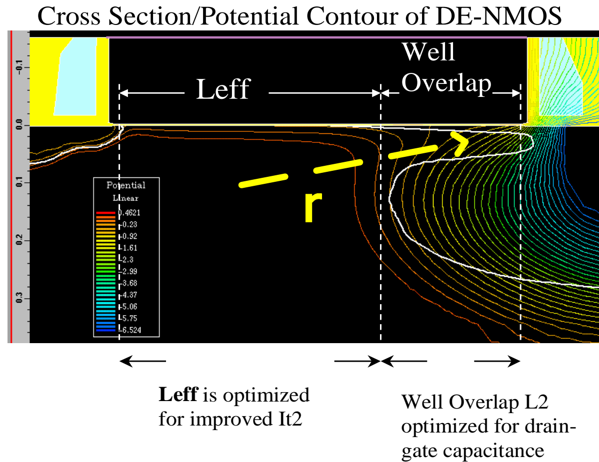

Fig. 7 *Optimized N-Well* overlap to control the ambipolar flow of avalanche generated carriers near the surface

Furthermore, the halo-implant impacts the surface bipolar turn-on by controlling the electrostatic coupling near the source region. It also determines the curvature of Drain-Substrate junction i.e (r) (fig. 6 & 7) near the surface which subtly controls the flow of avalanche generated carriers below the oxide in the drain and side wall overlap (fig. 2 & 7).

III. Electro-Thermal Instability Induced 3D Localization - Triggering RandoM & Anamolous Behavior

An early regenerative bipolar turn-on across the 2D array of planar bipolars in principle should weaken the localization during the 1st snapback, further-more the electron current crowding at the drain contact leads to ballasting behavior (fig. 3). Now, the 3D ballasting limits the short circuit current under snapback; this helps to alleviate the 3D localization and prevents the regenerative avalanche injection related to 2nd snapback at the drain contact [7,8]. Interestingly, while the non-ohmic drop (i.e *ballasting effect*) stabilizes the current in the protection circuit, the device failure can also related to localized, J.E heating at the drain contact due to the same ballasting action.

Dies– D3, D4, D5 fails due to *first snapback* through regenerative bipolar turn-on, while Dies- D1 & D2 survives the 1st snapback as exhibited by characteristic jump in the I-V curve (fig. 8). In fact, D2 exhibits an anomaly showing even *delayed bipolar turn-on* can sometimes be efficiently controlled – demonstrating the unpredictable or *chaotic* nature of the failure mode. In short, the highly sensitive process of filamentation, which is based on the positive feedback mechanisms leads to variations in the failure current that can be explained both due to electro-thermal origin and coupled electrostatics near the pinch-off region (fig. 2-3).

More-over, the devices show variations in slope, which can be also be explained due to intrinsic ballasting action (fig.3) and is related to an extent of bipolar turn-on across the surface and in the bulk (fig.2 & fig.6). Eventually, the failure of the device is ultimately related to catastrophic 3D current localization triggering the 2nd snapback - where-in the location of hot spot is determined by the peak E field at the edge of drain contact (PX) due to high electron current density (fig. 3) [16].

IV. Impact Of Biasing On Slope – Achieving Uniformity Of Ambipolar Current Flow

To summarize, the discussions, intricacies behind the snapback features and 3D localization can be related to both (a) accumulated space charge of *holes* near the surface and (b) *electrons* within the bulk at the edge of drain contact (fig. 3) as the bipolar activity is pushed into the bulk, which is influenced by gate and substrate biasing (fig. 2 & fig. 6) [14,15].

Gate biasing influences both the ballast resistor, R_{hole} and $R_{Electron}$ (fig. 6) and by optimizing the curvature (r) (fig. 7) and suitably adjusting the coupled electrostatics through the gate and substrate biasing, one can efficiently regulate the high current I-V slope, while in the process, we control the ESD design window (Fig. 5-9). For a given substrate biasing, while the features of 1st snapback are missing, the I-V slope is marginally improved for the optimally built N-well structure (fig. 8) [16].

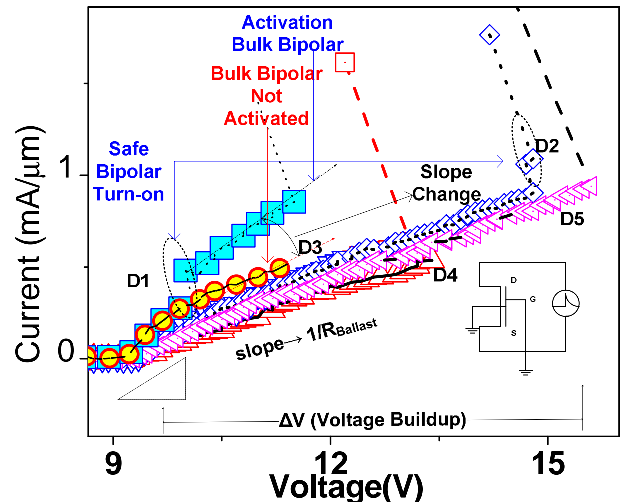

Fig. 8. TLP Data showing die to die variations some of the devices show snapback features (D1 & D2) marked by jump in I-V charecteristics, some fail early while others *exhibit voltage buildup* (ΔV) due to *current crowing* and eventually fail. I-V charecteristics show *change of slope* due to bipolar turn-on.

The gate biasing is known to improve and both degrade the performance of the second breakdown – (a) improvement is due to *uniformity in 3D current distribution* comprising of conducting array of planar bipolar, (b) degradation is due to *strong avalanche injection* at the drain contact. Further-more, the dual and conflicting role has been a design challenge under the gate protection, where the inability to correctly design the gate biased protection structure has impacted the device performance[7].

Further-more, steeper slope under the gate bias can be explained due to the uniform flow of ambi-polar current in the optimized structure, more-over, under these conditions there is a strong injection across the drain contact. Therefore, improving the flow of compensating am-bipolar carriers can lower the build-up of potential across the device. The critical feature for this optimal N well structure is that under a high gate bias (which is very often known to degrade the ESD performance), not only *the failure performance* can be improved but also *the high current I-V slope* can be efficiently regulated (fig. 9). The substrate bias while it reduces the avalanche injection across the drain region, it prevents the filamentation, where by it can impact the flow of holes into the substrate.

	Improvement ↑	Degradation ↓
Substrate Injection	Injection at Drain Contact	Impacts the Slope
Gate Biasing	3D Uniformity of 2D Bipolars	Strengthens Injection at Drain Contact

Table I. Comparison of performance between Gate Biasing and Substrate Injection

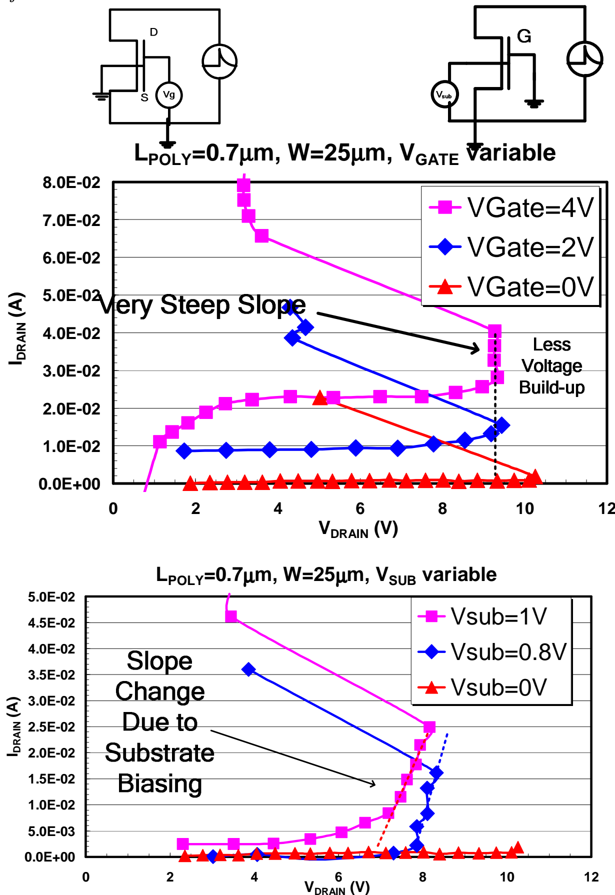

Fig. 9. a) Gate Biasing of DeNMOS. Flow of holes and electrons can be efficiently alleviated to improve it2 & high current I-V charecteristic showing *very steep slope* due to *ambipolar accumulation* of carriers. b) Substrate Biasing of DeNMOS. Substrate biasing *delays the second- snapback*.and impacts the slope.

V. CONCLUSION

We have investigated the snapback features as the parasitic bipolar turns-on and the implication on 2D electrostatics and 3D electro-thermal instabilities. We show that gate coupling can be optimized to enhance the failure performance as we analyze the electro-thermal trade-off to understand improved ESD performance.

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