GaN MOSFET: Projections for High Power High Frequency Applications

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Abstract—**It is well known that GaN has superior properties for the potential of producing a high frequency, high power device for use in millimeter wave technology. Currently, GaN based devices have been limited by the inability to suppress gate current sufficiently to allow for large gate charge and gate electric fields. The limitations on the perpendicular electric fields subsequently prevent the degree in which the devices gate length can be scaled without early breakdown and premature saturation of cutoff frequency. A suitable gate oxide is presented with the calibrated projection of the GaN MOSFET and the GaN HFET for small gate lengths. The GaN MOSFET structure shows a considerable advantage (f_t*Breakdown Voltage>10X) compared to the HFET largely because the superior charge control in the channel of the device. By reducing to a smaller gate length the resulting cutoff frequency of the device is improved. Through the use of a GaN MOSFET structure, the desire for high power and frequency applications is possible.**

Keywords- Breakdown Votlage; High power; High Frequency; GaN MOSFET; GaN HFET

I. INTRODUCTION

GaN based devices have shown to be the potential solution for high-power electronics for high frequency applications. Currently GaN HFET structures are extensively researched to improve the performance and high frequency capabilities of the devices [1]-[8]. However, complications have begun to arise from short-channel effects when reducing the gate length in HFETs [9]. By maintain an effectively thick barrier to produce the 2 dimensional electron gas (2DEG); the overall maximum frequency does not improve as the gate length is reduced. This limits the switching frequency of current GaN based devices.

With the recent advancements in growing improved gate dielectrics on GaN [10], the GaN MOSFET architecture has the potential to surpass current technology due to the enhanced electric field allowed in the channel. By having the capability to scale the gate oxide thickness with gate length, the MOSFET structure will have the capability to withstand early breakdown effects compared to the HFET. In this paper, we present the potential projections and limitation of the device structures to achieve large breakdown voltages and high switching frequencies.

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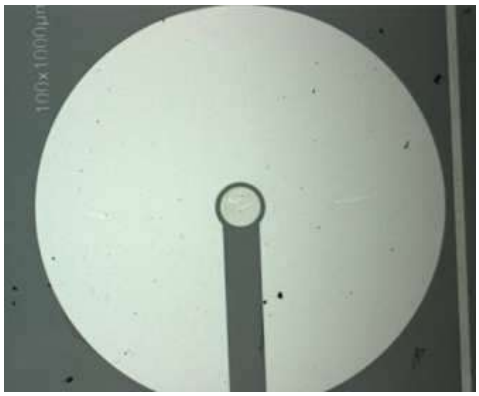

Figure 1: Examine of the planar GaN MOSCAP structure that was used to calibrate the simulation models.

II. CALIBRATION OF MODELS

The models and simulations of the devices were conducted with the commercially available microelectronics simulator Sentaurus TCAD. Various MOSCAP test structures (Figure 1) were fabricated and used to calibrate the material parameter files prior to the simulations. Through the collection of capacitance vs. frequency measurements for a series of simple test devices we were able to extract C-V plots (Figure 2) and compute the effective mobility for varying electric fields. The mobility/capacitance extraction provided consistent results on two layers of high-k oxide thicknesses deposited on GaN for device geometries ranging from 25μm to 200μm [11]. Leakage current (Figure 3) was significantly less than 1A/cm^2 for all test conditions (<2.5 V).

Through the extraction method discussed in [11] we were able to determine the effective channel mobility, as shown in

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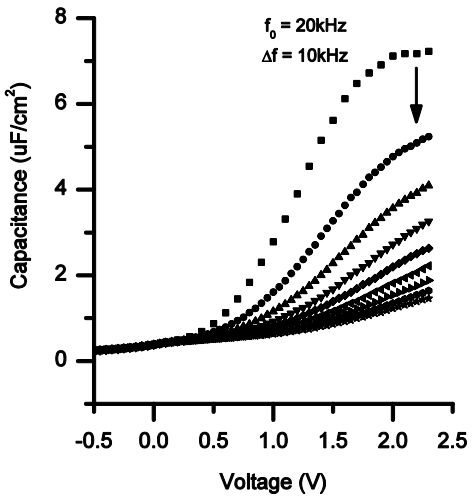

Figure 2: Capacitance measurements used to calibrate the simulation models.

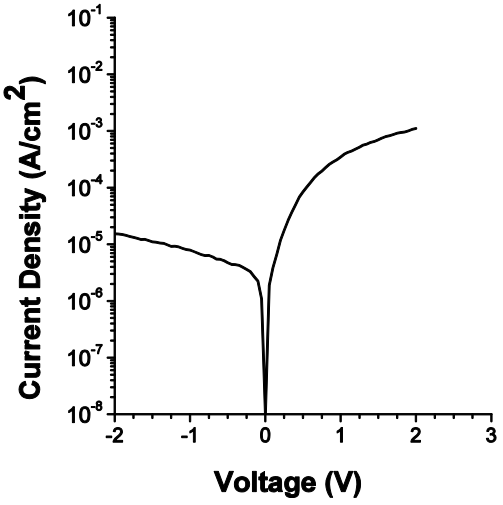

Figure 3: Current characteristics used to calibrate the simulation models and interface quality of the MOS structure.

Figure 4, which was used to confirm and calibrate the Synopsys TCAD files of the optimized GaN MOSFET [12] with the extracted channel mobility from the MOSCAP. The Synopsis simulations were cross calibrated with several HFETs that were available in the literature [13]. The resulting mobility vs. electric field curves were in agreement with the nature of GaN universal mobility curves, which is normally reported for silicon devices. Other than the use of the high-k gate dielectric compared to the AlGaN layer, the field plate architectures were not varied for this simulation study.

To improve the unity gain frequency of the devices, we reduce the gate length to sub 0.1um scales. The simulations are examined at gate lengths of 100nm, 50nm and 25nm for both the MOSFET and HFET. Field plate structures that were optimized for the MOSFET and HFET remained constant throughout the scaling of the devices. This reduced the peak electric fields along the gate-drain region to maintain a larger breakdown. In addition the gate-drain lengths were 8um to enhance the effect of the field plates to allow for the possibility of much larger breakdown voltages in the MOSFET. Furthermore, the MOSFET was simulated with a 3nm oxide and 0.75nm equivalent SiO_2 gate dielectric thickness. This is consistent with an 18nm and 3nm high-k, $\varepsilon_r = 24$, gate dielectric which was comparable to the dielectric thicknesses used to evaluate the interface quality of the oxide and semiconductor [14].

During all of the simulations, the GaN HFET barrier thickness was held constant thickness in order to maintain leakage current at the gate. By nature the MOSFET structure has the capability to simply scale the oxide thickness with the gate length. However, the AlGaN barrier of the HFET is required for all gate lengths since a minimum thickness is needed to maintain the 2DEG.

III. Simulation Results

Upon simulating the devices we extracted the results and compared the device characteristics of the GaN MOSFET and the AlGaN/GaN HFET. To examine the device characteristics for high frequency and high power application, we compared the drain current density versus drain voltage and the transconductance versus gate voltage plot to determine the quality of operation and potential capabilities. Figure 5, confirms that HFET IV characteristics, based on the transconductance, are degraded for gate lengths smaller than

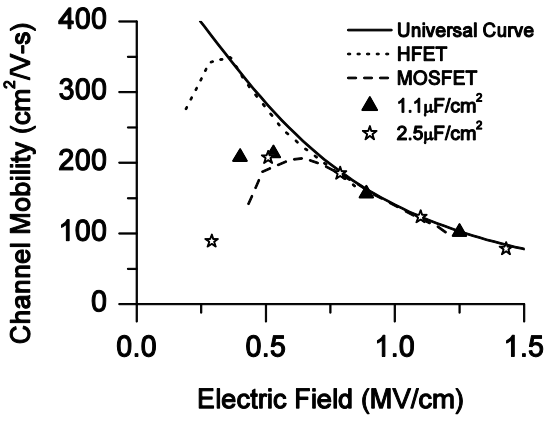

Figure 4: Simulation mobility calibrated to the extracted effective channel mobility of the fabricated test devices. The results follow the universal effective channel mobility for GaN [10].

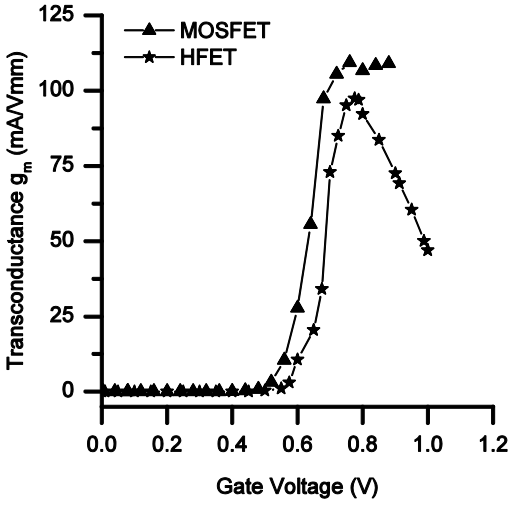

Figure 5: Simulated transconductance (g_m) for the MOSFET and HFET with 50um gate lengths.

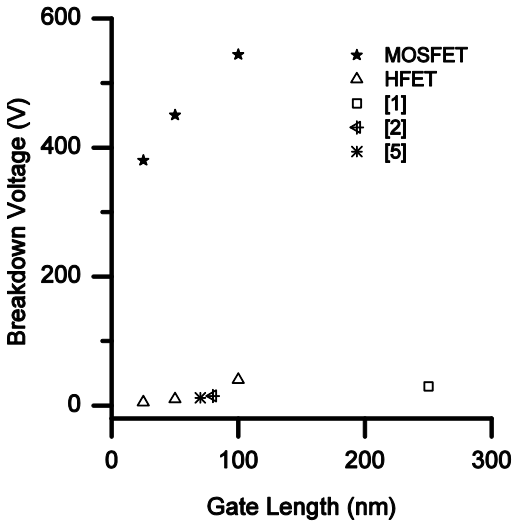

Figure 6: The breakdown voltage versus gate length of the simulated MOSFET and HFET devices compared to current fabricated HFETs.

50nm when compared to the MOSFET. The MOSFET is able to control the channel as the device is scaled down past 50nm. The transconductance of the MOSFET maintains a nearly constant value as gate voltage increases. Conversely, the HFET is not capable of preventing current collapse phenomena, which is why the transconductance decreases as gate voltage is increasing. As the gate length is reduced the MOSFET is capable of suppressing the charge under that gate, whereas the HFET is unable to control the 2DEG in the channel. Due to lack of controllability at such small gate lengths, the HFET will breakdown early while the MOSFET is still capable of producing a family of curve characteristics. This confirms that the device characteristics of the MOSFET exceed the HFET as we scale the devices. Furthermore, the breakdown voltage (Figure 6) for the optimized GaN MOSFETs is able to withstand voltages up to 550V before breaking down due to impact ionization under the gate. We observe that the design structure of the MOSFET is capable of withstanding early breakdown effects compared to the HFET. This allows the MOSFET to continue to operate at lower gate lengths whereas the HFET is not capable of producing characteristics required for high power applications.

A major improvement as gate length is scaled, is the unity frequency gain, shown in Figure 7. The frequency gain increases to a maximum of 540 GHz for the MOSFET as the gate length is scaled from 100nm to 25nm. This was achieved by scaling the oxide thickness with the gate length. By concurrently scaling the gate length and oxide thickness we are capable of improved control of the channel under the gate. Conversely, the unity gain frequency drastically saturates in the HFET as the gate length is scaled down. This agrees with Jensen [9], that there is a fundamental limit where the frequency gain of the HFET will stop increasing as the gate length is reduced for a given barrier thickness. Since, the barrier thickness of the HFET is required to maintain a minimum thickness to produce the 2DEG. The HFET will not be able to control the channel when the gate length is scale down. This prevents the HFET structure from improving unity gain frequency compared to the optimized MOSFET, shown in figure 7.

For high power and frequency applications, the breakdown voltage and unity frequency gain are two of most important

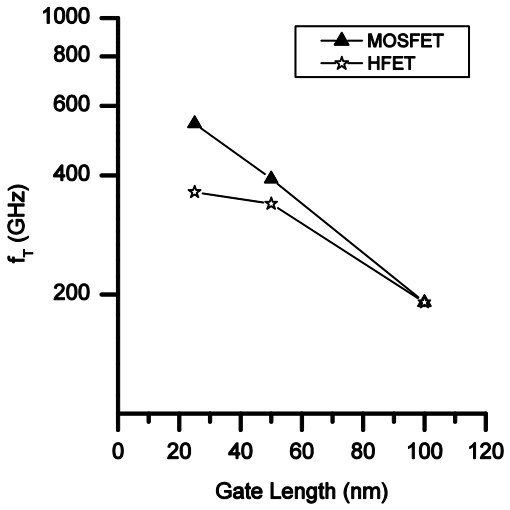

Figure 7: Unity gain frequency comparison for the optimized MOSFET and HFET

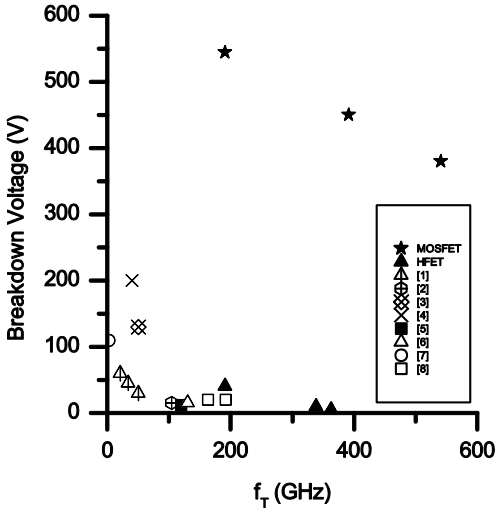

Figure 8: Breakdown frequency compared to unity gain frequency for current technology and the simulated devices.

factors for device characteristics. Figure 8 summarizes the primary outcome of this simulation study that is based on an experimentally obtained high-k dielectric on GaN projections and contrasts this with experimental values found in literature. The availability of the low defect density high-k on GaN gate dielectric system on GaN used to make these projections will enable the construction of GaN MOSFETs with breakdown voltages in excess of 500V and cutoff frequencies larger than 550GHz. The MOSFET structure is capable of reaching the theoretical limit for GaN-based devices whereas the HFET has many fundamental complications that arise when scaling the devices. The projections made in this work suggest that GaN MOSFET structures can provide a high power source solution for mm-wave applications.

IV. Conclusion

A cross calibrated TCAD from experimental high-k on GaN and literature obtained HFET data was used to project the capacity of GaN MOSFETs compared with GaN HFETs. The f_T*BV product was greater than 10x for MOSFET compared with HFET. This was largely resulting from the reduction in electron density during the depleted state as well as the superior channel control from the thinner gate dielectric. This also is an inherent enhancement mode structure, which also significantly increases the range of applications that the studied device can be used for.

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