Improvement of Drive Current Prediction in FinFET using Full 3D Process/Stress/Device Simulations

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***Abstract*—In this work, a 3D process and device simulation study of FinFET devices is reported. Mobility models on (100) and (110) surfaces are first calibrated to planar data and the stress dependence is calibrated to both through-Lgate and wafer-bending data. Surface orientation dependent mobility models are then implemented for FinFET simulations to improve drive current predictions. The simulated 3D stress is integrated with doping profiles as input to the device simulations. Full flow FinFET simulation results show good agreement with experimental data in terms of stress induced Ion gain and Vt shift. It is observed that the channel mobility in FinFET is higher than that of the planar devices due to lower transverse electric field.**

Keywords-surface orientation; mobility; FinFET

I. INTRODUCTION

Multiple-gate MOSFET is widely recognized as one of the most promising candidates for further scaling of CMOS technology, due to its excellent SCE and surface orientation mobility enhancement. Several researchers have presented modeling of multi-gate devices [1-4]. In ref. [1,3,4], FinFETs are modeled as double-gate devices; the top surface conduction is ignored, therefore, only a single mobility on one surface orientation is considered. Ref. [2] included the contribution of top surface conduction by two different orientation dependent mobility models, however, only at zero stress conditions. This paper presents a FinFET modeling methodology, which integrates full 3D stress and doping profile simulations, with 3D device simulations using strained orientation-dependent mobility models.

The FinFET channel region is divided into sub-regions with (100) and (110) surface orientations. For each sub-region, a proper mobility model corresponding to its orientation is selected. The (100) and (110) mobility models are first calibrated to measured planar device data from TCAD experiment wafers. Band structure based mobility calculations are then used to extend the models to stress levels beyond these of calibration devices. The strained mobility gain of holes on (100) is shown to be higher than that on (110), and the mobility crossover is found at channel stress levels beyond 3Gpa, consistent with that reported in ref. [5]. FinFETs manufactured with different stressors are simulated, and good agreement with data is observed. Study also shows that the FinFET mobility is generally higher than that of planar device due to its lower channel electric field under the same gate bias.

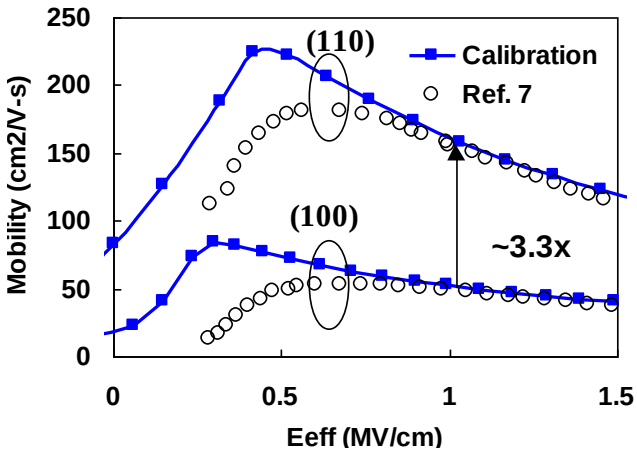

Fig.1 The calibrated unstrained hole mobility for (110) and (100) surfaces from planar devices. Literature mobility data [7] is also shown for comparison.

II. MODEL CALIBRATION AND IMPLEMENTATION

For (100) surface orientation, a six-band k•p strained mobility model for holes and a piezoresistive mobility model for electrons, as described in ref. [6], are selected. For (110) surface orientation, piezoresistive mobility models are selected for both electrons and holes. The TCAD decks are first tuned to match Vt/DIBL of planar devices from calibration wafers, from long to short channels, to ensure accurate capture of doping profiles and strain induced Vt shift. The mobility and its stress dependence are then extracted through I-V curve calibrations at different gate lengths. As shown in fig. 1, the unstrained hole mobility for (110) is ~3.3 times of that for (100), which is similar to most literature reports [5,7].

The strain dependent band warping induced effective mass change plays an important role in orientation dependent hole mobility.

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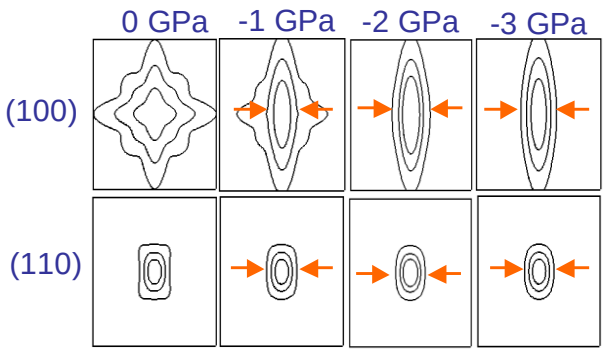

Fig.2 (a) The energy dispersion of first sub-band for (100) and (110) surfaces under <110> compressive uniaxial stress.

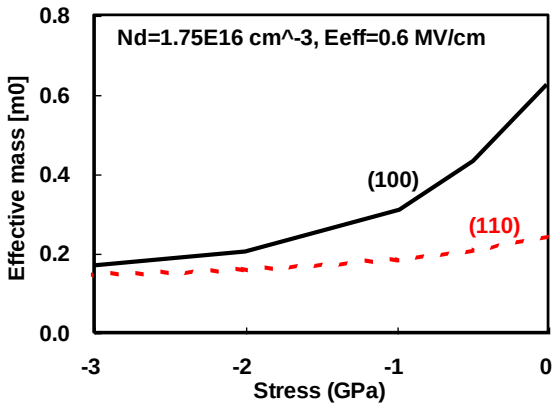

Fig.2 (b) The average effective mass (weighted with carrier occupancy) changes due to stain.

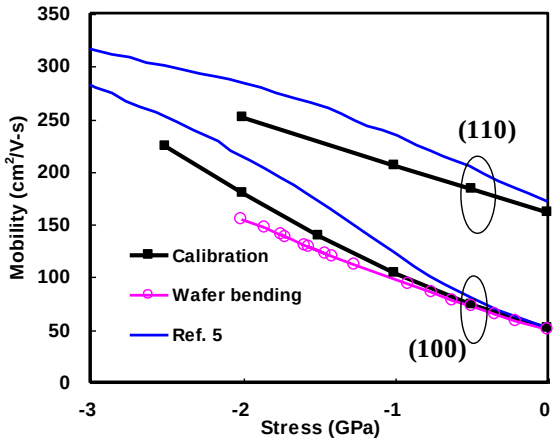

Fig.2 (c) PMOS strained mobility for (100) and (110) surfaces from wafer bending data, calibrations, and literatures[5].

Six-band k•p calculations have been carried out. The constant energy contours of the 1st subband for holes on (100) and (110) surfaces with compressive <110> uniaxial stress from 0 to 3GPa are shown in fig. 2(a). The corresponding hole effective mass changes due to stress induced band warping is shown in fig. 2(b). The unstrained hole effective mass on (110) surface is much smaller than that on (100) surface, which explains the experimentally observed higher unstrained hole mobility on (110) surface. However, the band warping on (110) surface is less significant under same applied compressive stress than that on (100). Therefore, a smaller reduction in effective mass under same stress is expected on (110) than on (100). This is reflected in the smaller mobility versus stress slope for (110) than that for (100), as can be seen in fig. 2(c). However, since the large mobility difference at zero stress between (100) and (110) surface orientations, no mobility crossover is observed at stress level below -3Gpa. The strained hole mobility gain slopes are further validated by wafer bending data, as shown in fig. 3.

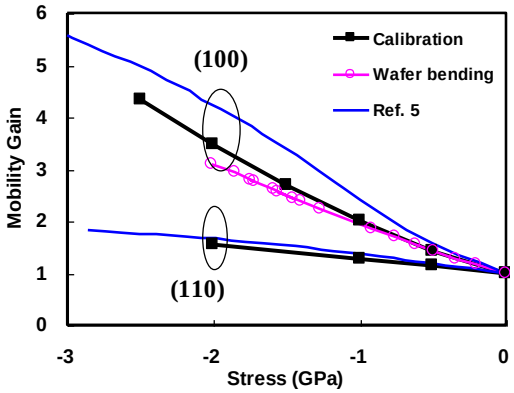

Fig.3 PMOS strained mobility gain for (100) and (110) surfaces under <110> uniaxial compressive stress.

Similarly, electron mobility stress responses for (100) and (110) are extracted and illustrated in figs. 4-5. Theoretically, since the 1st sub-band in the inversion layer for (110) is located in Δ4 valley, while for (100) in Δ2 valley, the electron effective mass along <110> direction for (110) wafer is larger than that for (100), and the resulting electron mobility for (110) is lower than that for (100).

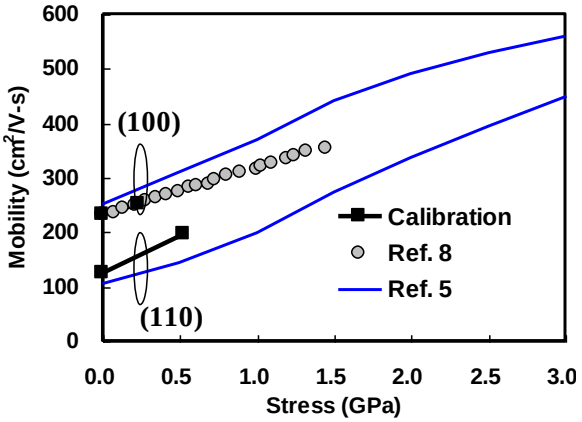

Fig.4 NMOS strained mobilities under <110> tensile stress for (100) and (110) surfaces from wafer bending, calibrations, and literature[8].

When tensile <110> uniaxial stress is applied, the valley minimum of Δ2 moves lower relative to Δ4 on (100) surface, causing increased electron occupancy of Δ2 which has lower transport effective mass. Because electrons on (110) surface initially occupy mainly in Δ4 valley at zero stress, the effective mass change is larger under stress when electrons increasingly

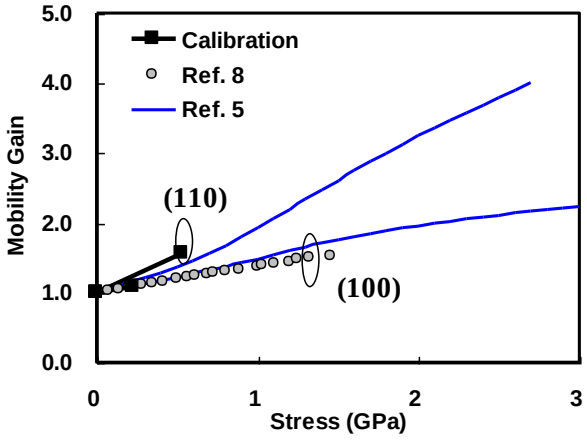

Fig.5 Experimental and theoretical NMOS mobility gain under <110> uniaxial tensile stress.

occupies Δ2, than that on (100) surface where electrons already has partial occupancy in Δ2 valleys under zero stress. Consequently, the mobility stress gain slope on (110) surface is greater than that on (100) as illustrated in fig.5. The electron mobility extracted from calibration confirms the theoretical expectation, and also agrees with literature reported wafer bending data [8].

III. FINFET SIMULATION RESULTS

The FinFET channel region is divided into two sub-regions with (100) and (110) surface orientations, as shown in fig. 6. The channel stress generated from 3D FAMMOS [9]

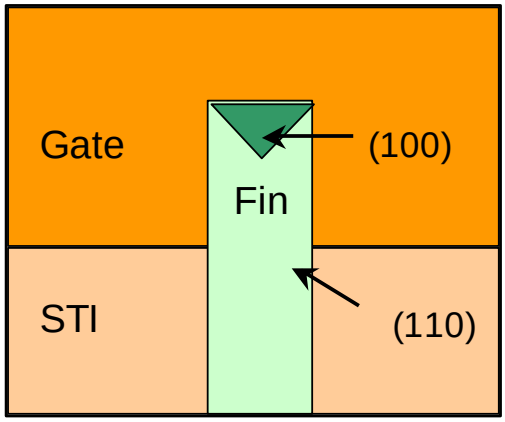

Fig.6 Schematic diagram of FinFET structure. The channel region is divided into two sub-regions with (100) and (110) surface orientations.

simulations and doping profile generated from 3D Sprocess [10] simulations are integrated together in 3D Sdevice [11] to obtain accurate drive current predictions. N/P-FinFET experiments with two different stress film thicknesses and two different Ge

P-FinFET (Lg=35 nm)				
Ge (%)	A'		B'	
	Data	Simulation	Data	Simulation
ΔVtlin (mV)	Ref.	Ref.	24.9	30
ΔVtsat (mV)			20.7	29
ΔIdlin (%)			-9	-7.4
ΔIdsat (%)			-9.1	-12.9
N-FinFET (Lg=35 nm)				
CESL thickness	A		B	
	Data	Simulation	Data	Simulation
ΔVtlin (mV)	Ref.	Ref.	19.4	13
ΔVtsat (mV)			16.2	13
ΔIdlin (%)			-6.8	-5.7
ΔIdsat (%)			-8.3	-7.7

Table 1 Comparison of simulation results with measurement data. P-FinFET's with different Ge % (A'>B') and N-FinFET's are manufactured with different CESL thickness (A>B).

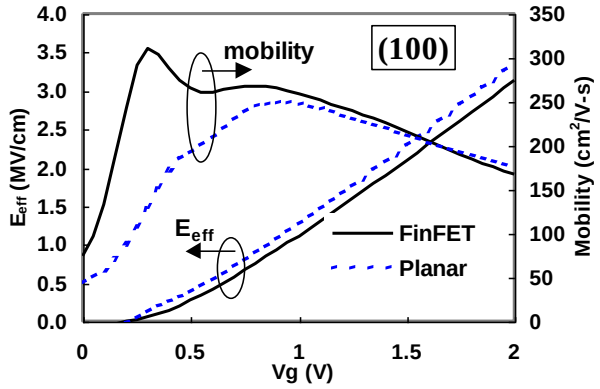

Fig.7 (a)

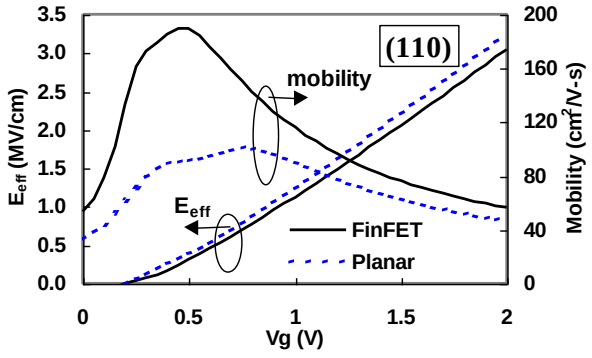

Fig.7 (b) Comparison of Eeff and mobility between Planar and FinFET at the same gate bias for (a) (100) surface and (b) (110) surface. FinFET shows lower electric field in the channel than planar device, thus has less mobility degradation.

mole fractions are simulated to validate the model. The simulation results shown in table 1 are quite consistent with measured data without any additional parameter adjustment. The simulations also show good agreement with strain induced Vth shift and Id gain. The vertical E-field and mobility versus gate bias for N-FinFETs and planar devices are compared in fig. 7. It is observed that FinFETs have higher mobility than that of planar devices, due to the lower transverse E-field in FinFETs resulted from the double gate configuration.

IV. CONCLUSIONS

In this article, a physical based FinFET TCAD modeling methodology is presented. Surface orientation and stress dependent mobility models are extracted based on calibration to planar device data. The strained hole mobility gain slope and (110)/(100) mobility cross over point are established. Simulations of FinFET devices demonstrate good agreement with data and with strained Vt shift and Id gain. It is also observed, that impact of lower (110) electron mobility on FinFET performance is smaller than that on planar devices due to the lower transverse E-field in FinFET.

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