3D simulations of random dopant induced threshold voltage variability in inversion–mode $In_{0.53}Ga_{0.47}As$ GAA MOSFETs

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***Abstract*—A study of random dopant fluctuation effects in a 50 nm gate length inversion–mode $In_{0.53}Ga_{0.47}As$ gate–all–around MOSFET is carried out via an in–house parallel 3D finite–element drift–diffusion device simulator with quantum corrections. Quantum confinement effects are taken into account through the density gradient approximation meticulously calibrating carrier density in the channel cross-sections against a 2D Schrödinger-Poisson solver. Then, the I_D–V_G characteristics obtained from the quantum corrected 3D simulations are validated against experimental data and the variability study is performed. The results show a significant reduction in the variations of threshold voltage with a spread of only 5.9 mV as well as in the threshold voltage lowering when compared with bulk Si MOSFETs.**

***Index Terms*—random dopants; threshold voltage variability; drift–diffusion; density gradient; III–V materials; gate–all–around MOSFETs**

I. Introduction

High mobility channel n-type MOSFETs based on III-V semiconductors are very promising candidates for digital applications [1] aiming for the sub-16 nm Si CMOS technology. The high electron mobility and overall low effective mass in III-V materials can result in a very high injection velocity delivering a high device performance and a very large switching speed at a low supply voltage [2]. The introduction of III-V semiconductors into Si CMOS technology requires transistor architectures which can take a full advantage of the high mobility and injection velocity into channel thus simultaneously neutralising some of the potentially detrimental effects [3] related to a lower density of states when compared to Si. On top of that, carriers in the channel have to be very well controlled by the metal gate. This calls for thin-body device architectures which are feasible within III-V based heterostructures. However, the gate control offered by the thin-body architectures is not sufficient for the sub-16 nm Si CMOS technology low leakage current requirements and thus the solutions based on non-planar technology using a gate–all–around (GAA) approach might be needed.

Recently, one of the first inversion–mode $In_{0.53}Ga_{0.47}As$ GAA FinFET by a top–down approach with atomic–layer deposited Al_2O_3/WN gate stacks have been demonstrated [4]. These demonstrations represent a significant step in technology development of III-V channel FinFETs and allow for a start of studies on device variability. Since the variability effects are recognised as one of the main limiting factors for nanoscale scaling of devices, these new device architectures should be assessed for their variability behaviour in typical working conditions. In this work, we first investigate the impact of random dopant fluctuations on the threshold voltage of the device because the random dopant fluctuations are one of the most important sources of variability in conventional MOSFETs [5]. The improved electrostatic integrity of GAA FinFETs promises to reduce the impact of the random dopant induced threshold voltage variations on the performance and reliability of the device. We have studied the threshold voltage variability due to the presence of random discrete dopants in the n-type doped source/drain regions and p-type doped channel of a 50 nm gate length $In_{0.53}Ga_{0.47}As$ GAA MOSFET. We have employed a parallel 3D finite–element (FE) drift–diffusion (DD) device simulations with extensively calibrated quantum–corrections. This paper is organised as follows. Section II introduces the basic features of our 3D DD device simulator. The device structure and the calibration of the simulator against both Silvaco simulations and experimental data are presented in Section III.A. The simulated variability in the threshold voltage is presented in Section III.B. Finally, Section IV summarises the main conclusions of this work.

II. 3D finite–element quantum–corrected drift–diffusion device simulator

The random dopant induced variability is studied in an inversion–mode GAA $In_{0.53}Ga_{0.47}As$ MOSFET using a 3D FE quantum–corrected DD device simulator [6]. The quantum effects have been incorporated using the implementation of the FE density gradient (DG) approach described in [7]. We have employed a very fine unstructured tetrahedral mesh, generated by the Gmsh software [8], which is appropriate for the study of intrinsic parameter fluctuations. The 3D FE DD simulator has been fully parallelised using MPI in order to reduce the

 ISBN 978-0-615-71756-2

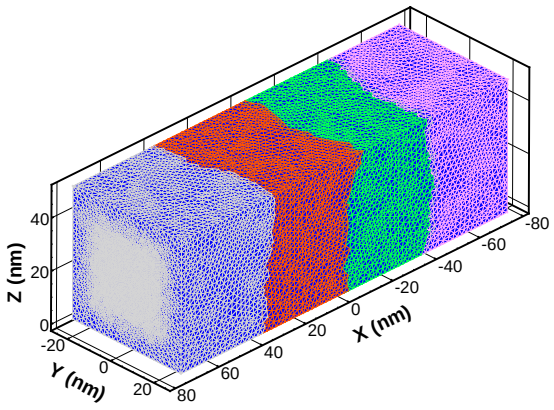

Fig. 1. Tetrahedral mesh of a 50 nm gate length $In_{0.53}Ga_{0.47}As$ GAA MOSFET divided into 4 subdomains.

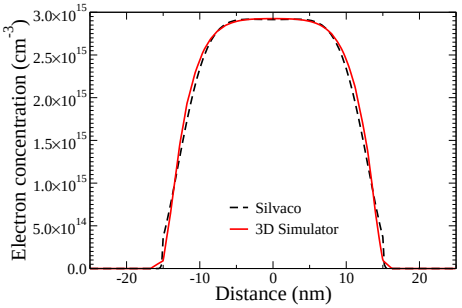

Fig. 2. Comparison of the electron concentration in the middle of the channel of the device obtained from the 3D simulator and the 2D Schrödinger solver at $V_G = -0.9$ V.

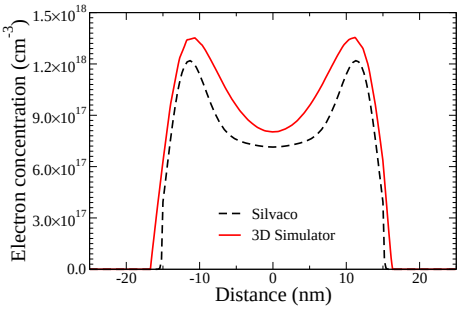

Fig. 3. The same as in Fig. 2 but at $V_G = -0.5$ V.

memory requirements and to save computational time. We have used the METIS program [9] to partition the mesh among the available processors. Fig. 1 shows the tetrahedral mesh used in this study divided into 4 subdomains. This mesh has 337,099 nodes and 2,128,612 elements.

The DD quantum corrected model implemented in the 3D simulator solves the Poisson, density gradient, and current continuity equations for electrons consistently with mixed Dirichlet, Robin, and Neumann boundary conditions. These discretised equations are first decoupled using the Gummel method [10] so that they can be solved sequentially. Then, each of these non–linear systems is linearised using the Newton–Raphson iterative method [11]. Domain decomposition methods [12] have been used to solve, in a parallel manner, the sparse linear systems arising from the linearisation of these equations. We have employed Krylov subspace iterative solvers (FGMRES or BiCGSTAB methods) [12] in order to obtain the local nodes within each subdomain. We have used an incomplete LU factorisation as a preconditioner which depends on both a numerical threshold and a certain level of fill–in (standard ILUT preconditioner).

III. Numerical results

In this section, we initially provide information regarding the structure of the $In_{0.53}Ga_{0.47}As$ GAA MOSFET and the calibration process carried out to validate our simulator. After that, we present the threshold voltage variability results.

A. Device structure and calibration process

The simulated device has a 50 nm gate lenght, an $In_{0.53}Ga_{0.47}As$ channel, p–doped at $2x10^{16}cm^{-3}$ with 30x30 nm^2 cross–section, a 10 nm thick Al_2O_3 encapsulation layer and 50 nm wide n–doped S/D regions. The modelling of the S/D Si implantation was performed at energy of 20 keV and a dose of 10^{14} cm^{-2}; the dopant activation at 600 °C for 15 s in nitrogen ambient. The doping profile was generated via the atomistic Monte Carlo simulation of ion implantation available in the Sentaurus Process [13], [14].

Initially, we calibrated the DG parameters used in our 3D DD–DG simulator against Silvaco's ATLAS 2D Schrödinger solver [15] across the middle of the channel at several gate voltages (-0.9, -0.5, 0.0 and 0.5 V). Figs. 2 and 3 show a comparison of the 1D electron concentrations along the y-axis obtained from the 3D DD–DG simulations and the 2D Schrödinger solver at gate biases of -0.9 and -0.5 V, respectively. The corresponding electrostatic potential is shown in Fig. 4. These results show that the DG approach allow us to accurately reproduce the shape of the electron density in the channel, especially at large negative gate biases. The electron effective masses in the $In_{0.53}Ga_{0.47}As$ region and in the oxide are used as calibration parameters and they were changed for different working conditions to accommodate the different qualitative characteristics of the electron distribution. Therefore, at a very low gate bias (such as -0.9 V), the electron effective masses were determined to be $0.014m_0$ in the x–direction and $0.041m_0$ in the y and z–directions and the effective mass for the oxide was set to $0.1m_0$. However, for larger biases (-0.5 V and above) the electron effective masses were determined to be $0.014m_0$ in the x, y and z–directions and the effective mass for the oxide was set to $0.2m_0$ clearly showing the calibration is not possible with a single set [16].

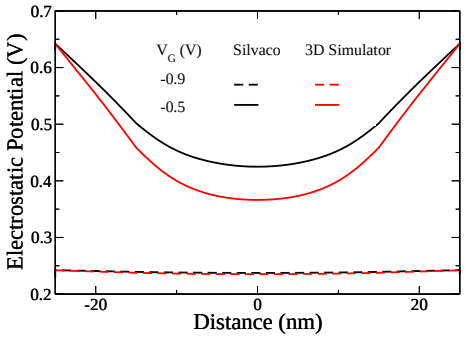

Fig. 4. The same as in Fig. 2 but at gate biases of -0.9 and -0.5 V.

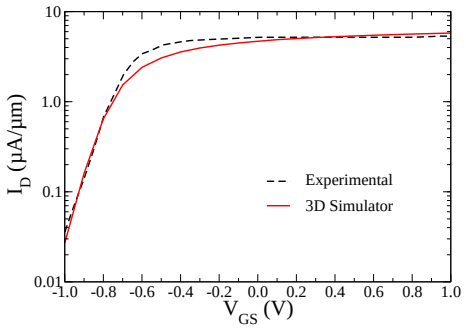

Fig. 5. Calibration of I_D–V_G characteristics obtained at a drain bias of 0.05 V for the 50 nm gate length GAA III–V MOSFET on a logarithmic scale. Results from the 3D DD–DG simulator are compared to the experimental data.

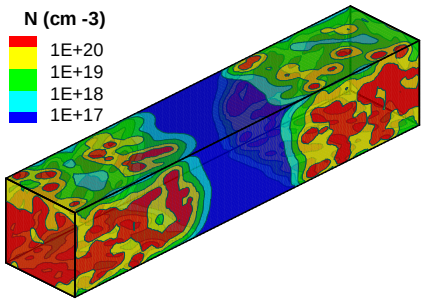

Fig. 6. Electron concentration in $In_{0.53}Ga_{0.47}As$ region for a randomly generated pattern of dopants using 3D DD–DG simulations. V_G and V_D are respectively the V_T value and 0.05 V.

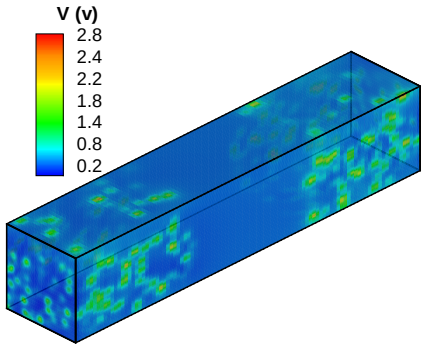

Fig. 7. Electrostatic potential in the $In_{0.53}Ga_{0.47}As$ region for a randomly generated pattern of dopants using 3D DD–DG simulations. V_G and V_D are respectively the V_T value and 0.05 V.

After the DG parameters have been adjusted, the I_D–V_G characteristics obtained from the 3D simulations have been calibrated against experimental data [4] at a drain bias of 0.05 V, as seen in Fig. 5 on a logarithmic scale. Simulation results provide a very good resolution of the sub–threshold region including the slope. In the calibration process, we have used a low field mobility model specific for III–V compounds [17] and the transferred electron mobility model for high electric fields [18]. The transversal component of the electric field has also been included.

B. Threshold voltage variability

To investigate the variability introduced by the random discrete dopants in the S/D regions, we have simulated an ensemble of 300 microscopically different $In_{0.53}Ga_{0.47}As$ GAA MOSFETs. The different devices are obtained using a rejection technique from the device with continuous doping generated by Sentaurus Process. The dopants are placed on an atomistic grid defined by the positions of the In, Ga and As atoms. The charge associated with this distribution is then mapped to the tetrahedrical mesh using a cloud–in–cell algorithm [19]. Using this approach, the charge associated with each dopant is divided into the four nodes of the tetrahedron enclosing it. Therefore, the point–like charge is smoothed on the nearest neighbour mesh nodes.

Every configuration of random dopants creates a different potential distribution which results in different electron concentration profiles along the channel leading to change in I–V characteristics. Figs. 6 and 7 show the electron concentration and the electrostatic potential, respectively, inside the $In_{0.53}Ga_{0.47}As$ region for the same randomly generated pattern of dopants when the gate bias is equal to the threshold voltage. From the generated statistical samples, we have extracted the average threshold voltage, $\langle V_T \rangle$, and its standard deviation, σV_T. We have utilised a constant current criterion ($I_T = 0.475$ μA/μm) to estimate the threshold voltage in each sample [20]. This value has been selected from the simulation results with a continuous doping, choosing a drain current value where the I_D–V_G characteristics on a logarithmic scale exhibit a linear behaviour in the sub–threshold region.

Fig. 8 shows the distribution of the threshold voltages for the randomly generated random dopant distributions. The average threshold voltage and the value obtained from continuous sim-

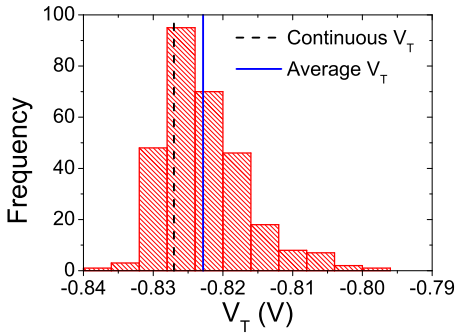

Fig. 8. Distribution of the threshold voltages due to intrinsic variations in the $In_{0.53}Ga_{0.47}As$ region. The average threshold voltage and the threshold voltage for the continuous distribution are also shown for comparison.

ulations, V_{T0}, are also presented for comparison. The average number of p–type dopants in the channel of the device and n–type dopants in the S/D regions are, respectively, 3 and 2116. The observed random dopant induced threshold voltage shift, $\langle V_T \rangle$–V_{T0}, is 4.2 mV, and the spread in the threshold voltage values is 5.9 mV. These values are noticeably lower than those observed in equivalent bulk Si MOSFETs [21] (with $\langle V_T \rangle$ and $\langle V_T \rangle$–V_{T0} over 800 and 70 mV respectively). Finally, it is worth noting the computational burden that a statistical analysis of this kind entails. When using 4 processors, it takes approximately 6 hours to obtain a single I_D–V_G curve simulation on an Intel(R) Xeon(R) CPU L7555 @ 1.87GHz.

IV. Conclusion

In this paper, we have presented a study of the threshold–voltage induced random dopant variability for a 50 nm gate length inversion–mode $In_{0.53}Ga_{0.47}As$ GAA FinFET. For this purpose, we have used a parallel 3D FE quantum–corrected DD device simulator. The quantum confinement effects are included via the density gradient approach. The carrier density in the channel has been meticulously calibrated against the 2D Schrödinger–Poisson solution in the cross–section through the middle of the gate using Silvaco's ATLAS. After that, the mobility model implemented in the simulator has been validated by adjusting the I_D–V_G characteristics obtained from the 3D simulator against experimental data. Simulation results show an important decrease in the variations, the spread in the threshold voltage values is 5.9 mV, and in the threshold voltage shift which is 4.2 mV, when compared with bulk Si MOSFETs.

Acknowledgment

The work developed in this paper has been supported in part by the Ministry of Education and Science of Spain and FEDER funds under contract TEC2010–17320 and by the Xunta de Galicia under contracts 2010/28 and 09TIC001CT. NS, AGL, EC, and RV would like to thank Galician Supercomputing Centre (CESGA) for the access granted to the SVGD system. KK thanks for support from EPSRC ARFellowship (EP/D070236/1–2).

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