A 3D Simulation of the Lateral Charge Spreading Effect in Charge Trapping NAND Flash memory

Sangyong Park, Seongwook Choi, Kwang Sun Jeon, Hui Jung Kim, Seung Man Rhee, ilo Yoon and Young June Park
School of Electrical Engineering, Seoul National University
Seoul, Korea
E-mail: sypark81@snu.ac.kr

Abstract— **To investigate the lateral charge spreading effect on the retention characteristics of charge trapping memories, we conduct the simulation study with various extended nitride structures, programming patterns and the retention cycles (Program-Retention-Erase) using the in-house 3D self-consistent simulator [1]. The initial condition for the retention simulation is calculated self-consistently considering the charge transport in the conduction band during programming. From this study, we identify that the extended nitride length is an important parameter, and the surround cells and the retention stress must be considered to accurately predict the retention characteristics.**

Keywords - Retention, Charge trapping type memory, Lateral charge spreading,

I. INTRODUCTION

The Charge Tapping Flash (CTF) memory has been regarded as a promising candidate to overcome the scaling limitations of the conventional floating gate. The thin trap layer reduces the cell to cell interference and makes the 3D vertical structures plausible [2][3]. Even though the CTF type cell has many merits, the reliability issues, especially the retention characteristics degraded by the lateral charge spreading, have not been clearly understood yet. Many previous researchers on modeling and simulation of the charge loss mechanism have been limited to the 1D effect considering only along the vertical direction [4-8]. The experimental data, however, reveals that the charge transport in the lateral direction should be taken into account [9][10]. Moreover, it is difficult to define the trap layer only within the cell region both in the planar and the vertical structure so that the lateral charge spreading cannot be prevented [11]. Therefore, the investigation on the influence of the lateral charge spreading is vital to design the device and predict their characteristics. Some authors reported 2D simulations considering the lateral charge spreading but they assume the initial charge distribution and neglect the vertical charge redistribution [12][13].

In this study, we simulated the retention mode using a 3D self-consistent simulator, developed in house [1]. All retention simulations are conducted with the programmed condition as the initial condition. The details of the charge distribution in the nitride layer have been obtained from the same 3D simulator considering the charge transport in conduction band of the nitride layer. The dependency of the extended nitride length is demonstrated by comparing the three cases (no-extension, finitely-extension, and infinitely-extension). To show the programmed pattern dependency, three-gate string structure is simulated. The retention cycling (program-retention-erase) is also performed, and the result is analyzed. We assumed all the device structures are Self-Aligned Shallow Trench Isolation (SA-STI) structure [13].

II. MODELS AND SIMULATION STRUCTURE

A. Physical Models

Three-dimensional band diagram together with the charge fluxes in the nitride layer during the retention mode are depicted in Fig. 1. The x-direction and y, z-direction indicates the vertical direction and the lateral direction, respectively. In this simulation, the major charge fluxes are classified into four main mechanisms in retention mode as shown in Fig. 1. The two fluxes are tunneling fluxes which are toward to the substrate conduction band from the trap (flux-1 in Fig. 1) and conduction band of nitride (flux-2 in Fig. 1). These currents are expressed in (1) and (2), respectively.

$$J_{TC} = q n_T T_n \nu \Delta l \tag{1}$$

$$J_{CC} = q n_c T_n v_T \tag{2}$$

where n_T is the trapped electron density and n_c is the electron density of the conduction band at the interface, ν is a hitting frequency to escape the trap, T_n is tunneling probability based on the WKB approximation, Δl is the distance between nodes and v_T is the average tunneling velocity of the electrons [7][8]. Assuming that the blocking layer is thick enough to block the

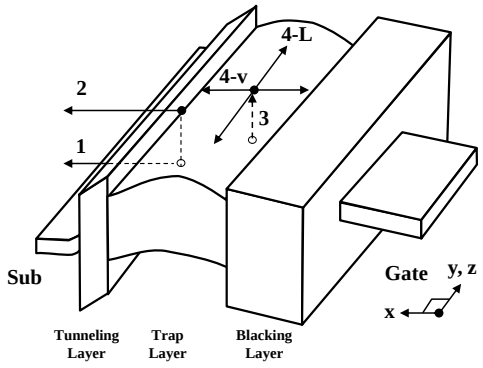

Fig. 1. Three-Dimensional SANOS band diagrams and charge flux diagrams in retention mode.

ISBN 978-0-615-71756-2

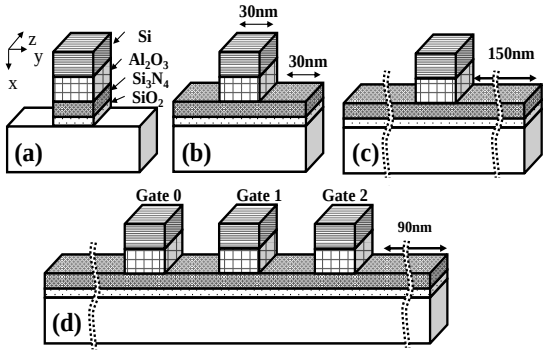

Fig. 2. Simulated structures of the SA-STI SANOS device with (a) No extended nitride, (b) finitely extended nitride, (c) infinitely extended nitride, and (d) three gate string.

back tunneling in the retention mode, the tunneling current of the nitride to gate electrode is ignored.

The electron capture and emission between the trap and conduction band of the nitride are depicted in Fig. 1 (flux-3). The capture is model by the SRH statistics and the emission process is represented by the Poole-Frenkel model as in (3) and (4).

$$\frac{\partial n_c}{\partial t} = \nabla \cdot J_n - c_n (N_T - n_T) n_c + \nu \exp(-\frac{E_t - \beta\sqrt{\varepsilon}}{k_B T}) n_T \quad (3)$$

$$\frac{\partial n_T}{\partial t} = c_n (N_T - n_T) n_c - \nu \exp(-\frac{E_t - \beta\sqrt{\varepsilon}}{k_B T}) n_T \quad (4)$$

where c_n is capture coefficient, N_T is the total trap density in the nitride, E_t is the trap energy, β is the Frenkel constant, ε is the electric field and J_n is the flux-4 in Fig. 1. The flux-4 is the charge transport in the conduction band of the nitride which can be written as

$$J_n = q\mu_n n_c \varepsilon + qD_n \nabla n_c = q\mu \left[n_c(-\nabla\varphi) + \frac{k_B T}{q} \nabla n_c \right] \quad (5)$$

It may be noted here the charge transport along the vertical and lateral direction in both the program and the retention mode are considered since the current density is calculated three-dimensionally.

B. *Simulation Structure*

The 3D SANOS ($Si/Al_2O_3/Si_3N_4/SiO_2/Si$) devices with 4nm tunneling oxide, 8nm Si3N4, 14nm Al2O3, and 30nm channel length are considered in this study. The dependency of the extended nitride length is analyzed by comparing the four structures. Fig. 2(a) is the control device without lateral spreading along the channel direction. A 15nm and 30nm extended nitride structure are selected to represent the finitely extended nitride case (Fig. 2(b)). To reflect the infinitely extended nitride structure, we defined the extended nitride to the 150nm as shown Fig. 2(c).

In fact, the actual NAND flash memory has the array structure. Thus, the three gate string structure is used to show

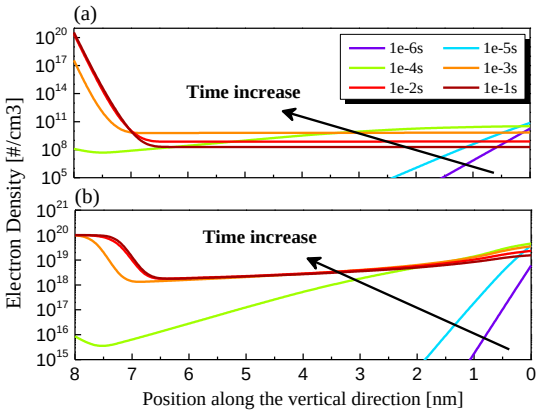

Fig. 3.The transient distribution of the (a) conduction electrons, (b) trapped electrons during the retention mode

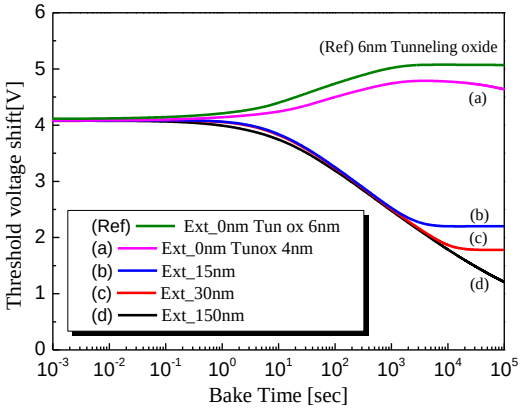

Fig. 4. The threshold voltage shifts of the four devices. (Ref) structure has the 6nm tunnel oxide to eliminate the vertical charge loss.

the interference with the neighbor cells (Fig. 2(d)). Because all of these structures are the SA-STI structure, the changes of the charge distribution along the z-direction in the nitride are neglected.

III. Simulation Results

A. *The initial charge distribution*

The retention simulations are conducted under the temperature of 500K after programming the devices by enforcing 18V to the gate electrode under the temperature 300K. The transient charge distribution of the conduction electron density and the trapped electron density are shown in Fig. 3. The programming is stopped when the threshold voltage shift is 4V, and the charge density distribution is used for the initial condition of the retention simulations.

B. *The dependency of the extended nitride length*

Fig. 4 is the retention curves of the five devices. The Fig. 4(a)-(d) curves are the retention curves of the three cases as already shown in Fig. 2(a)(b)(c). First of all, to distinguish the vertical charge loss from the lateral charge loss, we simulated the structure in Fig. 2(a) with the 6nm tunneling oxide as shown in Fig. 4(Ref). The thick (6nm) tunneling oxide

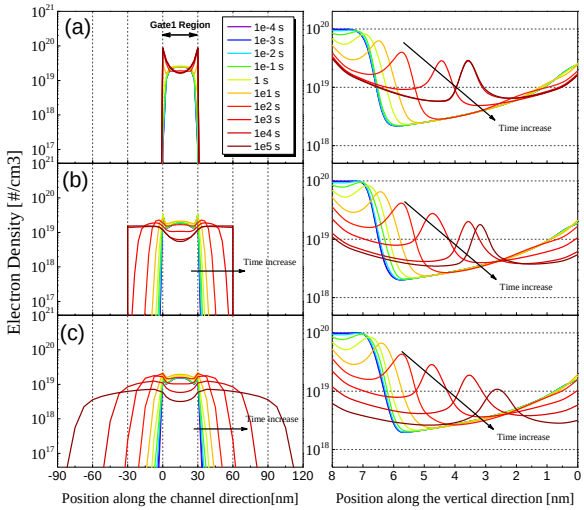

Fig. 5. The transient trapped charge distributions along the channel direction at the tunneling oxide interface (left three graph) and the vertical direction at the middle of the channel (right three graph) of the (a) no-extended, (b) finitely-extended (30nm), and (c) infinitely-extended structures.

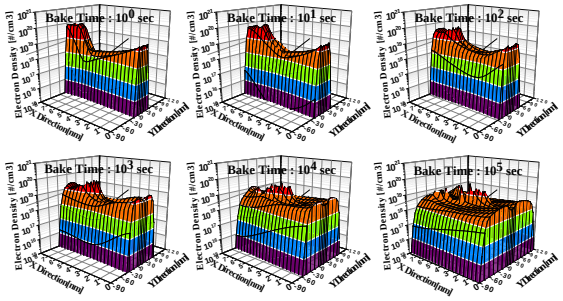

Fig. 6. The transient trapped charge distributions of the infinitely-extended structures from 10^0 sec to 10^5 sec.

structure has no vertical and lateral charge loss except for the charge redistribution along the vertical direction [7]. Thus, the difference between the no-extended nitride device (Fig. 4(a)) and the 6nm tunnel oxide device (Fig. 4(Ref)) indicates the vertical charge loss only. The increment of the threshold voltage of the no-extended nitride structure is due to the charge transport along the vertical direction from the gate side to the tunneling oxide side as shown in Fig. 5(a). Since the trapped electrons are transported along the vertical and the lateral direction in the cases of the finitely and the infinitely extended structure as shown in Fig. 5(b)(c) and Fig. 6, the significant threshold voltage shift is observed, unlike the no-extended nitride structure in Fig. 4(b)-(d). Interestingly, the saturation of the threshold voltage occurs and the saturation point depends on the extended nitride length as shown in Fig. 4(b) and Fig. 4(c). The saturation can be explained by the transient distribution of the trapped electron density as shown in Fig. 5(b). When the extended nitride region is filled with the transported charges up to the equal level of the gate region, the finitely-extended nitride structure has no lateral charge loss but has the vertical charge loss. Therefore, the retention curves are saturated and the saturation of the 15nm extended nitride structure occurs earlier than the 30nm extended nitride structure. From this result, the extended nitride length is

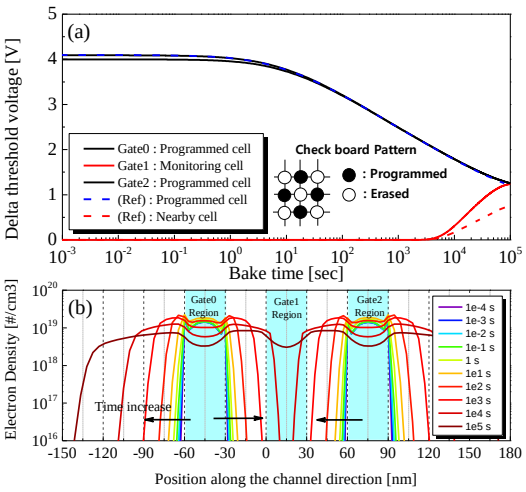

Fig. 7. (a) The threshold voltage shift and (b) the charge distribution of a device which is programmed with the check-board pattern as the bake time goes by.

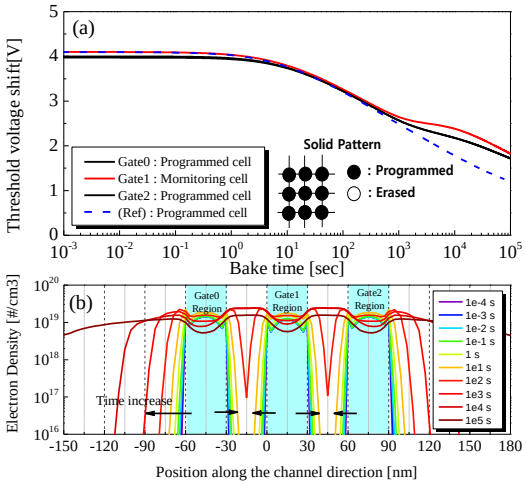

Fig. 8. (a) The threshold voltage shift and (b) the charge distribution of a device which is programmed with the solid pattern as the bake time goes by.

confirmed as an important parameter in predicting the retention time and deciding the specification of the structure, such as a side-wall spacer size [9].

C. The dependency of programmed pattern

To understand the influence of the lateral charge spreading on the neighbor cell, the check-board (Fig. 7) and the solid (Fig. 8) program patterns are simulated with the infinitely-extended nitride structure. Because we assumed that the devices have the SA-STI structure, the nearby cells in the other string is neglected and the only two nearby cells in a same string line affect the monitoring cells. For the reference, the string structure is simulated with a programmed cell and an erased nearby cell. The threshold voltage shift of the reference structure is shown in the Fig. 7(Ref). In the check-board pattern, the threshold voltage of the erased cell is increased more than the reference structure, because the cell is affected by the two programmed cells surrounding the erase cell. The charge

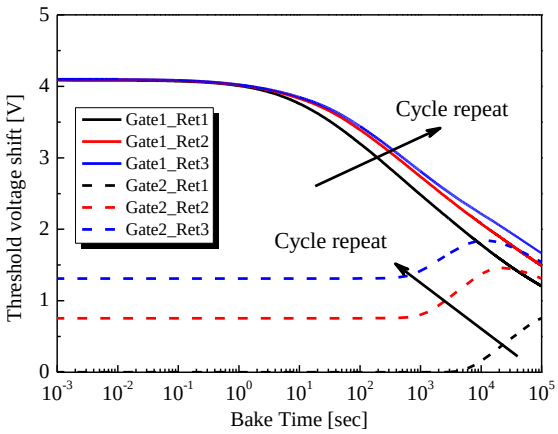

Fig. 9. The threshold voltage shifts of the cycled cell and the nearby cell.

transport is illustrated in Fig. 7(b) with the trapped electron density distribution. Since the transported electrons from the programmed cells reach the erased cell (gate1) region, the threshold shift is increased until the threshold voltage of the erased cell is same as that of programmed cells. The threshold voltage shift of the programmed cells is not different from the single transistor retention characteristics shown in Fig. 4(d).

In the solid pattern, since all cells are programmed, the space region between the gates is the only way for the transport. Hence, the uncovered region with the gate is filled by the electrons which come from the neighboring cell until the potential of the uncovered region is equal to the cell region. As the space region is filled with the electrons, the lateral charge transport is interrupted and the decrease rate of the threshold voltage is reduced as shown in Fig. 8(a). The retention curves, however, are not saturated because the electrons are transported to the outside of the solid pattern array. The charge density in the space region also decreases after the space region is filled as shown in Fig. 8(b). In addition, Fig. 8(a) and Fig. 8(b) show that the retention characteristics of the edge cell is not same as the inner cells in the solid pattern. These pattern dependency results are consistent with the experimental data in [9]

D. The dependency of retention cycle

The remaining electrons after the retention mode could affect to the second retention characteristic. To reflect this situation, we simulated the retention cycle (programming – retention – erase) using the string structure as shown in Fig. 2(d). Fig. 9 shows simulation result after the retention cycle. Remaining charges in the uncovered region disturb the charge spreading. Therefore, the slope of the threshold voltage shift is decreased as the retention cycle is repeated. The experimental data of the retention cycle are reported in [13]. This Simulation results indicates that measurement sequence impacts on the retention performance of the CTF.

IV. CONCLUSION

Using the 3D self-consistent simulator, we simulated the effects of the lateral charge spreading in the CTF. The initial charge distribution has been obtained from the same simulator after the programming considering the charge transport in the conduction band of the silicon nitride self-consistently. Considering device structures with various lateral extended structure, it has been concluded that the extended nitride length is an important parameter to determine the erase characteristics. Since that the neighbor cells affect the monitoring cell of interest, the programmed pattern has to be considered in analyzing the retention characteristics. Finally, we showed that the charge loss characteristic in the retention cycle is also strongly affected by the lateral charge spreading.

ACKNOWLEDGMENT

This research has been supported in part by the Smart IT Convergence System Research Center funded by the Ministry of Education, Science and Technology as Global Frontier Project (SIRC-2011-0031845), Brain Korea 21 Project in 2012, and SAMSUNG electronics.

REFERENCES

[1] Kwang Sun Jeon, "A Study on the Spatial Trap Profile in the TANOS Device using the Numerical Simulation and Charge Pumping Method", Ph.D Dissertation, School of Electrical Engineering, Seoul National University, Korea, 2011.

[2] H.Tanaka, *et al*, "Bit Cost Scalable Technology with Punch and Plug Process for Ultra High Density Flash Memory", *VLSI Technology, 2007 IEEE Symposium on*, pp. 14-5.

[3] J. Jang, *et al*, "Vertical Cell Array using TCAT (Terabit Cell Array Transistor) Technology for Ultra High Density NAND Flash Memory", *VLSI Technology, 2009 Symposium on* , pp. 192-193.

[4] Yu Wang; Marvin H. White, "An analytical retention model for SONOS nonvolatile memory devices in the excess electron state", *Solid-State Electronics*, vol. 49, pp. 97-107, 2005.

[5] Y. Yang, Marvin H. White, "Charge retention of scaled SONOS nonvolatile memory devices at elevated temperatures", *Solid-State Electronics*, vol. 44, pp. 949-958, 2000.

[6] A. Furnémont, *et al*, "A consistent model for the SANOS pro-gramming operation," in Proc. *NVSMW*, 2007, pp. 96–97.

[7] E. Vianello, *et al*, "Impact of the Charge Transport in the Conduction Band on the Retention of Si–Nitride Based Memories", *ESSDERC*, pp. 107-110, 2008.

[8] Elisa Vianello, *et al*, "Experimental and Simulation Analysis of Program/Retention Transients in Silicon Nitride-Based NVM Cells", *Electron Device, IEEE Transactions on*, vol. 56, pp. 1980-1990, 2009.

[9] Changseok Kang, *et al*, "Effects of Lateral Charge Spreading on the Reliability of TANOS (TaN/AlO/SiN/Oxide/Si) NAND Flash Memory", *International reliability physics symposium pro-ceedings*; 2007, p. 167–170.

[10] E. Vianello, *et al*, "Direct probing of trapped charge dynamics in SiN by Kelvin force microscopy", *2010 IEEE International Conference on Microelectronic Test Structures*, pp. 94-97, 2010.

[11] M. Florian Beug, Thomas Melde, Jan Paul, Roman Knoefler, "TaN and Al2O3 Sidewall Gate-Etch Damage Influence on Program, Erase, and Retention of Sub-50nm TANOS NAND Flash Memory Cell", *Electron Devices, IEEE Transactions on*, vol. 58, no.6, 2011.

[12] Arnaud Furnémont, *et al*, "Physical understanding and modeling of SANOS retention in programmed state", *Solid-State Electronics*, vol. 52, pp. 577-583, 2008.

[13] A. Maconi, *et al*, "Impact of lateral charge migration on the retention performance of planar and 3D SONOS devices", proc. *ESSDERC 2011*, pp. 195-198.