

Analysis of tunneling characteristics through hetero interface of InAs/Si nanowire tunneling field effect transistors

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Abstract—Band-to-band tunneling field-effect transistors (TFETs) are considered as potential candidates to replace conventional metal-oxide-semiconductor (MOS) FETs. However, TFETs have an aspect of small current due to its tunneling conduction mechanism. In this paper, we investigate the effectiveness of using the InAs/Si heterojunction nanowire (NW) as a solution to the above problem, and also analyze the tunneling characteristics through hetero interface of InAs/Si heterojunction NW.

I. INTRODUCTION

In recent years, advances in LSI technology based on the continuous scaling down of metal-oxide-semiconductor (MOS) field-effect transistors (FETs) has enabled improvements in the switching speed, density, functionality and cost of microprocessors. However, such downsizing now becomes a cause of reducing the device performance due to increasing leakage current and short channel effects. In addition, the subthreshold swing of conventional MOSFETs is limited to 60 mV/decade at room temperature because of their conduction mechanism where the carriers thermally emitted flow from the source region to the drain region over an energy barrier. These problems are major difficulty in reducing the power consumption of integrated circuits and mean consequently the practical downsizing limit of conventional MOSFETs. Therefore, new types of device have been explored.

Recently band-to-band tunneling transistors (TFETs) have been proposed as an effective means to reduce the power consumption taking the advantages of low leakage current and achieve steeper subthreshold swing than the limit of conventional MOSFET, and various types of TFET have been investigated [1]-[3]. In contrast to conventional MOSFETs, TFETs are comprised of a p-doped source/drain, an intrinsic channel and an n-doped drain/source (p-i-n structures). One of the advantages in such TFETs is that it can act as bandpass filter which can cut off the high and low energy tails of the source Fermi distribution TFETs, reducing effectively the value of subthreshold swing below 60 mV/decade. However, there is an intrinsic drawback in TFETs that the current is carried only via the band-to-band tunneling process and thus

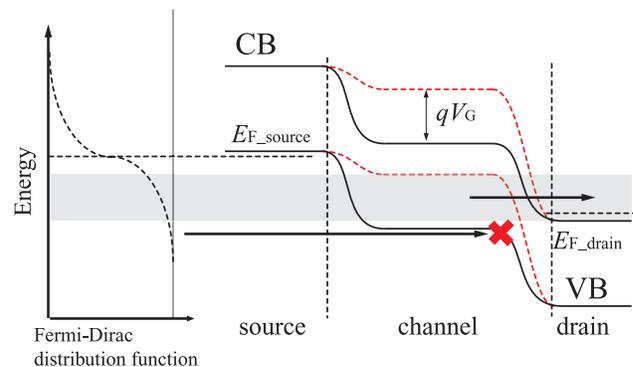


Fig. 1. Band profile for two different gate voltages in p-type tunneling FET. The carrier in particular energy region is only allowed to tunnel from valence band in source region to conduction in drain region.

the on-current is relatively small compared with conventional MOSFETs. In this work, we investigate the effectiveness of using the InAs/Si heterojunction nanowire (NW) as a solution to the above problem, and influence of strain caused by heterojunction on tunneling characteristics through hetero interface.

II. SIMULATION METHOD AND DEVICE MODEL

TABLE I
COMBINATION OF MATERIALS IN OUR MODELS

Model	p-region	i-region	n-region
Si NW	Si	Si	Si
InAs NW	InAs	InAs	InAs
Si/Si/InAs NW	Si	Si	InAs
InAs/InAs/Si NW	InAs	InAs	Si

The device structure analyzed in this work is shown schematically in Fig. 2, where the perfect lattice matching between Si and InAs is assumed. In order to explore the optimum structure of InAs/Si heterojunction NW for TFETs, we analyze four models: Si NW, InAs NW, Si/Si/InAs NW, and

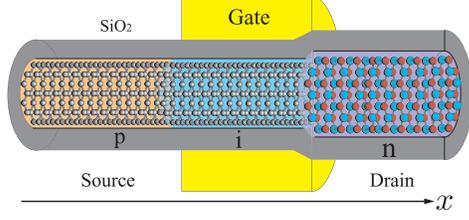


Fig. 2. Schematic illustrations of an example of InAs/Si heterojunction nanowire TFET structure considered in this study (called Si/Si/InAs NW monde in text), where Si nanowire is used in p- and i-type regions while InAs nanowire is used in n-type region. The channel orientation is $\langle 110 \rangle$.

InAs/InAs/Si NW model. The devices have channel length of 10 nm for Si and 11 nm for InAs (the gate length is assumed to be equal to the channel length). The acceptor (donor) density in the source (drain) region amounts to $1.9 \times 10^{19} \text{ cm}^{-3}$ ($1.9 \times 10^{19} \text{ cm}^{-3}$). The diameter of the nanowire is 1.78 nm for Si and 2.01 nm for InAs. All the nanowire regions are surrounded by a 1 nm-thick dielectric layer (SiO_2) and the transport direction is aligned with $\langle 110 \rangle$ orientation. All the nanowires have the gate-all-around (GAA) structure.

The strain arising from the different lattice constant between of Si and InAs is taken into account by performing the structural relaxation employing the valence force field method with the Keating potential [4]. In the Keating potential, the strain energy of the i th atom $E_{\text{strain}}(i)$ is expressed in terms of the changes in the bond lengths and bond angles as

$$E_{\text{strain}}(i) = \sum_j \frac{3\alpha_{ij}}{8d_{ij}^2} (|r_{ij}|^2 - d_{ij}^2)^2 + \sum_{j,k>j} \frac{3\beta_{ijk}}{4d_{ij}d_{ik}} \left(r_{ij} \cdot r_{ik} - \frac{1}{3}d_{ij}d_{ik} \right)^2. \quad (1)$$

Here the first summation is over four neighbor j th atoms around the i th atom, the second summation is over all pairs of the neighbors j and k of i th atom, and r_{ij} is a position vector joining j th atom to the i th atom. d_{ij} is the strain-free bond length of the i - j bond, α_{ij} is the bond-stretching force constant of the i - j bond, and β_{ijk} is the bond-bending force constant of the j - i - k bond angle. In order to minimize the strain energy, each atom is iteratively moved along the direction of the force acting on it (i.e., $\mathbf{F}(i) = -\nabla(E_{\text{strain}}(i))$) until the force vanishes. Once the relaxed structure is obtained, the calculation of the band-to-band tunneling current is carried out by using the Landauer-Büttiker formula,

$$I = \frac{2q}{h} \int dE T(E) (f(E - \mu_S) - f(E - \mu_D)), \quad (2)$$

where $q(> 0)$ is the elementary charge. $f(E - \mu_{S(D)})$ is the Fermi-Dirac distribution function, $\mu_S = E_F$ and $\mu_D = E_F - qV_D$ are the Fermi energies in the source and the drain electrodes, with V_D being the source-drain voltage. We assume the room temperature $T = 300 \text{ K}$ throughout this paper. In Eq. (2), $T(E)$ is the transmission coefficient. To calculate the transmission coefficient, we use the three-dimensional non-equilibrium Green's function (NEGF) method [5] with

the $sp^3s^*d^5$ tight-binding Hamiltonian [6], [7]. The Green's function is represented as a function of electron energy E as

$$G(E) = [EI - H - U - \Sigma_L(E) - \Sigma_R(E)]^{-1}, \quad (3)$$

where H is the device Hamiltonian, and $\Sigma_{L,R}(E)$ are open-boundary terms [8]. In Eq. (3) U is the potential distribution in the device, and is obtained by solving the Poisson's equation self consistently with the charge distribution calculated with NEGF. The total transmission from the source to drain lead at the energy E is given by

$$T(E) = \text{Tr}[\Gamma_R(E)G(E)\Gamma_L(E)G^\dagger(E)], \quad (4)$$

where $\Gamma_{L,R}(E)$ are broadening functions represented by open-boundary terms

$$\Gamma_{L,R}(E) = i(\Sigma_{L,R}(E) - \Sigma_{L,R}^\dagger(E)). \quad (5)$$

III. RESULTS AND DISCUSSIONS

A. Strain of InAs/Si heterojunction nanowire

Figure 3 shows the maximum deviation of atomic positions from their initial (unrelaxed) positions in each plane (atomic layer with one atom thickness). In the structural relaxation calculation of our models, InAs NW and Si NW are assumed to be perfectly lattice matched at the heterointerface. In Fig. 3

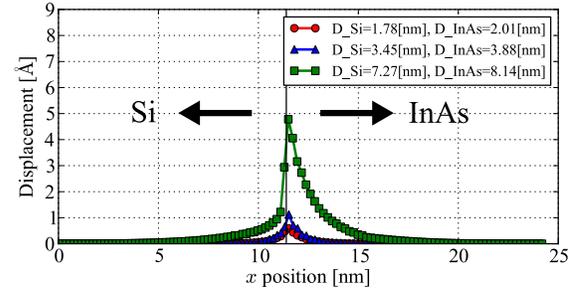


Fig. 3. Distribution of deformation along transport direction. Black solid line indicates the boundary surface between Si NW and InAs NW. The displacement from initial position of atom is plotted.

we observe that the atomic positions in the InAs NW side are deformed over longer region along the transport direction than in the Si NW side. Such clear difference of the deformations between InAs NW and Si NW sides is due to the difference of elasticity in crystalline InAs and Si. In fact, while the bond-stretching and bond-bending force constants of Si are 48.50 N/m and 13.81 N/m, respectively, those of InAs are 35.18 N/m and 5.50 N/m, respectively [9], which means that InAs is more deformable than Si. The larger the diameter of model becomes, the higher the maximum strain energy is. Noting the fact that the strain energy is concentrated around the heterojunction interface, we next show the distribution of strain energy within the heterojunction interfaces (InAs NW side and Si NW side). Figure 4 shows the cross sectional view of strain energy distribution within two planes located at the InAs NW side and the Si NW side of the heterointerface. Each mark corresponds to each individual atom. Darker and brighter colors represent low and high strain energy. Furthermore, in

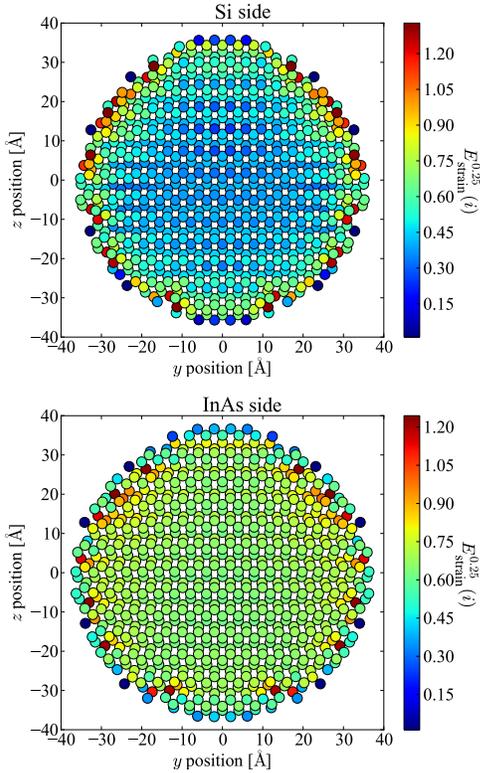


Fig. 4. Distribution of strain energy in cross section hetero surface of Si NW side (upper) and InAs NW side (lower) with the diameters 7.27 nm and 8.14 nm, respectively.

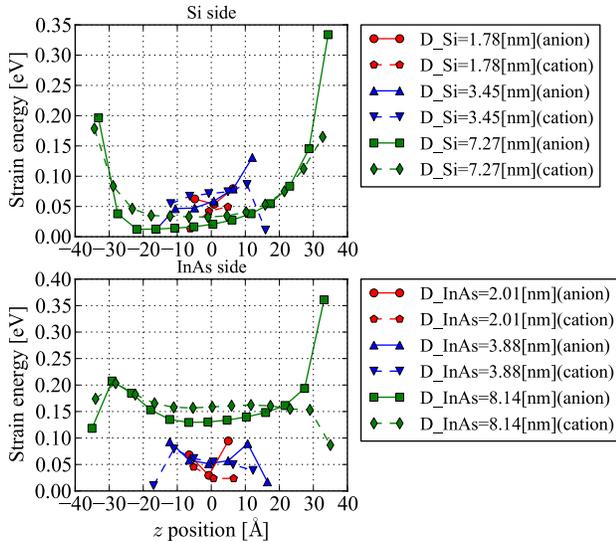


Fig. 5. Strain energy distribution for atoms located along the line specified by $y = 0$ in Fig. 4. Three different models in diameter are plotted.

order to examine the diameter dependence of strain energy, we focus on the atoms located along the line specified by $y = 0$ in Fig. 4, and their z position and strain energy are plotted in Figure 5. As seen in Figs. 4 and 5, the atoms near the surface of nanowire acquire larger strain in large model. This is

because the atoms near the surface of nanowire have less than four neighbor atoms, and thus these atoms can easily change their positions. On the other hand, atoms near the center of cross section acquire only small strain since those atoms are in the bulk like environment and are restricted in changing their positions from diamond or zinc blende structure. That is, deformation resulting from the heterojunction interface tends to concentrate on the surface of nanowire. In small diameter model, however, the atoms near the center of Si NW have larger strain energy compared with large diameter model. This result indicates that not only the atoms near the surface but also those near the center of cross section of nanowire can change their positions. Hence, the smaller the diameter of the model is, the more widely the atomic structure change and the more possible it is to make heterojunction of Si NW and InAs NW.

B. Complex band structures and I_D - V_G characteristics

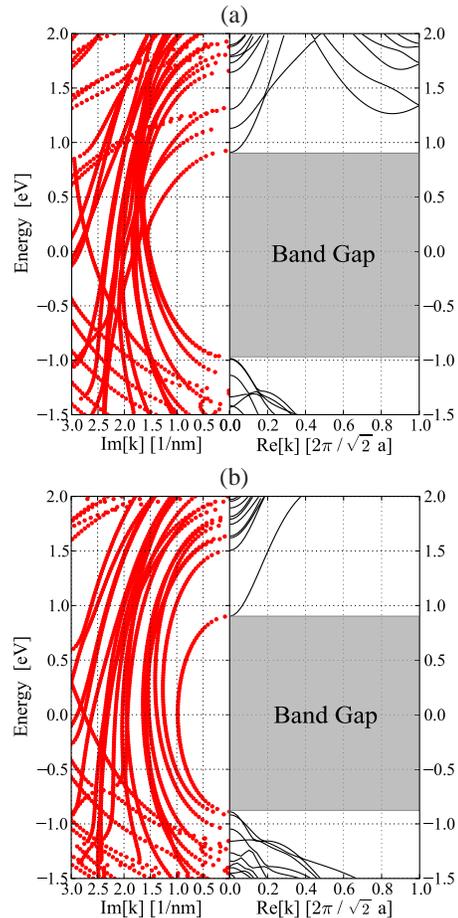


Fig. 6. Complex band structures of $\langle 110 \rangle$ oriented Si NW (a) and InAs NW (b) with the diameters 1.78 nm and 2.01 nm, where $a = 5.4309$ and 6.058 \AA are the lattice constants of bulk Si and InAs, respectively.

Figure 6 shows the complex band structures in Si NW (a) and InAs NW (b). Here the right and the left panels in the each figure represent the dispersion curves for the

real and the imaginary part of the wavenumber ($\text{Re}[k]$ and $\text{Im}[k]$), respectively, where the smaller value of $\text{Im}[k]$ within the band gap region allows the higher tunneling rate. Figure 7 shows the I_D-V_G curves for Si/Si/InAs NW (p-Si/i-Si/n-InAs), InAs/InAs/Si NW (p-InAs/i-InAs/n-Si), Si NW (p-Si/i-Si/n-Si), and InAs NW (p-InAs/i-InAs/n-InAs) models. As we can understand from Figs. 6 and 7, InAs NW model shows higher on-current due to the higher tunneling rate compared with Si NW model, but its leakage current also high. That is, it is difficult for both Si NW and InAs NW to suppress the leakage current and maintain high drive current at the same time. On the other hand, Si/Si/InAs NW model takes advantage of the low tunneling current characteristics of Si NW when gate voltage is not applied, and of the high tunneling current characteristics of InAs NW when negative gate voltage is applied. Additionally, in Si/Si/InAs NW and InAs/InAs/Si model, the bandgap widths in Si NW and InAs NW region don't have major difference as shown Fig. 8. Thus, the characteristics of InAs/Si heterojunction NW are attributed to the difference of the tunneling rate of the materials.

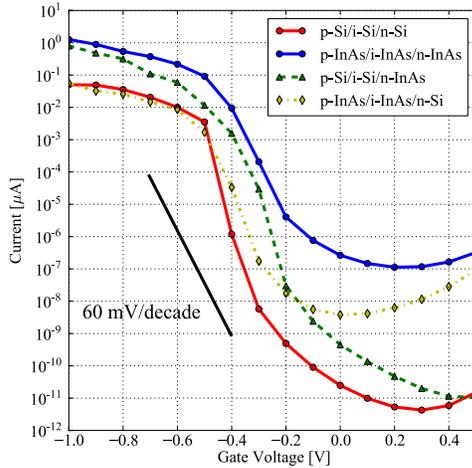


Fig. 7. I_D-V_G curve of Si/Si/InAs, InAs/InAs/Si, Si, and InAs NW TFETs are plotted for a given source-drain voltage $V_D = 0.5V$.

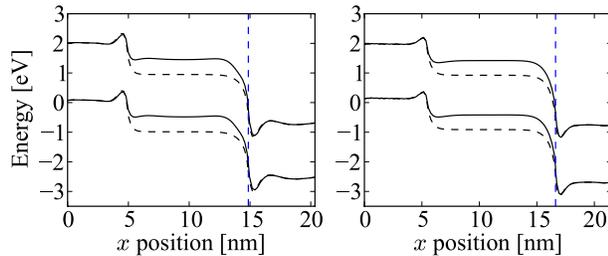


Fig. 8. Conduction and valence band profile (solid and dashed lines are $V_G = -0.5V$ and $0.0V$, respectively) of the Si/Si/InAs (left) and InAs/InAs/Si NW (right) models. Blue dashed lines indicate hetero interface.

C. The influence of strain on the tunneling characteristics

The effect of the structural relaxation on current characteristic of Si/Si/InAs NW model is shown in Fig. 9, where the relaxation model allows the atoms to be bonded smoothly at the hetero interface to maintain the perfect lattice matching,

while in the non-relaxation model the bonds are disconnected near the surface region of the nanowire. Higher transmission probability and larger current density spectrum are found in the lower energy regime in the relaxation model compared with the non-relaxation model. Thus the perfect lattice matching makes tunneling occur at the lower energy point.

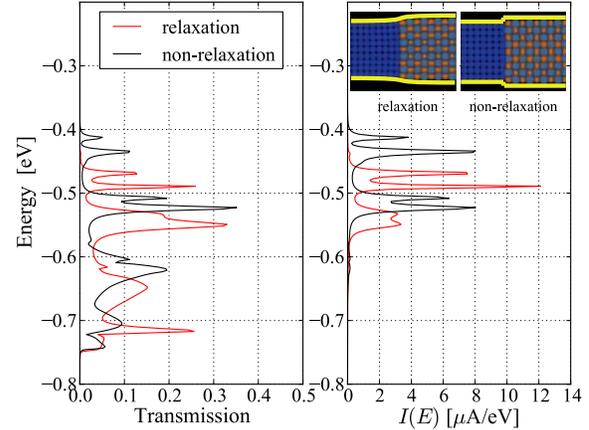


Fig. 9. Transmission and current spectra of relaxation and non-relaxation models of Si/Si/InAs, InAs/InAs/Si NW TFETs are plotted for a given source-drain voltage $V_D = 0.5V$ and gate voltage $V_G = -0.8V$.

IV. CONCLUSION

We have analyzed the performance of the TFET comprised of InAs/Si NW. By comparing with the TFET comprised of Si and InAs NW, we found that the use of p-Si/i-Si/n-InAs NW model is advantageous in the negative gate voltage regime in increasing the on current compared with the Si NW, and in keeping the lower subthreshold swing compared with the InAs NW. We have also shown that the change of atomic positions near the hetero interface influences meaningfully the magnitude of the tunnel current through the hetero interface.

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