# Strain engineering in MOS and Tunnel FETs: models, challenges and opportunities.

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**Context.** Starting from the 90nm technology node most semiconductor companies have introduced strain in their CMOS technologies, and strain engineering has soon become one of the most cost effective technology boosters [1], [2]. Given the many possible strain configurations that depend on the device structure (planar MOSFETs, FinFETs, nanowire transistors) and on the technological stressors employed in the fabrication process, the support of modeling and simulations appear of utmost importance to steer the device design and narrow down the possible options.

**Strain modeling.** The strain affects the behavior of CMOS transistors in many respects, including the mobility and the on current, the source-drain and gate leakage currents and also the device reliability. The presentation will be limited to topics related to carrier transport.

One can identify roughly two different families of approaches to model the effects of strain in electron devices. The first methodology consists in calculating the band-structure in the presence of strain by using possibly comprehensive, full-band models, which are then used to extract band edges and effective masses for transport models based on the effective mass approximation. The methods to calculate the band-structure include DFT [3], empirical pseudo-potential [4], [5], [6] and full-band **k·p** methods [7]. The extraction of band-edges and effective masses is useful to gain an insight in the simulation results, however it has a limited physical significance for $p$-type devices. A second approach consists in calculating the bands and solving the transport problem with the same model, as exemplified by mobility calculations in strained inversion layers described by a 6-band **k·p** model [8], [9], and by quantum transport studies of MOS and Tunnel FETs employing either a **k·p** [10], [11] or a tight-binding Hamiltonian [12]. This approach is viable for both $n$ and $p$-type transistors, but, being fully numerical, the interpretation of the simulation results is not always straightforward.

**Applications.** In recent years both modeling methodologies have been used to study strained nanoscale devices and some representative results will be presented at the conference, dealing with mobility and on current in MOSFETs as well as performance of Tunnel-FETs. As an example of results obtained in our group, Fig.1(a) reports the $I_{on}$ versus the uniaxial stress for both sSi and sGe $n$-MOSFETs [13]. The $I_{on}$ for (110) and (111) Ge is larger than for sSi essentially because of the larger injection velocity. As can be seen, the strained (100) Ge can outperform sSi if the series resistance $R_{SD}$ is the same, however the $I_{on}$ advantage of the sGe is lost if the $R_{SD}$ of the Ge $n$-MOSFETs is increased by 50%. Fig.2, instead, compares the IV curves of Tunnel-FETs for different stress conditions and shows that the biaxial stress increases remarkably the $I_{DS}$ of the transistors (and reduces the $V_T$), while the uniaxial stress has a limited impact on the IV curves [11].

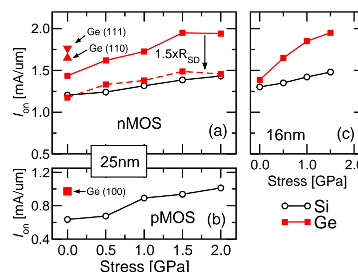


Fig. 1: $I_{on}$ vs. stress for Si and Ge $n$-MOSFETs; different crystal orientations for unstrained Ge are also shown. (b) $I_{on}$ vs. stress for Si $p$-MOSFETs; the unstrained Ge is also shown. (c) Same as (a) for a 16nm $n$-MSOFET ($EOT$=0.85nm, $T_{SI}$=7nm). See [13] for the device parameters.

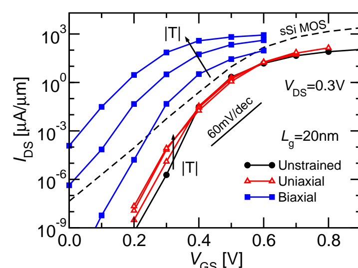


Fig. 2: Drain current versus gate voltage characteristics for different strain conditions. Compressive uniaxial stress is $T_{xx}$=−1, −2 and −3GPa and tensile biaxial stress is $T_{yy}$=$T_{zz}$=1, 2 and 3GPa. The sSi nMOS drain current has been reported for comparison. See [11] for the device parameters.

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