The story beyond primitive compact model - A super compact model for advanced technology

Chung-Kai Lin, Cheng Hsiao, Kei-Wei Su, Min-Chie Jeng
Taiwan Semiconductor Manufacturing Company
168, Park Ave 2, Hsin-Chu Science Park, Hsin-Chu County, Taiwan 308-44, R.O.C
email: cklinb@tsmc.com

Introduction: Over the past 15 years, a tremendous effort has been put together by university and industry to develop the so-called primitive compact models based on intrinsic device physics such as Short Channel (SCE)/Narrow Width (NWE)/mobility effects, .etc [1]. Although these effects are still extremely important for advanced technology modeling, effects extrinsic to devices such as mechanical stress induced mobility and threshold voltage shifts make these primitive compact models inadequate. As devices become dependent on layout and/or environment, even devices with the same W/L may not exhibit similar electrical characteristics [2-3]. This is a big surprise and troublesome to designs, which are sensitive to device matching. As a result, layout information is needed in addition to the device L and W to describe the device characteristics more accurately as shown in Fig.1. Secondly, the importance of variability sources is changing. In the past, variation due to lithography usually dominated the variability. For advanced technologies, fluctuation in doping concentration may surpass all other effects. To reduce the unnecessary design guard band, detailed partitioning of the variation sources is critical as shown in Fig. 2. Design sign-off based on the conventional total corner approach is definitely too conservative [4-5]. In addition, due to the smaller head-room (Vdd-Vth) caused by reduced operation voltage, prediction of variation to high-sigma region is extremely difficulty due to non-Gaussian distribution. As a result, significant amount of modeling resource is expected to spend on the variability model for advanced technologies. Thirdly, device performance drift due to reliability cannot be ignored. Using over-drive to boost circuit performance has become a common practice nowadays. How to predict the degradation caused by high voltage/temp stress is another challenge for compact modeling. The aging simulation is an emerging issue for the model developer and the design community. Finally, the parasitic components may not be regarded as "parasitics" anymore, since they are equally important as the intrinsic device while optimizing the device performance. The conventional boundary of Back-End-Line/Front-End-Line modeling is getting vague along with the complicated technology profile. Some of the FEOL primitive model components are counted in BEOL model now. The reduction of RC loading is one of deciding factors to achieve competitive designs. As a result, an accurate FEOL/BEOL model partition is crucial in the current compact modeling flow. In the presentation, the four subjects mentioned above will be discussed.

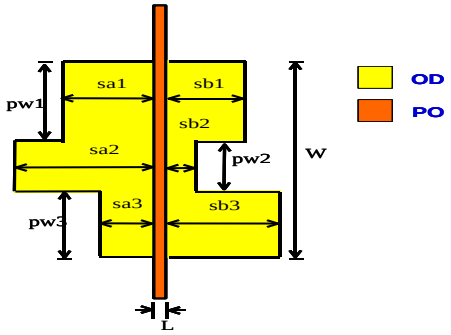

Figure 1. A typical layout of MOS devices needs more instance parameters (sa, sai and sbi) in addition to the traditional Land W [2]

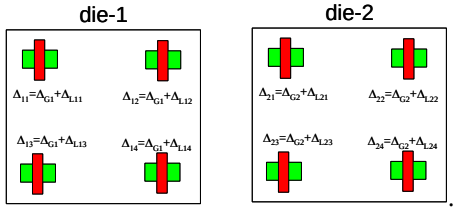

Figure 2. Two commonly observed random variation types. Local (intra die) and global variation (inter die). The detailed breakdown is described in [5].

REFERENCES

[1] Compact Model Cousil Homepage: http://www.geia.org/CMC-Introduction

[2] K-W. Su, Y-M. Sheu, C-K. Lin, S-J. Yang, W-J. Liang, X. Xi, C-S. Chiang, J-K. Her, Y-T. Chia, C. H. Diaz, and C. Hu, "A Scalable Model for STI Mechanical Stress Effects on Layout Dependence of MOS Electrical Characteristics", Proc. Custom Integrated Circuits Conference, Sept. 2003, pp. 245-248.

[3] Y. M. Sheu, K. W. Su, S. Tian, S. J. Yang, C. C. Wang, M. J. Chen, and S. Liu, "Modeling the well-edge proximity effect in highly-scaled MOSFETs," IEEE Trans. Electron Devices, Vol. 53, pp. 2792-2798, Nov., 2006.

[4] Chung-Kai Lin, Cheng Hsiao, Wei-Min Chan, Min-Chie Jeng, "A Smart Approach for Process Variation Correlation Modeling,", International Conference on Simulation of Semiconductor Processes and Devices (SISPAD) pp. 159–162, 2011.

[5] Chung-Kai Lin, Cheng Hsiao, HC Tseng, Min-Chie Jeng, "A Comprehensive Solution for Process Variation Characterization and Modeling," SISPAD 2012

ISBN 978-0-615-71756-2