Time Domain Simulation of Statistical Variability and Oxide Degradation Including Trapping/detrapping Dynamics

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Abstract—**We present a unified modelling framework for the simulation of time-dependent statistical variability resulting from the dynamics of oxide traps. Given that trap dynamics underlie the phenomena of RTN, BTI and TAT leakage, our approach enables the statistical evaluation of reliability parameters.**

Keywords: simulation; statistical variability; reliability

I. INTRODUCTION

Statistical variability (SV) is a prominent challenge for CMOS scaling [1, 2]. It is exacerbated by the degradation of the gate oxide, which augments the device mismatch in a time dependent fashion, due to the general increase of both the number of oxide traps and the number of trapped charges [3-5]. Moreover, SV itself affects the oxide degradation phenomena, making the projection of reliability, and the establishment of appropriate design margins at circuit/system level ever more difficult [3-5]. Unfortunately, the interplay between SV and reliability is not yet well understood, nor comprehensively studied [5, 6]. Guided by recent understanding of BTI and RTN phenomena as the manifestation of oxide trap dynamics [5, 7], we propose a unified simulation framework allowing three-dimensional, physics-based, time-dependent simulation of statistical variability and oxide degradation phenomena.

II. METHODOLOGY

The simulation framework is based on the 3D density-gradient-corrected drift-diffusion simulator GARAND, which can model all of the principle sources of statistical variability in contemporary MOSFETs – random dopant fluctuations (RDF), line-edge roughness (LER), metal gate work-function variability (WFV), etc. [8-10]. The simulator is coupled to a kinetic Monte-Carlo (KMC) engine, as schematically illustrated in Fig. 1. The KMC engine yields the event sequence and the necessary inter-event time-steps for the advancement of simulation time. The time-steps are exponentially distributed and appropriately describe the characteristic times associated with trapping/detrapping dynamics underlying RTN and BTI phenomena. The transition rates, being a necessary input for the KMC engine, are obtained from relevant local models for charge trapping and emission (one-dimensional inelastic, multi-phonon-assisted tunnelling), and oxide degradation, based on the 3D device-electrostatics computed by GARAND [11–13]. Oxide traps are modelled by three positional coordinates (x_T,y_T,z_T), energy level ($E_{T,0}$), and capture cross-section (σ). Local TAT current is evaluated as the moving average rate of single charge transfers accomplished by a sequence of capture and emission across the oxide as in [14], but a 1D semi-classical tunnelling model within the WKB approximation is used to calculate the current density in and out of a trap [15].

Simulations are based on a well-scaled 25 nm n-channel bulk MOSFET template with 1.2 nm SiON gate-dielectric, metal gate, retrograde channel doping plus halo-implants to control short-channel effect, and subjected to RDF [13]. Simulations reported here assume fixed number of traps in the oxide, disregarding bias-accelerated trap generation or anneal.

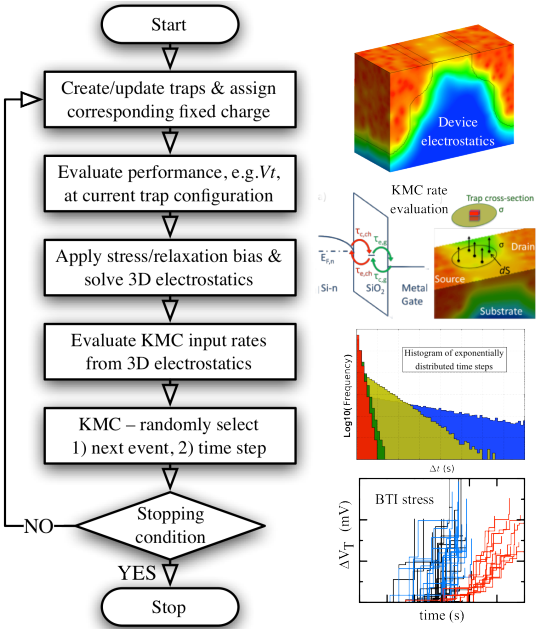

Figure 1. 3D device simulator coupling to the KMC engine, enabling time-domain simulation of BTI, RTN, TAT based on trap dynamics.

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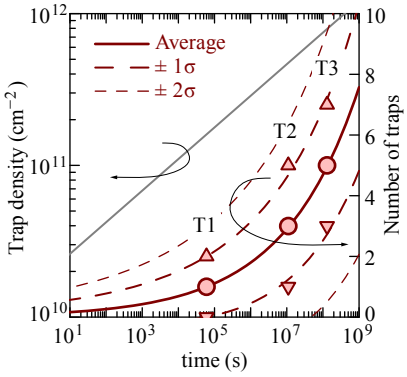

Figure 2. Power-law evolution of trap-density and trap number in the simulated bulk MOSFETs with 25x25nm^2 gate.

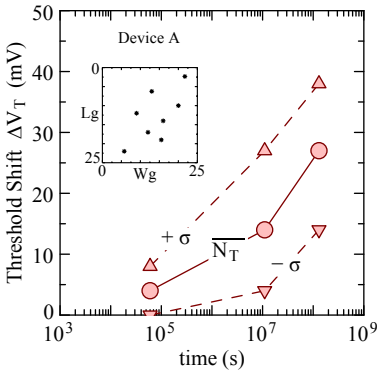

Figure 3. ΔV_T evolution corresponding to T1-T3 indicated in Fig. 2, for the average and ±σ number of traps, for a particular device subjected to RDF.

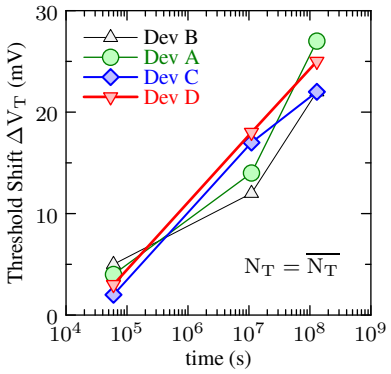

Figure 4. ΔV_T evolution for T1-T3 for devices A to D, all of which have the average number of traps, and are subjected to RDF.

III. Results and Discussion

Figure 2 shows the time-evolution of sheet density of oxide traps and the corresponding number of traps in the simulated device, assuming a power-law time-dependence, similar to experimentally observed trends [3,16]. Fig. 2 is subject to the following simplifications — field accelerated trap-generation is not considered, and the power factor describing the increase of trap density with time is adjusted so that over the lifetime of the device, assumed to be ~ 3x10^9 s, the average sheet-density of traps becomes 10^{12} cm^{-2}, considered representative for heavy degradation in ultra-scaled CMOS. With this in mind, Fig. 2 gives a clear indication that at any given time, the number of traps per device, in an ensemble of small transistors, e.g. as in SRAMs, will broadly vary in a stochastic manner. Figure 3 shows how this variation in the trap number N_T within the range of ±σ around the average translates in a variation of the threshold shift of a given transistor with time. If we adopt the typical lifetime criterion of $\Delta V_T = 30$ mV, a +σ deviation in the trap number results in a whole decade difference in lifetime, for the given device.

The inset of Fig. 3 shows the lateral configuration of the maximum number of seven traps being considered. It must be noted however, that devices with the same trap configuration at a given time exhibit markedly different ΔV_T evolution, due to the interaction between traps and RDF. This is demonstrated in Fig. 4, showing ΔV_T versus time for several devices having identical configuration of filled traps at each point in time. From the crossing guidelines connecting the simulation points in Fig. 4 it is clear that extrapolation of ΔV_T over time for a single device is meaningless. Indeed, one have to analyse the properties of device ensembles both in relation to variability and in relation to reliability, as suggested by experiments [4–7].

Figure 5 reports simulations of fast RTN in V_{TH} and I_{DS}. Conceptually these simulations mimic time-dependent defect-spectroscopy (TDDS) measurements of ΔV_T [5], and the conventional RTN measurements of I_{DS} [11], but provide complete information about the signature of individual traps on the RTN signal. The simulation results show a very different expression of traps in the RTN signal of V_T, compared to the RTN signal of the drain current. This reflects the sensitivity of the trapping dynamics to gate bias conditions. The RTN in V_T is simulated under relaxation conditions, with $V_{GS} \sim V_T$, which favours emission from traps, while the RTN in the on-current is simulated at $V_{GS} = 1.0$ V, which favours capture into traps.

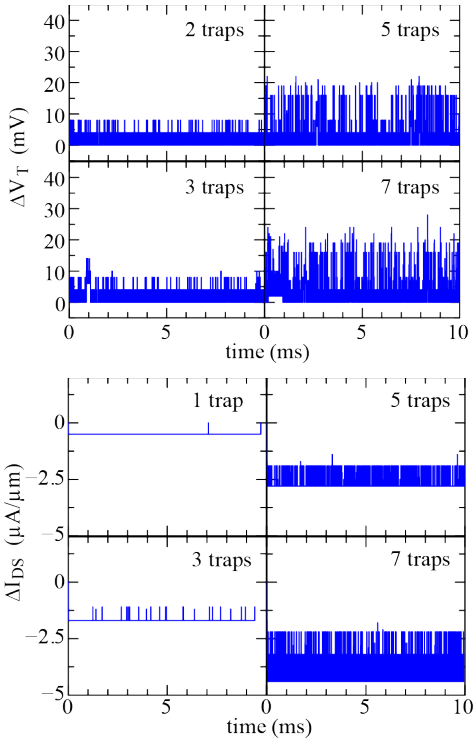

Figure 5. Fast-RTN in Device A, for increasing number of traps. ΔV_T and ΔI_{DS} are obtained at V_{GS} of 0.28V and 1.0V respectively. V_{DS}=50mV. Individual trap manifestation depends on trap position, RDF and V_{GS}.

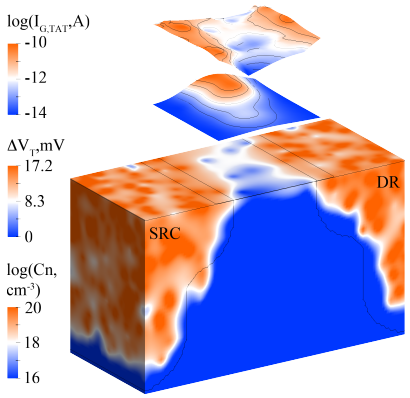

Figure 6. Elevated 2D maps of the single-trap contribution to $I_{G,TAT}$ and ΔV_T for Dev. A; electron concentration in 3D. V_{GS} = 0.28 V, V_{DS} = 50 mV.

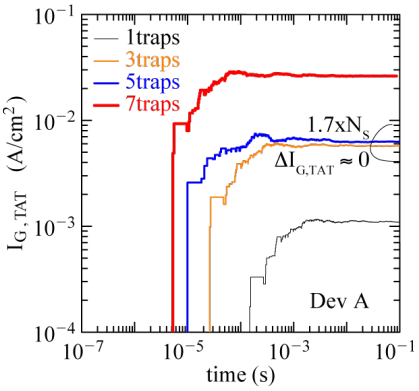

Figure 7. TAT modeled as sequence of single charge-transfer events, for different number of traps. V_{GS} = 1.0 V, V_{DS} = 50 mV.

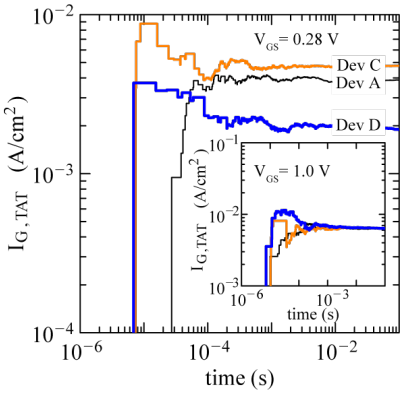

Figure 8. RDF-induced variation of TAT at low V_{GS} for five traps. Inset: RDF screening at high V_{GS}.

Note that in addition to bias and temperature, trap configuration and RDF also influence strongly the impact of an individual trap on ΔV_T. This is clearly shown in Fig. 6, illustrating the two-dimensional (2D) map of the single-trap-induced ΔV_T versus the position of the trap within the lateral extent of the gate. The ΔV_T-map can be related to the electron density distribution in the substrate of the transistor. However, the single-trap-induced ΔV_T is large only were the trap is positioned over a percolation path resulting from the random distribution of impurities in the channel, and much smaller where no percolative current flows, or above the accumulated S/D-overlap regions.

The interplay between RDF and oxide traps likewise impacts the TAT current associated with a given trap. Fig. 6 shows also the 2D map of the contribution of an individual trap to the TAT-component of the gate-leakage. Clearly, traps above a channel region of fewer electrons contribute much less, the variation in tunnel current density reaching four decades.

Figure 7 reports the simulation of TAT gate leakage in a device with RDF, for four cases differing by the number of traps. The time-domain traces reflect the averaging process leading to the steady-state current at the given gate bias of 1.0 V. There is a lower limit of time for reaching this steady state, which depends on the number of traps. More importantly however, the steady sate current in the presence of 3 traps, and in the presence of 5 traps, is the same. This is easily explained with the help of Fig. 6 and the 2D map of the individual trap contribution to the TAT-component of the gate leakage. Note that the addition of two traps to the device represents nearly 70% increase in trap density, which from the perspective of a 1D TAT-model based on continuum trap density would lead to the substantial overestimation of the tunnel current.

Figure 8 shows the RDF-induced dispersion in the TAT-leakage in devices featuring five traps in identical positions, at $V_{GS} \sim V_T$. The inset of Fig. 8 shows that at high gate bias of 1.0 V, the dispersion is greatly reduced. This is due to impurity screening from the inversion charge, as known for the direct tunnelling current as well [17]. A comparison between Fig. 7 and Fig. 8 suggests that in terms of TAT-leakage variability, the principle factor is the trap fluctuation, rather than RDF.

A note regarding the magnitudes of the TAT-leakage is due. It is well known that TAT plays negligible role in sub-2 nm SiON dielectric layers [19]. The results in Figs. 6 – 8 are obtained with a low activation energy of 0.16 eV, which leads to a substantially smaller trap-capture/emission time-constants than experimentally observed, hence an appreciable TAT current density even for the few traps present in the devices under consideration. However our simulation framework correctly predicts the saturation of the TAT-component of the leakage at higher bias [19, 15], and the model could be calibrated for high-κ dielectric stacks where the as-grown traps are with higher density and the exhibited TAT is larger [20].

Finally, we demonstrate the applicability of our simulation framework to the evaluation of the dispersion in BTI-limited lifetime and relaxation in the presence of statistical variability. Figure 9 and 10 report the simulation of typical PBTI charging and relaxation sequences as experimentally observed [3-5]. Note that even maintaining the number of traps fixed, i.e. ignoring trap creation and annealing, a large variation in the time to failure (reaching a predetermined ΔV_T) and in the relaxation time exists due to the stochastic character of the phenomenon and to RDF.

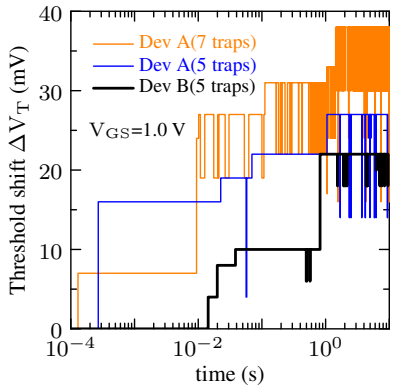

Figure 9. BTI impact at V_{GS}=1.0. Charging sequences are stochastic, depending on trap number and RDF.

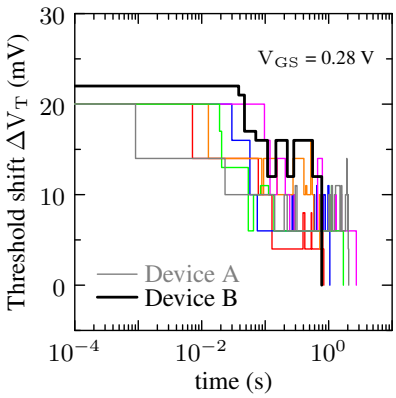

Figure 10. BTI relaxation of 5 traps. The dispersion in relaxation time for Device A is due to different sequences.

Note that results in Figs. 9 and 10 are obtained with an activation energy of 0.6 eV, which is derived experimentally [7], or theoretically from DFT simulations [5], and yields time-constants in very good agreement with measurements [7, 21].

IV. Conclusions

The presented simulation framework captures the effects of all principle sources of SV and the stochastic nature of oxide-trap dynamics and oxide wear-out, thus allowing the evaluation of the distribution of lifetime and relaxation time constants in ensembles of ultra-scaled devices. Moreover it enables the simulation of time-dependent variability, which is an essential aid for variability- and reliability-aware design of compact models, circuits and systems.

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