3D Simulation Study of Work-Function Variability in a 25 nm Metal-Gate FinFET with Curved Geometry using Voronoi Grains

G. Indalecio and A.J. García-Loureiro
Department of Electronics and Computer Science
University of Santiago de Compostela
15782 Santiago de Compostela, Spain
guillermo.indalecio@usc.es

M. Aldegunde and K. Kalna
Electronics System Design Centre
College of Engineering
Swansea University
Swansea SA2 8PP, United Kingdom

***Abstract*—A full-scale 3D simulation study of the impact of metal gate granularity (MGG) on the off-state of a 25 nm length gate SOI FinFET is carried out. The 3D simulations are performed using a parallel finite-element simulator within the drift-diffusion approximation using density gradient quantum corrections. The shapes in the device are described by using splines, and metal grains are modelled using Voronoi diagrams. We study two different grain sizes and silicon fin corner geometries. While the impact of the geometry is found to be negligible in our simulations due to a relatively large size of the device, the grain size has a large impact on the variability of subthreshold characteristics.**

I. Introduction

As the ITRS imposes new requirements over the device characteristics for the next generation of digital circuits, FinFET architectures have became the leading solution to continue the scaling beyond the 32 nm node [1], [2]. These devices are manufactured using high-κ/metal gate stack technology, which brings about a reduced EOT without compromising on leakage current. However, grains of different orientations in the metal gate of MOSFETs with sub-32 nm metal gate/high-K gate stacks induce a work-function variability whose impact is comparable with random dopant fluctuations (RDF) and line edge roughness (LER) [3]–[5]. The variability induced by the different metal grain orientation will become a dominating source of variability over RDF and LER at the 22 nm technology node [3]. Therefore, the work-function variability is expected to affect also significantly FinFET MOSFETs which use the similar metal gate/high-K gate stacks. Other sources of fluctuations (e.g., RDF and LER) have been studied extensively in the past because they were a main concern for scalability for several technological nodes. However, the metal gate granularity has become a source of concern in the last technology nodes with the substitution of polysilicon by a metal in the transistor gate stack.

In this work, we use an in-house developed parallel code to carry out the study of metal grains induced variability. This code implements a full-scale finite element simulation under the drift-diffusion approximation with quantum corrections [6], needed to account for the quantum confinement effects occurring in FinFET architectures [7].

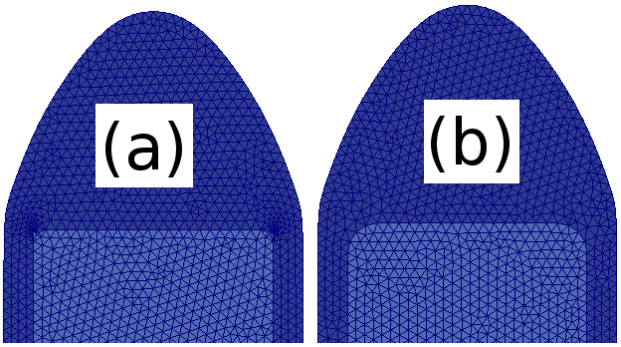

Fig. 1. Details of 'block' (a) and 'curved' (b) geometry of the Si Fin, note the difference at the inner top corners.

II. Device Description and Simulation Approach

The device under study is a 25 nm length silicon FinFET with a 30 nm tall and 12 nm wide silicon body [8]. The dimensions and shape of the oxide layer are modelled following the data of the actual high-κ based dielectric shown in [8], [9]. The geometry of the device is described by using spline functions instead of the more common block-shapes [10]–[13], achieving a more realistic simulation. The doping profile was defined analytically to reproduce experimental sub-threshold characteristics at low and high drain biases.

The device is modelled using a tetrahedral mesh suitable for finite element simulations. This modelling was made with Gmsh. This is a generic CAD tool, which allows us to define the whole device and tag each surface and volume, with arbitrary geometry. In this way, we can change the geometry of the device and reflect possible differences, like curvatures. An example is shown in Fig. 1, where we changed the geometry of the silicon fin from a squared to a rounded one, with the objective of analyse the possible effect of the fin curvature.

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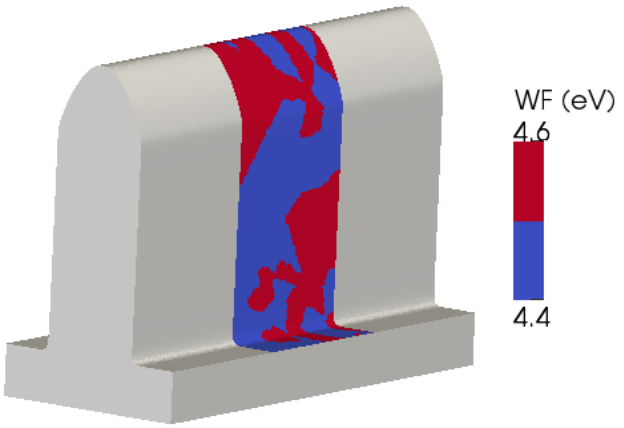

Fig. 2. Render of a simulated FinFET device, with a gate coloured according to work-function values for 5 nm metal grains.

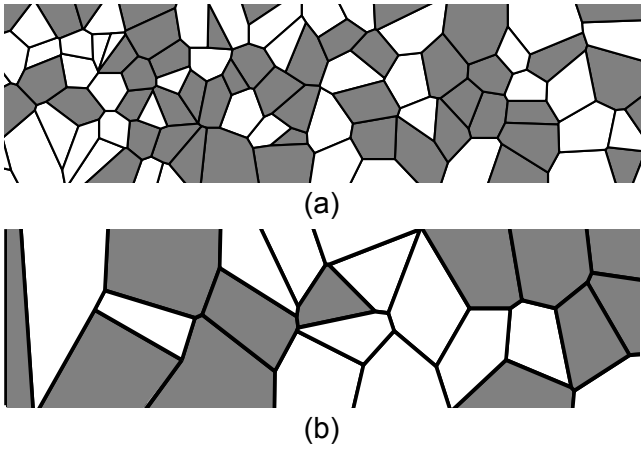

Fig. 3. Example of two Voronoi diagrams used to randomise metal grains, with a mean diameter of (a) 5 nm and (b) 10 nm. Different colour represents different work-function values, 4.4 eV (white) and 4.6 eV (grey).

The simulation code has been parallelised using the MPI communication library. One of the advantages is lower running time, which allows us to run more samples of the work-function or geometries. Another is to have more memory because the distributed scheme have access to available memory at all the nodes, which allows us to run finer meshes and evaluate fine details, like the curvature on Fig. 1 or small patches on the voronoi diagram. This MPI communication requires to divide the mesh in as many parts as nodes of computation. This division is made not using a CAD tool, but using Metis, a well known graph partitioner very suitable for this purpose.

Fig. 2 shows the geometry of the device and an example of the distribution of work-function values on the gate. The work-function granularity is modelled using a grain approximation in which we define two possible orientations for the grains in the metal gate with work-functions of 4.4 and 4.6 eV as shown in Table I together with their respective probability of occurrence [10], [11]. Instead of the usual approximation which employs squares for the shape of the grains [11], [12], we calculated a Voronoi diagram of a set of randomly generated points, which results in variations in size and shape as in realistic crystalline structures such as those used in [13]. Then, each polygon is assigned a certain orientation based on the experimental probabilities shown in Table I. Examples of such diagrams for two different grain sizes are shown in Fig. 3.

These stripes with randomly assigned work-functions are then mapped onto the metal gate of the simulation domain using the inverse of the spline-functions which define its shape. The result of this process for the diagrams in Fig. 3 can be seen in Fig. 4 for the two different grain sizes.

TABLE I
PROBABILITY AND WORK-FUNCTION OF THE DIFFERENT ORIENTATIONS OF THE GRAINS FOR THE METAL GATE USED IN THE SIMULATIONS.

Orientation	Prob.	WF (eV)
<200>	60 %	4.6
<111>	40 %	4.4

The use of Poisson-Voronoi diagrams to simulate the polycrystalline grain structure of materials, although common in other fields [14]–[16], has not been used previously for the metal gates in semiconductor device simulations, where a block-based approach is more common (probably because of its simplicity of implementation). The use of Poisson-Voronoi diagrams to simulate polycrystalline materials has some problems associated to its ability to reproduce certain statistical properties of the grains observed experimentally. This has lead to few studies of alternative approaches which try to obtain a closer match to experimentally observed properties [17], [18]. However, the inclusion of these methods can be computationally very demanding and as such is beyond the scope of this work. We feel that the approach selected in this work represents good compromise and significantly improves on block based generation methods. Thus more realistic simulations of polycrystalline structures following [17], [18] will bring small quantitative changes to the results obtained in the present work.

III. GRAIN INDUCED VARIABILITY

For the present study of variability, we have generated 200 different work-function patterns with two different average grain sizes using the methodology described in the previous section. Half of patterns have an average grain size of 10 nm, and the other half of 5 nm. We have also changed the shape of the Si body, as shown in Fig. 1, from a simple block ('block') to one with corners of 1.5 nm of radii ('curved'), following a similar approximation as in [19].

All the simulation were carried out on FinisTerrae supercomputer from CESGA supercomputing facilities at Galicia, Spain. The FinisTerrae supercomputer is an integrated system with shared memory nodes with a NUMA SMP architecture.

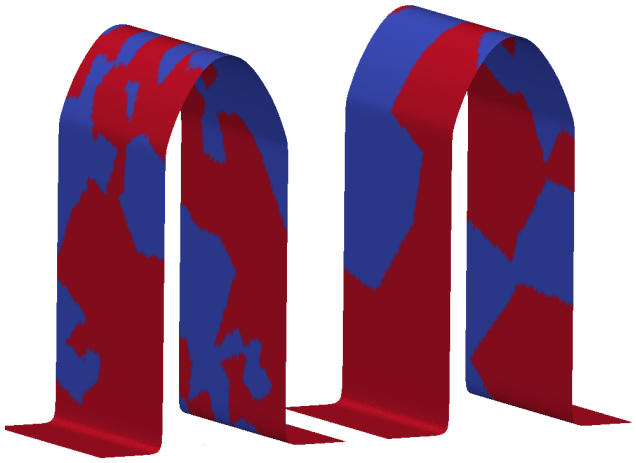

Fig. 4. Example of work-functions for 5 nm (a) and 10 nm (b) grain sizes. These are two of the 200 profiles used in our simulations showing different colour for different work-function values of 4.4 eV (blue) and 4.6 eV (red).

It is composed of 143 computing nodes (142 HP Integrity rx7640 nodes with 16 Itanium Montvale cores and 128 GB of memory each, 1 HP Integrity Superdome node with 128 Itanium Montvale cores and 1,024 GB of memory). This is a total of 2528 processing cores and 19.670 TB of memory, interconnected with an INFINIBAND 4xDDR at 20 Gbps.

The simulation results for the four situations, 5 nm and 10 nm average grain sizes and two geometries, are summarised in Fig. 5. This figure shows the distribution of threshold voltage, sub-threshold swing and off-current for all the simulated cases. The figure also indicates the mean for each case (thick line) as a reference.

Comparing the simulations using 'block' and 'curved' geometry, only small differences can be found, which are mainly statistical fluctuations. This is not the case for the average diameter of the grains. For every set on 5, the mean and variability does not depend on the gran size, but the shape of the histogram shows some change. Looking at the y-axis range on the threshold voltage, the data are more centered on the 5 nm grain case, and more spread on the 10 nm grain case.

TABLE II
THRESHOLD VOLTAGE (V_t), SUB-THRESHOLD SWING (SS), AND OFF-CURRENT (I_{off}) FOR INDICATED METAL GRAIN SIZES AND THEIR RESPECTIVE STANDARD DEVIATIONS.

'Block' geometry						
Grain [nm]	V_t [V]	$\sigma(V_t)$	SS [mv/dec]	$\sigma(SS)$	I_{off} [A]	$\sigma(I_{off})$
5 nm	0.356	0.020	72.752	1.211	-10.734	0.317
10 nm	0.349	0.028	73.220	1.259	-10.610	0.417
'Curved' geometry						
Grain [nm]	V_t [V]	$\sigma(V_t)$	SS [mv/dec]	$\sigma(SS)$	I_{off} [A]	$\sigma(I_{off})$
5 nm	0.355	0.024	72.981	1.199	-10.712	0.366
10 nm	0.356	0.026	73.216	1.362	-10.703	0.390

IV. CONCLUSIONS

In this work, we have studied the metal grain induced variability in the sub-threshold characteristics of a 25 nm gate length Si SOI FinFET using quantum corrected 3D FE DD simulations. We have introduced a new approach for modelling the metal grain granularity using Voronoi diagrams instead of the simple square-based approach. This method allows for a more physical representation of the grain shape and size distribution at very little extra computational cost. Furthermore, as the size of the gate decreases, this method will demonstrate its advantages over simpler physical representation of grain shapes. We also conclude that he study on grain size for the work-function variability produced a similar behaviour to that found on bulk MOSFETs.

When the grain size is comparable to the gate size, the distribution of V_{th} becomes wider. The mean values for the three parameters (I_{off}, V_{th} and SS) are similar, but the dispersion of V_{th} is 40 % larger for the 10 nm grain size than for the 5 nm one. Also, the dispersion of I_{off} is about 30 % larger for the bigger size of grains of 10 nm. This increase in the dispersion is not desired for device characteristics because not only the device figures-of-merit have to be matched but they have to exhibot also small dispersions.

On the other hand, the impact of corner effects on the metal grain induced variability are found to be negligible for the simulated device. The mean values for the parameters are similar in the both 'block' and 'curved' geometries deep inside the uncertainty margin. The dispersion σ shows that the larger grains make the distribution wider thus σ increases. These differences would call for a more extensive study taking a larger variety in work-function granularities into consideration.

V. ACKNOWLEDGMENTS

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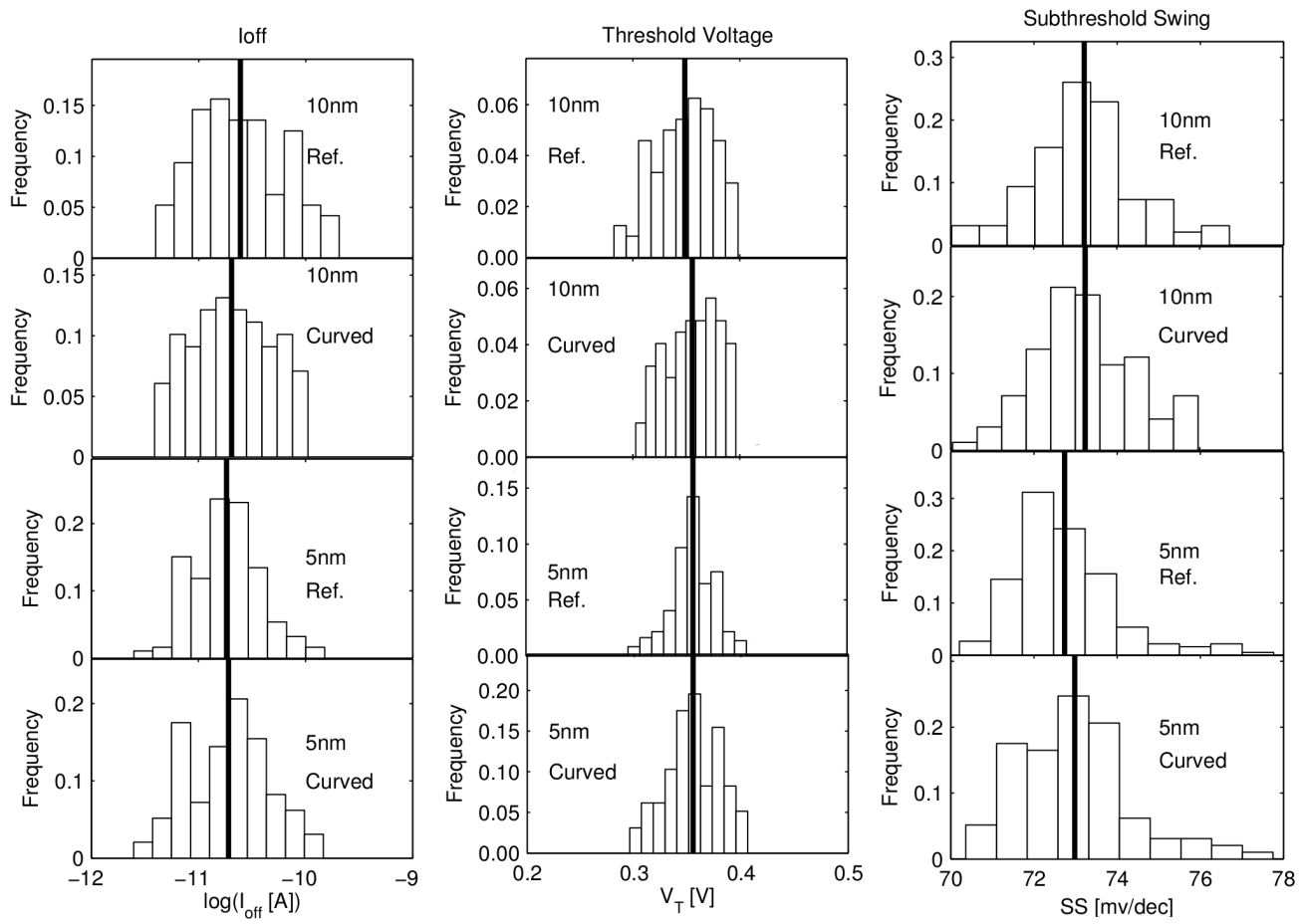

Fig. 5. Histograms for the simulated I_{off} (off-current), V_T (threshold voltage) and SS (subthreshold swing), showing the four possible parameter combinations of the curvature ('block' and 'curved') and the grain diameter (10 nm and 5 nm), vertically stacked to have a common x-axis. The mean of the data is shown by a thick black line in every plot.

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