A Physical Model to Predict Grain Boundary Induced Transistor Threshold Voltage Variation in Poly-Si TFTs

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***Abstract*—We present a physical model to capture the effect of grain boundaries (GBs) on the threshold voltage (V_{th}) variations in polysilicon thin-film transistors (poly-Si TFTs) considering the number, the position, and the orientation of GBs. The proposed model is extensively verified with 3-D drift-diffusion device simulator and experimental data. Using the proposed model, the impact of GBs on variability of transistor threshold voltage (V_{th}) and circuit performance is discussed for different grain sizes, device sizes, source-drain voltages and crystallization methods (such as sequential lateral solidification, SLS).**

Keywords-Poly-Si, GB-induced variations, grain boundary, threshold voltage variation, physical model

I. INTRODUCTION

Random distribution of Grain Boundaries (GBs) in poly-Si TFTs leads to large variations in the performance of TFTs. Hence, to facilitate poly-Si TFT technology for future applications, there is a need for modeling transistor threshold voltage (V_{th}) variation due to GBs. The existing simulation methods, which are based on drift-diffusion model [1] and ignore the impact of GB location in 2-D space [2], fail to meet accuracy. We propose a new physical model for GB-induced V_{th} variation in poly-Si TFTs. Compared to the existing literature, the salient features of the proposed model are as follows: 1) it takes into account the position of GBs in the channel, 2) it is applicable to both long and short channel devices, 3) the model can consider different crystallization methods (i.e. periodic or randomly distributed GBs), 4) it is analytical (i.e. the threshold voltage is derived in closed form) and, 5) it is computationally fast (~200x faster compared to 3-D device simulator [3]).

II. MODEL DESCRIPTION

The proposed approach determines variation in V_{th} by evaluating surface potential (Ψ), which is modeled by considering the applied voltages and the effect of GBs in the channel.

$$\Psi(x,y) = U(x,y,0) + \Phi_{gb}(x,y,0) \tag{1}$$

where U is the electrostatic potential due to the applied voltages, Φ_{gb} is the electrostatic potential contributed by GBs, x is along the direction of device length and y is along the direction of device width.

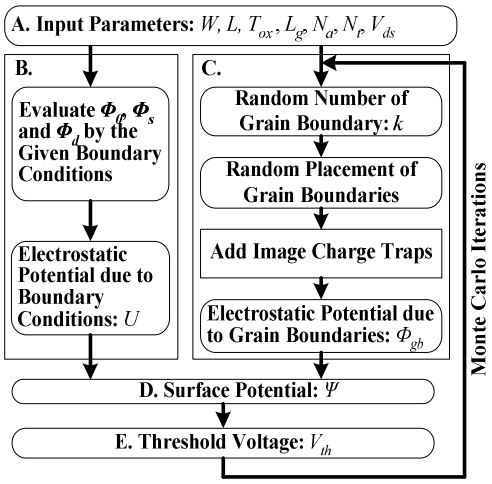

Fig. 1 Illustration of the effect of the RC delay of busline and GB-induced variations on pixel luminance.

The flowchart of the proposed simulation methodology is shown in Fig. 1. Simulation begins by inputting basic parameters which are necessary to define the geometry and the behavior of a poly-Si TFT. These input parameters include: 1) device width W, 2) device length L, 3) oxide thickness T_{ox}, 4) average grain size L_g, 5) doping profile N_a, 6) trap density of GBs (N_t), and 7) drain-source voltage V_{ds}. In step B, the electrostatic potential due to applied voltages is evaluated using the superposition principle [4],

$$U(x,z) = \Phi_0(x,z) + \Phi_S(x,z) + \Phi_d(x,z) \tag{2}$$

where Φ_0 is the solution of the Poisson equation that satisfies the boundary conditions in the gate electrode, Φ_S and Φ_D are solutions to Laplace equation that satisfy the boundary conditions at the source and drain electrodes, respectively. These solutions are derived in [4]. Step C determines the electrostatic potential due to GBs (Φ_{gb}). The number of GBs in the channel is first modeled using Poisson distribution.

$$P(k) = \frac{e^{-\lambda}\cdot\lambda^k}{k!}, \lambda = \frac{L}{L_G} + \frac{W}{L_G} \tag{3}$$

where k is the number of GB in the channel and λ is the mean of the number of GBs in the channel. Each randomly distributed GB is then described using four randomly assigned

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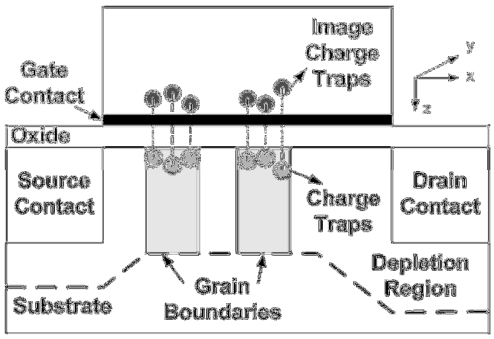

Fig. 2 Vertical cross section of TFT illustrating real and image charge traps (which are symmetrically added in the gate side).

variables (V_1-V_4) which are uniformly distributed between 0 and 1 and can be expressed as:

$$\begin{aligned} &V_1 x + (1-2K)\cdot V_2 y = -KV_2 W + (V_2 W + V_1 L)\cdot V_3 \\ &0 < V_4 \le 0.5 : K = 0 \\ &0.5 < V_4 \le 1 : K = 1 \end{aligned} \tag{4}$$

V_1 and V_2 determine the angle between the vector and x-axis, while V_4 is represents the incline of the vector. V_3 is related to the location of the cross point between the GB and x-axis. Note that, as indicated in the equations for V_4, the probability of the vector inclining to the positive x-direction is the same as that for the negative direction. Having specified the location of GBs in the device, Φ_{gb} is evaluated using Coulomb's Law in which the potential contribution of each charge trap in GB (Φ_i) and the mirror charge (Φ_i') is considered [5], as illustrated in Fig. 2.

$$\Phi_i(x,y,z) = \frac{-qD_{tr}}{4\pi\varepsilon_{si}R_i(x,y,z)} \tag{5}$$

$$\Phi_i'(x,y,z) = \frac{qD_{tr}}{4\pi\varepsilon_{si}R_i'(x,y,z)} \tag{6}$$

$$\Phi_{gb}(x,y,z) = \sum_{i=1}^{N}(\Phi_i(x,y,z) + \Phi_i'(x,y,z)) \tag{7}$$

In the above equations, D_{tr} is the density of the charge trap, R_i is the distance of the charge trap in the GB to the evaluated point while R_i' is the distance between the image charge trap and the evaluated point and z is the direction along the

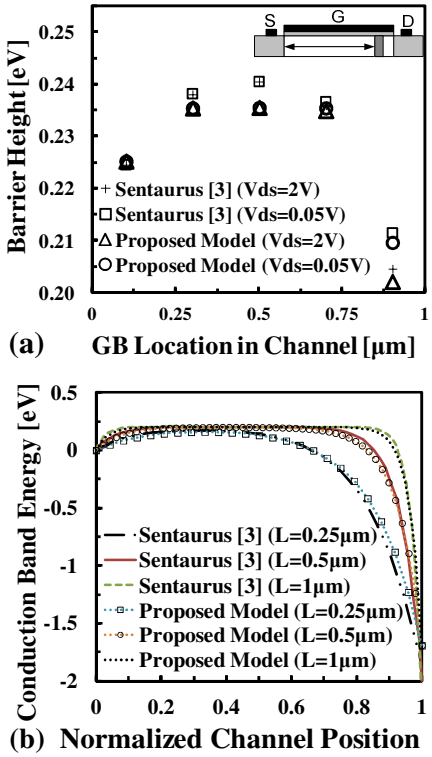

Fig. 4 Comparison of simulation results from the proposed model and 3-D device simulator [3]. (a) Maximum barrier height with different position of GBs (b) Conduction band with different L.

substrate thickness. In step D, the surface potential is obtained by the superposition of U and Φ_{gb} as shown in Fig. 3. V_{th} can be determined from the surface potential. To define V_{th}, the channel is divided into parallel "lanes" where the electrons move from source to drain contact laterally. With such gate slicing method [5]-[7], the local threshold voltage (V_t) is determined by the maximum surface potential across the "lane".

$$V_t(y) = \max_{x=(0\ldots L)}\left(\Psi(x,y) + \frac{\sqrt{2\varepsilon_{si}\cdot qN_A\Psi(x,y)}}{C_{ox}}\right) \tag{8}$$

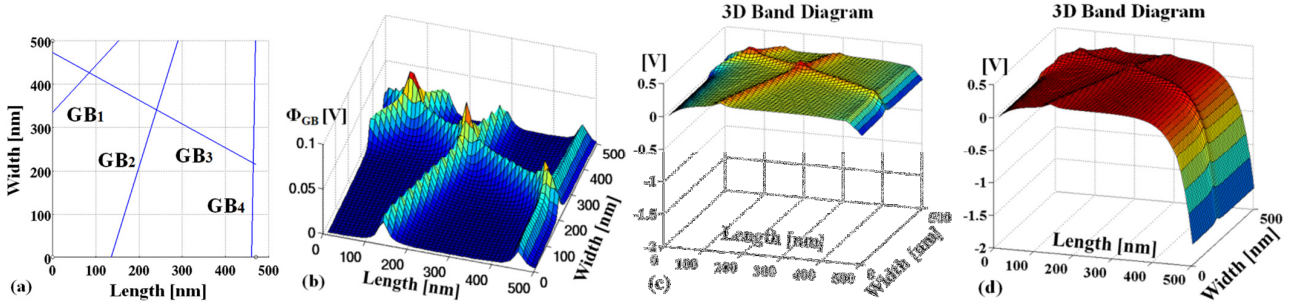

Fig. 3: (a) Vectors in random location and direction indicating the random orientation of four GBs in the TFT channel (W=L=0.5μm), (b) surface potential due to charged traps in the GBs (Φ_{GB}) evaluated by Coulomb's law. 3-D Band diagram evaluated using the proposed model for (c) low V_{ds} and (d) high V_{ds}.

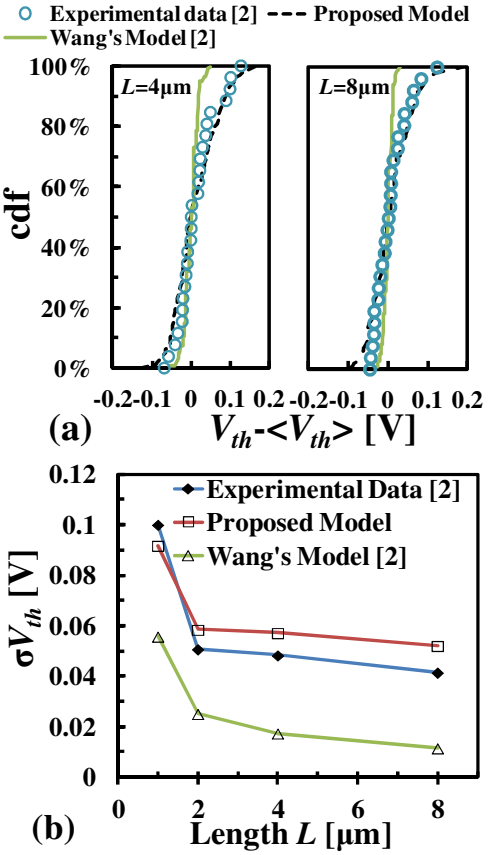

Fig. 5 Comparison of (a) cumulative distribution function and (b) standard deviation of V_{th} obtained from the proposed model, experimental data [2] and Wang's model [2] for different device length L. (W=8μm, mean L_g= 0.4μm, T_{ox}=0.03μm, V_{ds}=2V)

Finally, V_{th} is obtained by averaging all V_t of the lanes [5]-[7].

$$V_{th} = \frac{1}{W}\int_0^W V_t(y)dy \qquad (9)$$

Noted that, if the current along the width is comparable to the current along the device length, the assumption regarding the same direction of the current in each channel has to be corrected [6]. This process is repeated for all the samples (Monte Carlo analysis), which have different number and location of GBs, to determine the distribution of V_{th}.

III. Model Verification, Results and Discussions

In this section, the efficacy of the proposed framework is verified with 3-D drift-diffusion device simulator [3] and experimental data [2]. Then we describe the simulated statistical results under various conditions for device and circuits.

In Fig. 4a, the maximum barrier heights with different positions of GB obtained by our model and 3-D device simulator [3] are compared. Note that the maximum barrier height is modulated significantly if the GB position is in the middle of the channel. However, if the GB position is close to the source or the drain, the transistor V_{th} is minimally affected since the GB-induced barrier is nullified by the lateral electric field. In Fig. 4b, we demonstrate the applicability of the proposed model by comparing the conduction band diagrams for a wide range of technology nodes, sweeping the gate length from 250nm to 1μm.

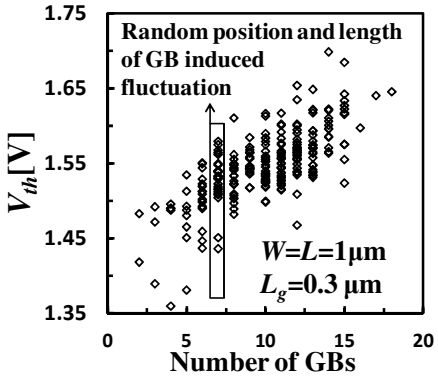

Fig. 6 V_{th} distribution of a sample set of 250 transistors.

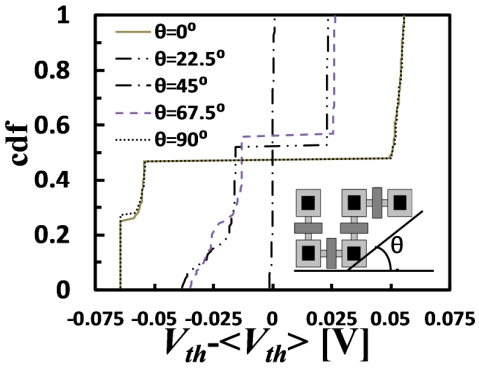

Fig. 7 Comparison of cumulative distribution of V_{th} with different angle of periodic GBs using the proposed model.

Fig. 5 shows our statistical analysis in comparison to that of previous work [2] and experimental data [2]. It is evident that the standard deviation of V_{th} (σ_{Vth}) from the proposed model has better agreement with experimental data [2] for different device lengths. The results obtained by the previous work [2] have significantly low σ_{Vth}, since the model only considers the number of GBs in the channel but not their location [2].

For a fixed number of GBs within the device channel, we are able to observe the distribution of threshold voltage due to the random position of GBs. Fig. 6, for a sample set of 250 TFTs, illustrates the threshold voltage distribution as a function of the number of GBs. It is clear that a large variation in threshold voltage can occur for the same number of GBs, while the mean of the threshold voltage increases with the number of GBs. Consequently, the large variations (even when the number of GB's is kept constant) verify the significant role of the position of GBs on V_{th}.

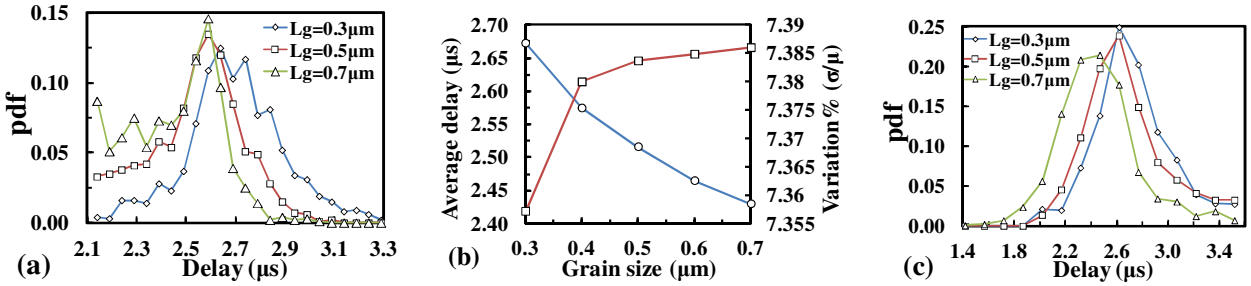

Fig. 8 (a) Statistical delay distribution of a single-stage inverter when average grain sizes are in the range of 0.3 to 0.7 μm. (b) Improvement in normal delay of a single-stage inverter with enlarging grain size at the cost of increased variations (σ/μ). (c) Statistical delay distribution of a 20-stage inverter chain when average grain sizes are in the range of 0.3 to 0.7 μm.

By simply changing the random vectors to periodic vectors for describing the locations of GBs, the proposed framework can also predict the effect of periodic GBs on V_{th} variation. Fig. 7 shows the cumulative distribution function (cdf) for different angles (θ) of periodic GBs induced by SLS [8]. It is shown that V_{th} variation is minimal when $\theta=45^0$. This can be attributed to the fact that the devices have relatively the same number and position of GBs when $\theta=45^0$, which has also been experimentally observed in [8].

Based on the above characterization of V_{th}, in Fig. 8, we evaluate the impact of GBs at the circuit level. We observe that, as the grain size approaches the device size, the randomly distributed GBs induce a non-Gaussian delay distribution for a single-stage inverter, as shown in Fig. 8a. Hence, for circuits having low logic-depth (such as pixel circuit of display and memory cell), the delay distribution cannot be evaluated using a Gaussian-distribution-based analysis when the grain size is comparable to the device size. Fig. 8b shows that increasing grain size can improve circuit performance at the cost of delay variations. Note that, with the increase in logic depth, the multimodal distribution converged to unimodal distribution regardless of the grain size, as shown in Fig. 8c. However, the dependence of average delay on the grain size is still clear.

In Fig. 9, we compare the delay of a single-stage inverter with different multi-finger TFTs. The less spread of delay distribution in a 4-finger TFT shows the effectiveness of multi-finger structure for minimizing GBs-induced V_{th} variation. This is due to the fact that the unbalanced current drivability of each finger compensates each other.

IV. Conclusion

We propose, for the first time, a physical model which simultaneously considers the impact of the number, the position, and the orientation of GBs on V_{th} variations. The applicability of proposed framework is demonstrated for different technology nodes and crystallization methods. We have shown that the spread of threshold voltage and delay increase significantly and is non-Gaussian when the grain size is comparable to the device size. These statistical attributes pose an intrinsic barrier to further scaling of supply voltage and device size. The fast computation time and the flexibility of the proposed framework make it suitable for fast circuit simulations.

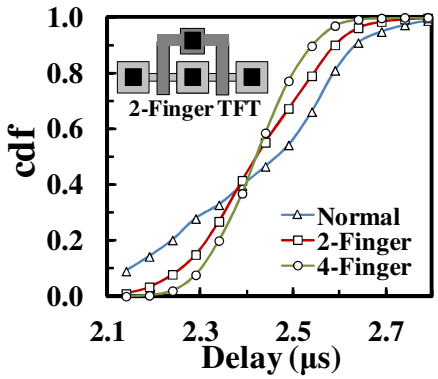

Fig. 9 Cumulative distribution of propagation delay in a single-stage inverter with different multi-finger TFTs. (L_g = 0.7μm)

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