Analytical Model for the Threshold Voltage Variability due to Random Dopant Fluctuations in Junctionless FETs

Antonio Gnudi, Susanna Reggiani, Elena Gnani, Giorgio Baccarani
Dept. of Electronics DEIS/ARCES
University of Bologna
Viale Risorgimento, 2, 40136 Bologna, Italy
agnudi@arces.unibo.it

Abstract—**An analytical model of the threshold voltage variance induced by random dopant fluctuations (RDF) in junctionless (JL) FETs is derived for both cylindrical nanowire (NW) and planar double-gate (DG) structures considering only the device electrostatics in subthreshold. The model results are shown to be in reasonable agreement with TCAD simulations for different gate lengths and device parameters. The results confirm previous indications that the threshold voltage fluctuations are a serious concern for nanometer-scale JL FETs.**

FET; junctionless; nanowire; double-gate; random dopant fluctuations; threshold voltage variability

I. Introduction

The JL FET has been proposed as a means to avoid the fabrication problem of sharp source-drain junctions in nanometer-scale FETs [1-2]. The projected performance of JL FETs has been investigated theoretically both for the planar UTB-SOI [3] and for the NW topology [4-5]. Also the variability due to RDF has been investigated [6-7], showing the rather poor performance of the JL FET with respect to its enhancement mode counterpart. In [7] analytical models for the threshold-voltage standard deviation σ_{Vt} have been derived for planar DG and NW JL FETs, based on the analysis of the device electrostatics above threshold in the presence of RDF. In this paper, as a complement to [7], the analytical σ_{Vt} models are extended to the subthreshold region of DG and cylindrical NW JL transistors, thus providing a continuous expression across the threshold voltage. The model is validated against numerical TCAD simulations and the obtained results confirm the very large RDF-induced threshold-voltage variability of JL transistors.

II. Model Derivation

Let us consider first a cylindrical *n*-doped NW JL transistor. The derivation of the analytical model for σ_{Vt} is based on the following simplifying assumptions: i) only the device electrostatics is taken into account, i.e. the effect of mobility and current path variations in the channel due to RDF are neglected; ii) the channel is assumed to be uniformly doped in the nominal condition with donor concentration N_D; iii) the potential profile is considered to be uniform along the transport direction, i.e. $V_{DS} \to 0$ and the fringing fields due to the source-drain junctions are neglected; iv) linear response to the doping variations with respect to the nominal case is assumed. By virtue of the above assumptions, one can consider the response to the fluctuation of the doping concentration $\delta N_D(r)$ integrated along the angular and longitudinal cylindrical coordinates φ and x, thus reducing the variational problem to an effectively one-dimensional one in the radial coordinate r. Assuming that the electron concentration in subthreshold is negligible with respect to the doping concentration, the variation $\delta\psi(r)$ of the electrostatic potential can be written as follows by integrating the Poisson equation

$$\delta\psi(r) - \delta\psi(R_s) = \frac{q}{\varepsilon_{\mathrm{Si}}} \int_r^{R_s} \frac{\mathrm{d}r'}{r'} \int_0^{r'} \delta N_D(r'') r'' \mathrm{d}r'' \quad (1)$$

$$C_{\mathrm{ox}}[\delta\psi(R_s) - \delta V_G] = q \int_0^{R_s} \delta N_D(r) 2\pi r \mathrm{d}r \quad (2)$$

where R_S is the Si NW radius and C_{ox} the oxide capacitance per unit length given by $C_{ox} = 2\pi\varepsilon_{ox} / \ln(1 + t_{ox} / R_S)$. In addition, the variation of the electron charge per unit length δQ_n can be expressed as

$$\delta Q_n = -q \int_0^{R_s} \frac{q n_o(r)}{k_B T} \delta\psi(r) 2\pi r \mathrm{d}r \quad (3)$$

$$n_o(r) = n_o(0) \exp\left[-\frac{q^2 N_D}{4\varepsilon_{\mathrm{Si}} k_B T} r^2\right] \quad (4)$$

where $n_0(r)$ given by (4) is the electron concentration in the nominal condition. The threshold voltage variation δV_t is then found from the above equations as the value of δV_G for which $\delta Q_n = 0$. Finally, the variance σ_{Vt}^2 can be calculated as the ensemble average of δV_t^2 over all possible doping profiles. To this end, a Poisson distribution is assumed for the dopants, which leads to the following expression of the correlation function for $\delta N_D(r)$

This work has been supported by the EU ENIAC Project MODERN (contract 216537) via the IUNET consortium.

ISBN 978-0-615-71756-2

$$\overline{\delta N_D(r_1)\delta N_D(r_2)} = \frac{N_D}{2\pi r_1 L}\delta(r_1 - r_2) \qquad (5)$$

where the overbar denotes ensemble average and δ(r) the Dirac function. The exact evaluation of σ_{Vt}^2 can be carried out only through a numerical integration. However, all the integrals can be easily evaluated analytically with the approximation of the Debye length $\lambda_D = [(\varepsilon_{Si}\, k_B\, T) / (q^2\, N_D)]^{1/2} << R_S$, which is well justified in properly scaled transistors with high doping levels. The final result is

$$\sigma^2_{\mathrm{NWV_T}} = \frac{q^2 N_D R_S^2}{L}\left[\frac{1}{8\pi\varepsilon^2_{\mathrm{Si}}} + \frac{\pi}{C^2_{\mathrm{ox}}} + \frac{1}{2C_{\mathrm{ox}}\varepsilon_{\mathrm{Si}}}\right] \qquad (6)$$

A similar procedure is adopted for the DG JL FET, leading to

$$\sigma^2_{\mathrm{DGV_T}} = \frac{q^2 N_D t_S}{2WL}\left[\frac{t_S^2}{3\varepsilon^2_{\mathrm{Si}}} + \frac{t_S}{C'_{\mathrm{ox}}\varepsilon_{\mathrm{Si}}} + \frac{1}{(C'_{\mathrm{ox}})^2}\right] \qquad (7)$$

In (7) C'_{ox} and t_S are the oxide capacitance per unit area and half the Si layer thickness of the DG JL FET, respectively.

In [7] similar expressions for the σ_{Vt}^2 of NW and DG JL FETs were derived based on the same simplifying assumptions mentioned at the beginning of this section, but focusing on the above-threshold regime rather than subthreshold and assuming an abrupt transition between the neutral and the depletion region. The latter assumption is consistent with the Debye length $\lambda_D << R_S$ taken in this paper. The result obtained in [7] for NW JL FETs is reported hereafter for reference

$$\sigma^2_{\mathrm{NWV_T}} = \frac{q^2 N_D}{L_{\mathrm{eff}}}\left[\frac{1}{4\pi\varepsilon^2_{\mathrm{Si}}}\left(R_o^2 \ln\frac{R_o}{R_s} + \frac{R_s^2 - R_o^2}{2}\right) + \right. \\ \left. + \frac{1}{C_{\mathrm{ox}}\varepsilon_{\mathrm{Si}}}\frac{R_s^2 - R_o^2}{2} + \frac{2\pi}{C^2_{\mathrm{ox}}}\frac{R_s^2}{2}\right] \qquad (8)$$

where R_0 is the radius of the neutral region. Also in this case δV_t is calculated as the variation of the gate voltage which is necessary to maintain the channel charge constant, compensating for the doping fluctuations. It should be noticed that, as expected, (8) reduces to (6) when $R_0 \rightarrow 0$, i.e. in the subthreshold limit. Similar considerations apply to the DG JL FET.

For completeness, we also report hereafter the expressions of the nominal threshold voltages for the two FET types, which can be easily derived under the above assumptions and are used in the discussions of the next sections:

$$V_{\mathrm{TNW}} = \Phi_{MS} - qN_D R_S^2\left[\frac{\pi}{C_{\mathrm{ox}}} + \frac{1}{4\varepsilon_{\mathrm{Si}}}\right] \qquad (9)$$

$$V_{\mathrm{TDG}} = \Phi_{MS} - qN_D t_S\left[\frac{1}{C'_{\mathrm{ox}}} + \frac{t_S}{2\varepsilon_{\mathrm{Si}}}\right] \qquad (10)$$

III. Model Validation

The proposed analytical models (6) and (7) have been compared with the results of TCAD simulations carried out both

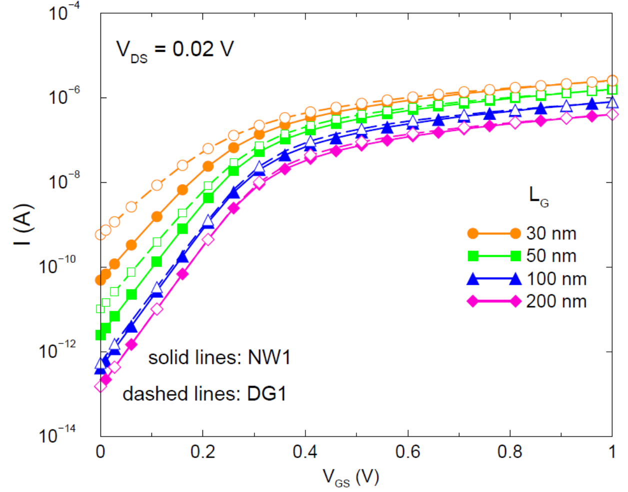

Figure 1. Simulated turn-on characteristics of the NW1 (filled symbols) and DG1 (empty symbols) FET families defined in the text for different gate lengths at V_{DS} = 20 mV.

with statistical atomistic and with the linear Green function methods [8]. Two families of NW FETs with different parameters have been simulated, the first, hereafter referred to as NW1, with R_s = 10 nm, t_{ox} = 2 nm, $N_D = 10^{19}$ cm^{-3}, the second (NW2) with scaled parameters (R_s = 5 nm, t_{ox} = 1 nm, $N_D = 4\cdot10^{19}$ cm^{-3}), so as to give the same threshold V_t = 0.32 V for a gate Φ_{MS} = 1.12 eV according to (9). Similarly, two families of DG FETs have also been simulated, the first (DG1) with t_s = 10 nm, t_{ox} = 2 nm, $N_D = 4.43\cdot10^{18}$ cm^{-3}, W = 25 nm, the second (DG2) with t_s = 5 nm, t_{ox} = 1 nm, $N_D = 1.77\cdot10^{19}$ cm^{-3}, W = 12.5 nm: widths and doping concentrations have been chosen so as to have approximately the same threshold voltage given by (10) and channel conductivity at low V_{DS} of the NW counterparts. Fig. 1 reports the simulated turn on characteristics for the NW1 and DG1 FET families for different gate lengths ranging from 30 nm to 200 nm. It is seen that while for long channel lengths the two families with the chosen parameters give almost identical characteristics, they exhibit different subthreshold slopes for short gate lengths, due to short channel effects that are more pronounced for the DG device, as expected.

The results of the analytical models and TCAD simulations for σ_{Vt} are collected in Fig. 2. For the scaled families NW2 and DG2 the shortest simulated channel length is 20 nm. It is seen that an overall acceptable agreement is obtained for all considered devices, the maximum relative error between models and simulations being less than 10%. The two DG devices exhibit the largest errors, due to the limited accuracy of the uniform-channel assumption related to 2D electrostatic effects. It is also interesting to notice that atomistic simulations are in fairly good agreement with linear Green-function simulations, justifying the basic assumption of the linear-response model.

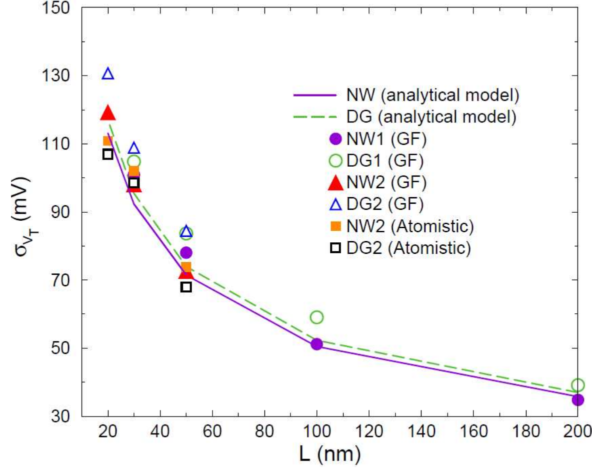

Figure 2. Threshold-voltage standard-deviation σ_{Vt} vs. gate length obtained with the model equations (6) and (7) (lines) and with TCAD (symbols) Green function-based (GF) and atomistic-based simulations for the NW and DG JL FETs families NW1, NW2, DG1, DG2 defined in the text.

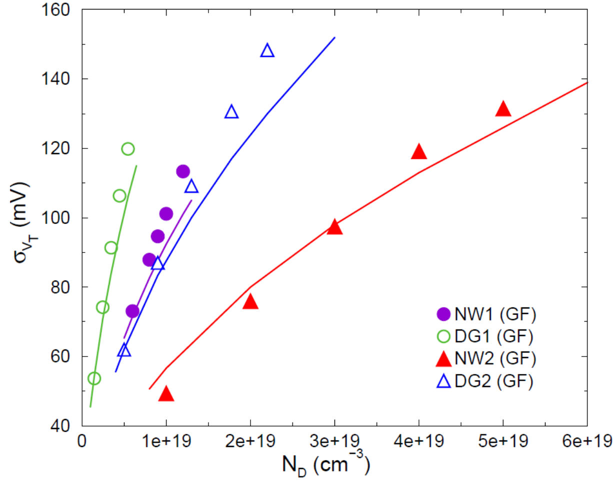

Figure 3. Threshold-voltage standard-deviation σ_{Vt} vs. doping concentration obtained with the model equations (6) and (7) (lines) and with TCAD Green function simulations (symbols) for the NW and DG JL FETs families NW1, NW2, DG1, DG2 defined in the text. For NW1 and DG1 $L = 30$ nm, for NW2 and DG2 $L = 20$ nm.

Fig. 3 shows analytical and simulation results as a function of N_D for the various device families, with $L = 30$ nm for NW1 and DG1, $L = 20$ nm for NW2 and DG2, corresponding to different threshold voltages. The worst case error between models and simulations is below 15%. The error decreases with N_D due to the reduction of 2D effects and is again generally lower for NW FETs.

IV. Discussion of Results

With the help of (6) and (7) it is easy to understand the impact of the device parameters on the threshold variability. The analytical values of σ_{Vt} are shown in fig. 4 as a function of the relative permittivity κ of the gate dielectric for the NW1 and DG1 devices with $L = 30$ nm. As expected, the use of a high-κ dielectric improves the RDF-induced variability due to the stronger electrostatic gate control. Fig. 4 indicates that for high values of κ, DG1 is slightly favoured. However, this conclusion could be misleading, because it must be recalled that the DG1 parameters (doping and width) have been chosen so as to match the NW1 characteristics for κ = 3.9.

It is interesting to observe that the σ_{Vt} given by (6) and (7) can be expressed in terms of the total source/drain extrinsic resistances $R_{s/d}$. In the high-κ limit, when the second and the third terms in brackets in (6) and (7) can be neglected, σ_{Vt} can be written as

$$\sigma^2_{\mathrm{NWV_T}} = \frac{1}{R_{\mathrm{s/d}}} \frac{L_{\mathrm{s/d}}}{L} \frac{q}{4\mu\pi^2\varepsilon^2_{\mathrm{Si}}} \tag{11}$$

$$\sigma^2_{\mathrm{DGV_T}} = \frac{1}{R_{\mathrm{s/d}}} \frac{L_{\mathrm{s/d}}}{L} \left(\frac{t_S}{W}\right)^2 \frac{q}{6\mu\varepsilon^2_{\mathrm{Si}}} \tag{12}$$

where $L_{s/d}$ is the length and μ the electron mobility of the source/drain neutral regions. The above expressions clearly show a fundamental limitation of the JL FETs, which exhibit a hard-to-break trade-off between threshold variability and parasitic resistance. It should also be noticed that $R_{s/d}$ does not include the contribution of the contact resistances. For example, with reference to a 20-nm diameter NW FET case, assuming $L \cong L_{s/d}$, $\mu \cong 100$ cm^2/Vs and $R_{s/d} \cong 5$ kΩ, in line with the ITRS prescription [9] of a total parasitic resistance of ≅ 200 Ω µm and assuming half of this value is due to the source/drain contribution, it turns out from (11) that σ_{Vt} can not be lower than nearly 80 mV, a quite large value for most applications.

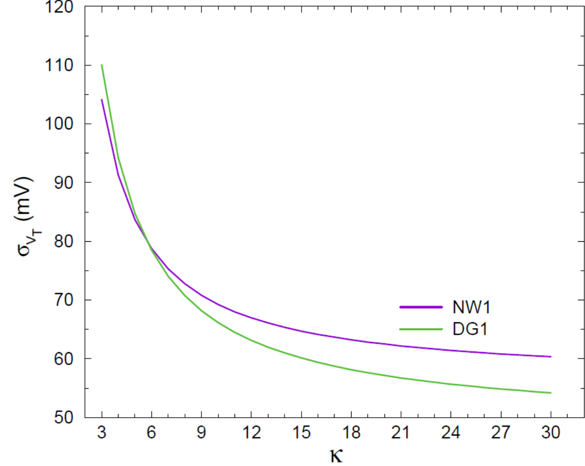

Figure 4. Threshold-voltage standard-deviation σ_{Vt} vs. dielectric constant κ obtained with the model equations (6) and (7) for the NW1 and DG1 families defined in the text with $L = 30$ nm.

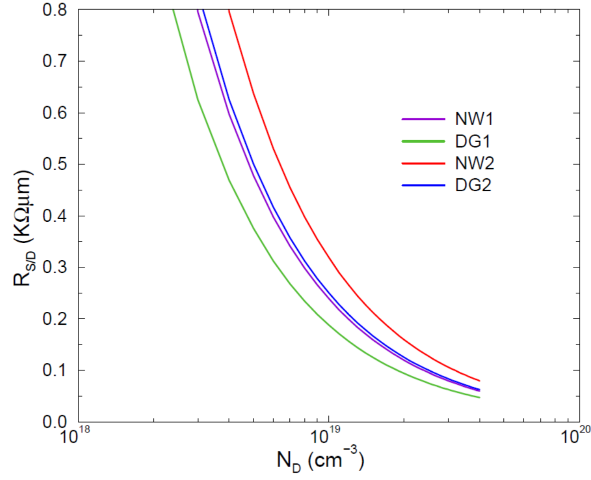

Figure 5. Total series source/drain resistance vs. doping concentration calculated for the device families NW1, NW2, DG1, DG2 defined in the text. The resistance is normalized to the width for DGs, to the diameter for NWs. For NW1 and DG1 L = 30 nm, for NW2 and DG2 L = 20 nm. The source/drain lengths have been taken equal to the channel lengths.

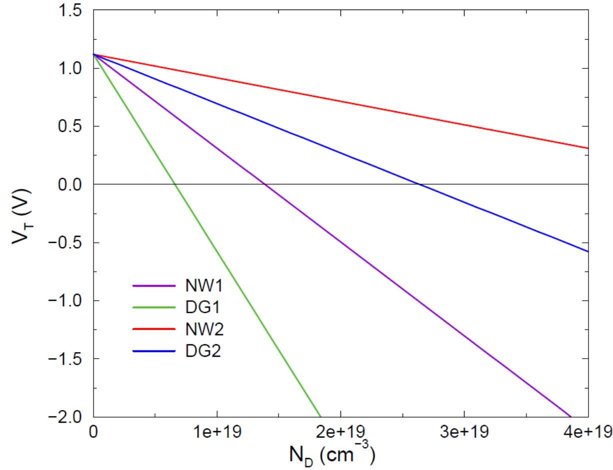

Figure 6. Threshold-voltage vs. doping concentration calculated with the model equations (9) and (10) for the NW and DG JL FETs families NW1, NW2, DG1, DG2 defined in the text. The gate work function Φ_{MS} = 1.12 eV.

For a more precise and complete calculation, the total source/drain series resistances for the four considered device types are plotted in Fig. 5 vs. doping concentration, again assuming $L = L_{s/d}$ and μ = 100 cm^2/Vs. The resistances are normalized to the width for DG FETs and to the diameter for NW FETs for an easier comparison with the prescriptions of [9]. It is seen that for the resistance values implied in [9] doping values above 10^{19} cm^{-3} are required in all cases. The corresponding σ_{Vt} can be deduced from Fig. 3, confirming the difficulties outlined above in achieving an acceptable σ_{Vt}, and the necessity of adopting specific technological solutions to reduce the series source/drain resistance.

Provided the parasitic resistance problem is circumvented somehow, from Fig. 3 it turns out that reasonable values of σ_{Vt} can be obtained only with low doping levels, typically smaller than 5×10^{18} cm^{-3}. This may imply the choice of a gate work function different from what used so far in the discussion. Fig. 6 reports the nominal threshold voltages for the device families as given in (9) and (10) with Φ_{MS} = 1.12 eV as a function of doping concentration. Clearly for low doping levels a lower Φ_{MS} is necessary for a threshold voltage around 0.3 V.

V. CONCLUSIONS

An analytical model has been presented for the threshold voltage variability due to RDF in NW and DG JL FETs. The model is consistent with previous analytical expressions derived in the above-threshold regime. The model has been validated for well scaled devices up to 10-nm diameter (or silicon thickness) and 20-nm gate length through comparisons with TCAD simulations carried out both with the Green-function method and with the atomistic statistical method. A fundamental limitation of such JL FETs has been outlined, namely a difficult-to-break trade-off between threshold variability and source/drain series resistance. Provided the series resistance problem is solved by means of special technological solutions, reasonable values of σ_{Vt} can be achieved only by keeping the doping level well below 5×10^{18} cm^{-3}.

REFERENCES

[1] C.-W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, and J.-P. Colinge, “Junctionless multigate field-effect transistor”, *Appl. Phys. Lett.*, vol. 94, no. 5, p. 053511, 2009.

[2] J.-P. Colinge et al., “Nanowire transistors without junctions”, *Nat. Nanotechnol.*, vol. 5, no. 3, pp. 225–229, 2010.

[3] E. Gnani, A. Gnudi, S. Reggiani, and G. Baccarani, “Physical model of the junctionless UTB SOI-FET”, *IEEE Trans. on Electron Devices*, vol. 59, no. 4, pp. 941-948, 2012.

[4] B. Sorée, W. Magnus, and G. Pourtois, “Analytical and self-consistent quantum mechanical model for a surrounding gate MOS nanowire operated in JFET mode”, *J. Comput. Electron.*, vol. 7, no. 3, pp. 380–383, 2008.

[5] E. Gnani, A. Gnudi, S. Reggiani, and G. Baccarani, “Theory of the junctionless nanowire FET”, *IEEE Trans. Electron Devices*, vol. 58, no. 9, pp. 2903-2910, 2011.

[6] M. Aldegunde, A. Martinez, and J.R. Barker, “Study of discrete doping-induced variability in junctionless nanowire MOSFETs using dissipative quantum transport simulations”, *IEEE Electron Device Lett.*, vol. 33, no. 2, pp. 194-196, 2012.

[7] A. Gnudi, S. Reggiani, E. Gnani, and G. Baccarani, “Analysis of threshold voltage variability due to random dopant fluctuations in junctionless FETs”, *IEEE Electron Device Lett.*, vol. 33, no. 3, pp. 336-338, 2012.

[8] Synopsys Inc., “Sentaurus device simulator (release D-2010.03),” 2010.

[9] International Technology Roadmap for Semiconductors, 2011 Report Edition.