Statistical TCAD Based PDK Development for a FinFET Technology at 14nm Technology node

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Abstract—**A TCAD-based process design kit (PDK) development strategy is present for a generic SOI-based FinFET technology targeted at the 14nm technology node. It enables the circuit design exploration and benchmarking at the early technology development stage. Its application for transistor - SRAM cell design and co-optimisation is discussed.**

Keywords-FinFET; PDK; SRAM; Statistical Variability; Compact Model

I. INTRODUCTION

With the traditional bulk MOSFET architecture reaching scaling limits due to excessive random discrete dopant fluctuation [1], new variability-resilient device architectures, such as FinFETs and ultra thin body (UTB) SOI devices, are required in order to maintain the benefits of technology scaling at the 22nm node and beyond [2,3]. From the circuit and system designer's perspective, a reliable process design kit (PDK) at the early stages of new technology development, can allow design exploration and benchmarking. Before actual silicon data becomes available, physics-based TCAD simulations can provide accurate information regarding new device characteristics and performance. In this study, a TCAD physics-based PDK development strategy, driven by the GSS 'atomistic' simulator GARAND and compact model extractor MYSTIC [4], is presented for a generic SOI-based FinFET technology targeted at the 14nm technology node. The PDK will be used in the evaluation of SRAM subsystem design.

II. DEVICE DESIGN AND STATISTICAL VARIABILITY

A. Device Design and Uniform Device Simulation

The schematic view of a DG SOI FinFET corresponding to a generic 14nm technology node is depicted in Fig.1. The device doping profile is illustrated in Fig.2 with a background doping of 1×10^{15} cm^{-3} in the channel region to minimize the impact of random discrete dopants on device characteristics. The device geometry corners and performance at an operating temperature of 85°C with nominal geometry configuration (L_G of 20nm, W_F of 10nm and H_F of 25nm) are presented in Table 1. The DIBL of n- and p-FinFETs are 56 and 65 mV/V, respectively, demonstrating the excellent electrostatic integrity that the FinFET architecture can offer.

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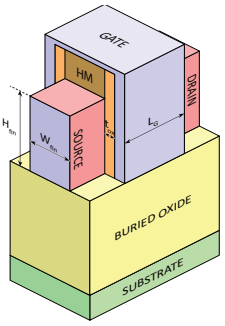

Fig.1 3D Schematic plot of the FinFET device.

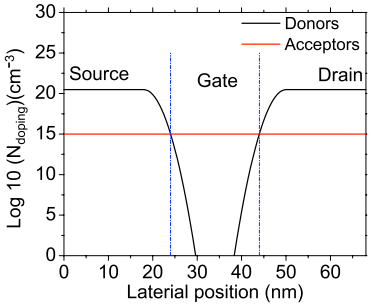

Fig.2 1D doping profile of the FinFET device with nominal geometry configuration.

Table 1 Device geometry corners and performance with nominal geometry configuration

Parameter	Min (nm)	Max (nm)
Gate Length, Lg	18	22
Fin Width, WF	8	12
Fin Height, HF	22	28
EOT	0.7	0.9

T=85°C V_{DD}=0.9V	NMOS	PMOS
I_{ON} (mA/μm)	0.9	0.8
I_{OFF} (nA/μm)	10	10
DIBL (mV/V)	56	65
SS (mV/Dec)	86	88

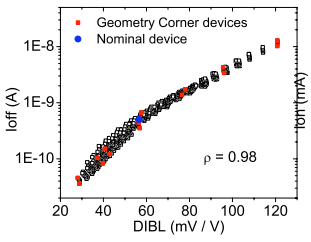

Fig.3 Correlation between DIBL and off-current for devices with various geometry configurations.

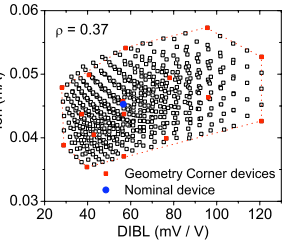

Fig.4 Correlation between DIBL and on-current for devices with various geometry configurations.

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Comprehensive device simulations are carried out to cover the full device geometry spectrum within the process corners, and provide detailed information that is important for long-range process variation (e.g. die to die, chip to chip). Sub-threshold figures of merit have strong inter-correlations, as depicted in Fig.3, while the independence between the sub-threshold and on-current regions is clearly demonstrated in Fig.4. Using on-current, I_{ON}, and overdrive current, I_{ODsat}, as examples, the dependences of the device figures of merit on the fin height, width and gate length are illustrated in Fig.5. For each fin height used, a plane shows the variation in the corresponding figure of merit with gate length and fin width. The planes on the back show the variation with fin height. Contour lines have been added to further clarify the variation.

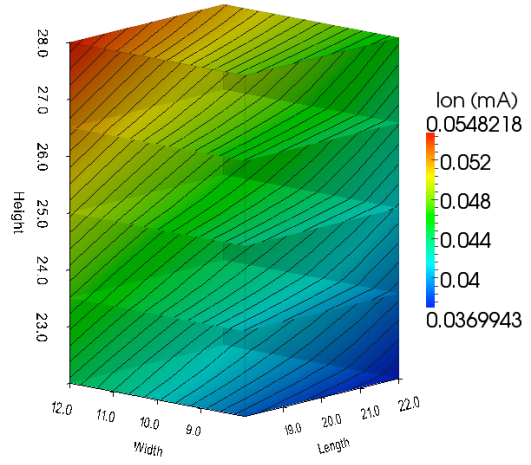

Fig.5 Distribution of (a) on-current and (b) overdrive current (under constant gate overdrive bias condition against V_{TH}) within the geometry corners. Planes showing the variation with gate length and fin width for different fin height.

Due to the fixed over-drive gate bias condition in I_{ODsat}, low threshold voltage value introduced by poor electrostatic integrity would not provide advantage on the over-drive current performance, and the best over-drive current corner corresponds to devices with the best short-channel-effect performance, which is in contrast to on-current behaviour where the highest on-current corner corresponds to the devices with the worst short-channel-effect performances.

The dependence of device electric figures of merit on the device geometry can be captured by parametric regression techniques, as demonstrated in Fig.6. The associated sensitivity information between device figures of merit and geometry parameters can be utilized to connect long-range variation and local statistical variation.

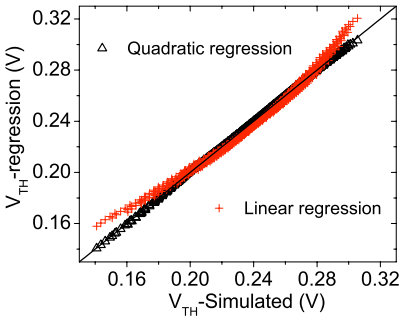

Fig.6 Reproduction of uniform device simulation with different geometry configurations by data regression

B. *Statistical Device Simulation*

Random discrete dopants (RDD), fin edge roughness (FER), gate edge roughness (GER) and metal gate granularity (MGG) are considered in this work, and comprehensive statistical variability studies are carried out to investigate the impact of statistical variability sources on device characteristics. In MGG simulation, TiN metal gate is assumed with two metal grain orientations, corresponding to two work-functions differing by 200mV occurring with probabilities of 40% and 60%. A typical fin configuration under the influence of RDD, FER and GER is depicted in Fig.7 with the top gate showing the metal grain pattern with average grain diameter of 10nm. Side-gates show the actually potential variation introduced by MGG, which is not only determined by the grain pattern, but also the grain orientation.

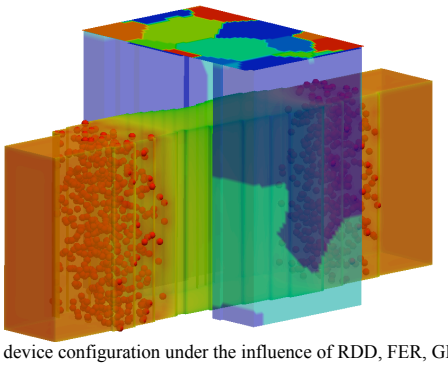

Fig.7 FinFET device configuration under the influence of RDD, FER, GER and MGG. In this case, the average grain diameter of MGG is 10nm.

As an example, Id-Vg characteristics of an ensemble of 1000 devices with nominal geometry configuration under the influence of combined statistical variability sources is depicted

in Fig.8, with 3σ of GER at 2nm and 3σ of FER at 1nm. It is shown that in this particular configuration, MGG with average grain size of 5nm can introduce an additional 60% and 58% increase in σV_{TH} and σI_{ON}, respectively.

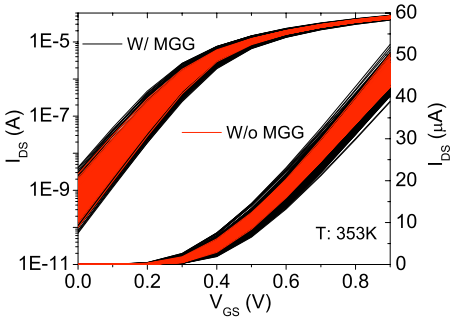

Fig.8 Id-Vg characteristics under the influence of combined statistical variability sources at drain bias of 0.9V. The average grain diameter of MGG is 5nm.

MGG can dramatically alter the correlations between sub-threshold figures of merit, as demonstrated in Fig. 9. Such information can be used to determine whether MGG is present as a significant statistical variability source for FinFETs with an undoped channel.

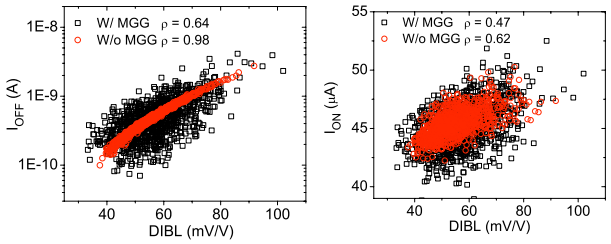

Fig.9 DIBL correlation with off-current and on-current under the influence of statistical variability

III. Compact Modell Extraction

Physics-based device TCAD simulations discussed in section II provide accurate information for PDK development of emerging technologies, while the corresponding compact model extraction is at the heart of PDK development. Fig.10 illustrates the development flow of a statistical compact model library. The main purpose of this workflow is to transfer all the information obtained from TCAD simulations into compact models that are ready to be used by designers.

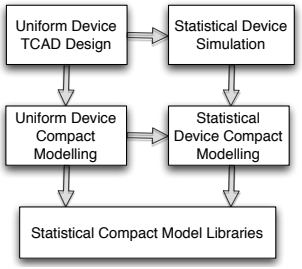

Fig.10 Statistical compact model library development flow

The surface-potential-based BSIM-CMG model [5] is used in this work, and a combination of local optimization and group device extraction strategy is developed for uniform-device compact model extraction. The I_D-V_G results of group extraction are presented in Fig.11, with the I_D-V_D of the nominal device depicted in Fig.12, demonstrating the quality of the uniform device compact modelling.

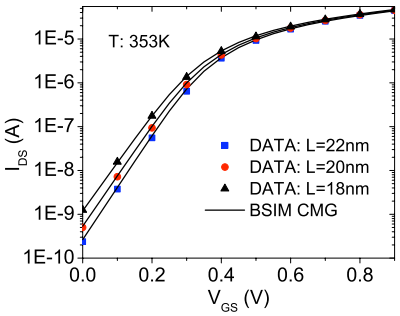

Fig.11 Id-Vg results of BSIM-CMG for device with different gate length

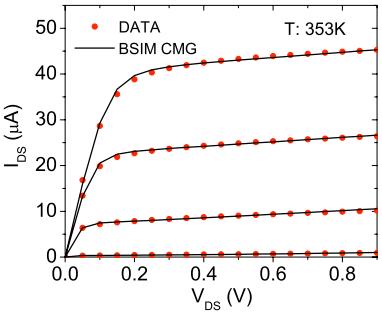

Fig.12 Id-Vd results of BSIM-CMG for a device with nominal geometry configuration

The uniform compact model is extended to cover the full spectrum of geometry configurations within the process corners. Fig.13 illustrates the compact modelling results of devices with different fin heights, demonstrating the capability of the compact model for capturing process induced systematic geometry variation.

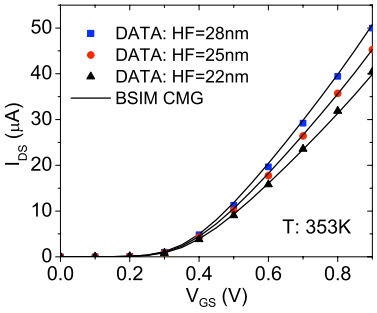

Fig.13 Id-Vg results of BSIM-CMG with different fin height, while the gate length is 20nm

Based on the analysis of underlying correlations between parameters and device characteristics, a statistical BSIM-CMG parameter set is identified for capturing the statistical variability. A device-operation-region orientated statistical

extraction strategy is developed and typical extraction results are exemplified in Fig.14. As one of the cores of PDK development, statistical compact model libraries are built based on the statistical compact modelling parameter extraction results, which then integrate naturally with Spice simulators.

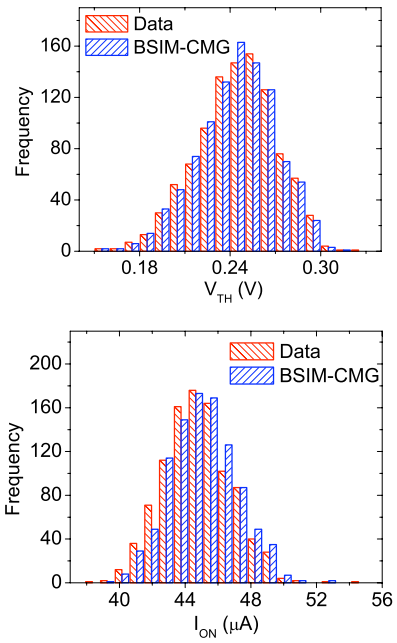

Fig.14 Typical statistical compact modelling results of V_{TH} and I_{ON}

IV. SRAM Simulation

The TCAD-based PDK enables the SRAM and device co-optimization practice at the early stage of new technology development. Fig.15 explores the impact of device gate length on FinFET SRAM performance for a cell ratio of 1 and 2. For this particular design, device gate length has a mild impact on SRAM noise margin. With gate length increased from 18nm to 24nm, around 11% and 8% improvement on SNM can be obtained for cell ratio of 1 and 2, respectively. However, it will introduce around 11-12% degradation on cell read-current performance. Meanwhile, a one-order-of-magnitude reduction in cell leakage current can be achieved. Based on actual applications, this information can provide guidelines on design trade-off decisions.

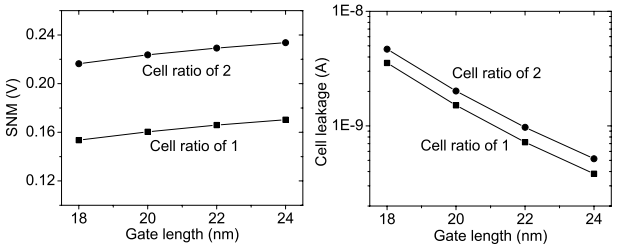

Fig.15 Impact of device gate length on SRAM performance

Among all the CMOS circuit components, the SRAM cell is the most sensitive to transistor statistical variability and it is essential to take into account the device variability in SRAM design. Fig. 16 illustrates the impact of combined statistical variability sources (including MGG) on FinFET SRAM-cell noise-margin performance with a cell ratio of 1 and nominal geometry configuration for base devices. In this design case, the WNM has much higher standard deviation and skew values (31mV, -0.97 respectively) compared to the SNM (11mV, -0.34). However, the mean value of WNM (340mV) is more than two times larger than SNM (151mV). Consequently, the limiting factor of SRAM operation in this design is on the read side. From a design decision aspect, it would be beneficial to introduce read-assist circuits in this technology.

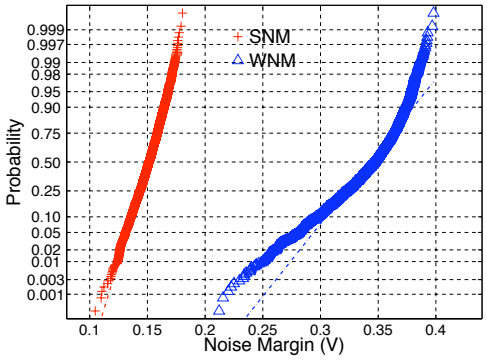

Fig.15 Impact of device statistical variability on SRAM noise margin performance

V. Conclusions

A TCAD-based PDK development strategy is presented to enable the early delivery of a PDK for emerging technologies. Its application for SRAM cell design for a 14nm technology node is demonstrated.

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