Comprehensive Study of Process-Induced Device Performance Variability and Optimization for 14 nm Technology Node Bulk FinFETs

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Abstract— **In this paper, we propose a device and process design strategy for L_g= 14 nm FinFETs considering the effects of process-induced geometry variability on device performance. A calibrated TCAD simulation and DC/RF compact model were used to design 14 nm CMOS bulk FinFET structures. The structures were tested under various process split conditions. The relationship between process-induced geometry variation and device performance was investigated, and key design factors to mitigate process variability are proposed.**

Keywords- 14 nm, CMOS, bulk, FinFET, variability

I. INTRODUCTION

Due to its excellent electrostatic properties, tri-gate bulk FinFETs can overcome the physical limitations of conventional planar devices and are attractive options for the sub-20 nm technology node [1, 2]. However when physical dimensions are aggressively scaled, variability becomes an issue. Recently, much research has addressed random dopant fluctuations (RDFs), line edge roughness (LER), and metal gate granularity (MGG) [1], but they remain difficult to control. In addition, variability from fluctuations in geometry becomes even more important in sub-20 nm FinFET structures [4]. In this study, we investigate the relationship between device performance and controllable geometry variations and propose a way to optimize geometric parameters in terms of DC and RF operation for the 14 nm technology node.

II. PROCESS FLOW AND SIMULATION STRUCTURE

Figure 1(a) briefly illustrates the process flow of n/pFinFETs. Figure 1(b)-(c) show a simulated n/pFinFET structure with $L_g/W_{fin}/H_{fin}$= 14/7/14 nm. The nominal fin geometry and transistor footprint were assumed to be linearly scaled from 22 nm FinFETs [2]. The gate dielectric consists of SiO_2=1 nm and HfO_2=2 nm. In both cases, a lightly doped channel (N_A, N_D <5E17cm^{-3}) was used to prevent RDFs. In the nFinFET, after undoped epi growth, As was implanted and the I/I peak exist on the top surface of fin. The undoped epi prevents the As from penetrating into the shallow trench isolation (STI) and diffusing out below the fin and decreases the I_{off} (see Figure 1(d)). In the pFinFET, doped SiGe epi was grown on the source/drain (S/D) region and dopants were driven into the fin. The SiGe makes compressive stress and enhances the hole mobility in the p-channel. The S/D structures (doping, epi, and silicide) for both n/pMOSFETs were separately optimized to meet the device targets in the International Technology Roadmap for Semiconductors (ITRS) [3]. A range of device geometric skew parameters were also derived from the ITRS [3].

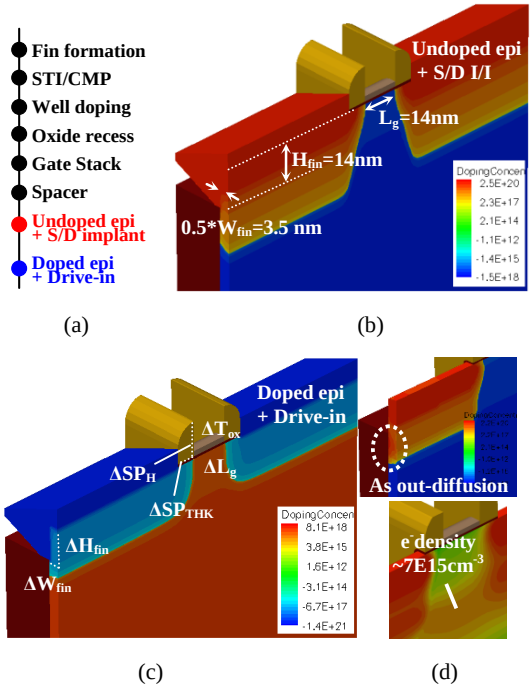

Figure 1 (a) process flow, (b) nFinFET with detailed geometry, (c) pFinFET with geometry variation. Lightly doped channel and retrograde well doping used in both, (d) As diffusion from below the fin w/o undoped epi and high I_{off}(> 1E-8 A) @V_g=0 V, V_d=1V.

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III. Results and Discussions

BSIM model parameters were extracted using nominal device data (see Figure 2). A compact model for parasitic capacitance and resistance in 3D tri-gates was developed to investigate how variations in geometry impact fringing capacitance and RF characteristics (f_T and f_{MAX}) and to determine the optimum layout for improved AC/RF. Fig. 3(a)-(b) show TCAD-simulated I_d-V_g, I_d-V_d data and well-fitted BSIM modeling data. These extracted parameters were used as a reference for all geometry variability.

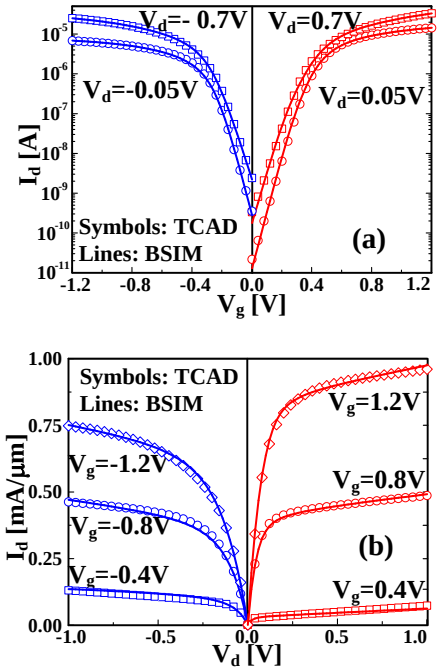

Figure 2 TCAD and modeled data for (a) I_d-V_g and (b) width (W_T=2H_{fin} +W_{fin}=35 nm) normalized I_d-V_d.

Table I ITRS 3σ requirement for MPU with a physical L_g= 14 nm

Variation	Process	nFinFET		pFinFET	
		-3σ	+3σ	-3σ	+3σ
ΔL_g	Litho	-1.5nm	1.5nm	-1.5nm	1.5nm
ΔW_{fin}	Litho	-1.4nm	1.4nm	-1.4nm	1.4nm
ΔH_{fin}	CMP, STI recess	-6%	6%	-6%	6%
ΔSP_{THK}	Depo. & etch of SiN	-0.7nm	0.7nm	-0.7nm	0.7nm
ΔSP_H		3.3~28.3 nm		-	-
ΔT_{ox}	ALD	< ±4%		-	-

Table I shows the relationship of geometry variability and process parameters and the ±3σ range for the 14 nm MPU technology node as suggested in the 2010 ITRS. Figure 3-4 exhibit variations in key device parameters (ΔSS, ΔDIBL, ΔI_{on}, and ΔI_{off}) as they correspond to geometric variations (W_{fin}, H_{fin}, L_g, and SP_{THK}) in 14 nm nFinFETs. Nominal values are shown in the boxes. The ±1x indicate the ITRS ±3σ range; 1.5x and 2x indicate variations 1.5 and 2 times that range. By simulating changes from ±1x (ITRS ±3σ) to ±2x (extreme case), we can identify/prioritize key design parameters for 14 nm device performance.

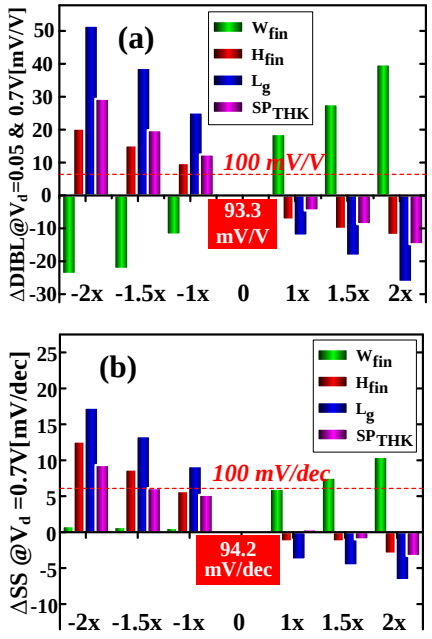

Figure 3(a) ΔDIBL and (b) ΔSS dependence of ±ΔW_{fin}, ±ΔH_{fin}, ±ΔL_g, ±ΔSP_{THK}. W_{fin} and H_{fin} are the most significant factors in nFinFET variations.

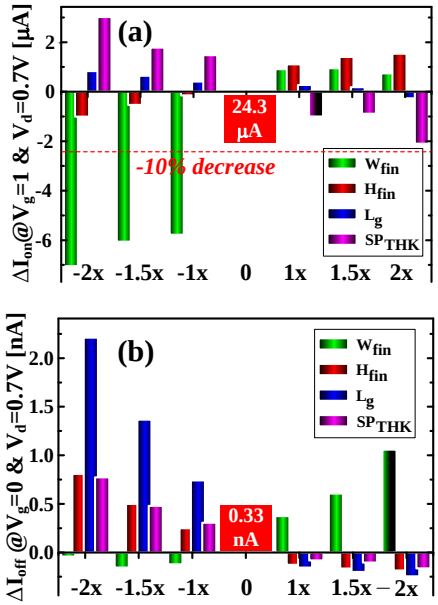

Figure 4 (a) ΔI_{on} and (b) ΔI_{off} dependence on ±ΔW_{fin}, ±ΔH_{fin}, ±ΔL_g, ±ΔSP_{THK}.

As shown in Figure 3(a)-(b), ΔDIBL and ΔSS are sensitive to ΔW_{fin} and ΔL_g; even while in the ±3σ range, they already exceed the upper limits. In Figure 4(a), ΔI_{on} decreases significantly when W_{fin} is narrower because fin resistance increases. The ΔI_{off} is mostly affected by ΔW_{fin} and ΔL_g. However, all the I_{off} values are acceptable for the targeted operation condition (Figure 5(b)). To improve the DIBL and SS margin, the nominal L_g should be extended above 14 nm. Even though a narrower W_{fin} can effectively improve the short channel margin, i.e., less DIBL and SS, it severely degrades I_{on}. Moreover W_{fin} is expected to be defined by double patterning, hence a thicker W_{fin} can reduce process complexity and variability. To compensate for the DIBL degradation due to a greater ΔW_{fin}, SP_{THK} and H_{fin} could be optimized to maintain device performance without increasing the footprint.

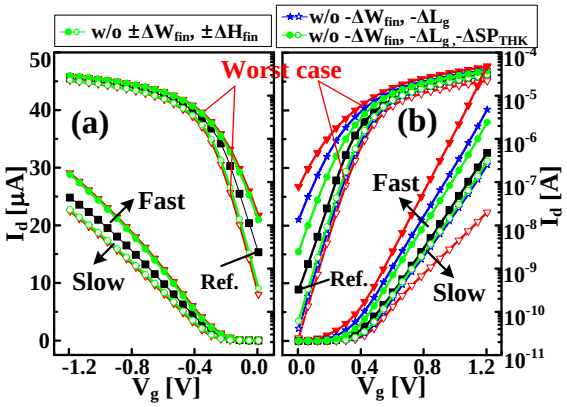

Figure 5 Fast and slow (a) pFinFET and (b) nFinFET for circuit simulation. Green represents acceptable I_d-V_g.

In pMOSFETs, device characteristics are almost same regardless of variations in W_{fin} and H_{fin} (Figure 5(a)). These variations can be significantly reduced by a doped epi and drive-in process for S/D formation. Therefore, an in situ doped epi structure might be neessary for the sub-20 nm technology node. Similarly, pFinFET variation can be reduced by a longer L_g. As shown in Figure 5(b), I_d-V_g can be adjusted for nFinFET circuit designs. Figure 6 shows the dependence of I_{off} on ΔSP_H. If the spacer height is less than 8 nm, I_{off} increases dramatically.

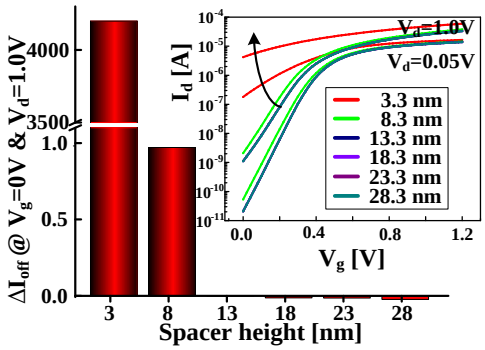

Figure 6 Below SP_H=8.3 nm, I_{off} degrades severely.

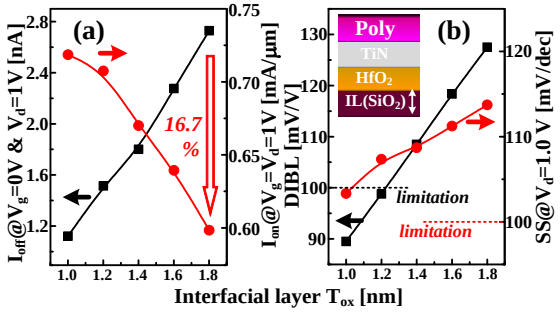

Figure 7 (a) I_{on} and I_{off}, (b) DIBL and SS as the function of the interfacial layer (IL).

In Figure 7(a), I_{off} remains acceptable as the interfacial layer (IL) increases but I_{on} dramatically decreases. DIBL and SS are already near their limits, hence scaling the equivalent oxide thickness (EOT) below 1 nm should be considered (Figure 7(b)).

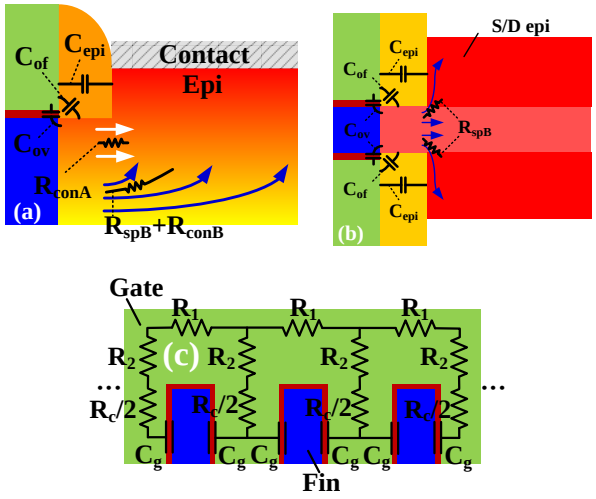

Figure 8(a) Simplified sideview and (b) topview of nFinFET for parasitic C_{para} and R_{sd} [5], (c) gate resistance R_g model [6].

Figure 8(a)-(c) show the parasitic $C_{para}=C_{ov}+C_{of}+C_{epi}$, series resistance $R_{sd}=R_{conA}\cdot(R_{spB}+R_{conB})/(R_{conA}+R_{spB}+R_{conB})$ [5], and gate resistance $R_g=0.25\cdot R_{eq,n}$, $R_{eq,n}=(R_2+0.5\cdot R_c)/(2(n+1)^2)+n^2\cdot(R_{eq,n-1}+R_1)/(n+1)^2$, $R_{eq,0}=R_2+0.5\cdot R_c$ [6].

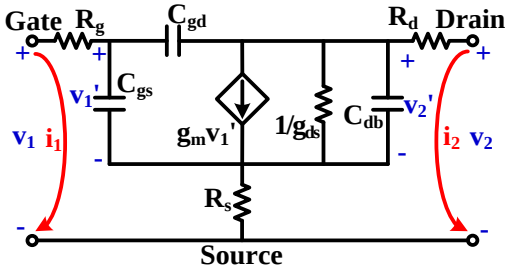

Figure 9 RF equivalent circuit including the parasitic C_{para}, R_{sd}, and R_g.

$$f_T = \frac{g_m}{2\pi\sqrt{C_{gs}^2 + 2C_{gs}C_{gd}}} \times \left\{1 - \frac{C_{gs}+C_{gd}}{C_{gs}^2+2C_{gs}C_{gd}} \times \begin{bmatrix} g_{ds}(C_{gs}R_s + C_{gs}R_d + C_{gd}R_d) \\ + g_m(C_{gd}R_d - C_{db}R_s) \end{bmatrix}\right\} \quad (1)$$

$$f_{MAX} = \frac{f_T}{2}\left\{\begin{matrix} g_{ds}R_g + 2\pi f_T C_{gd}R_g + \frac{C_{gd}+C_{db}}{C_{gs}+C_{gd}} 2\pi f_T C_{gd}R_g \\ - \frac{C_{db}}{C_{gs}+C_{gd}} 2\pi f_T C_{gs}R_s + \frac{C_{gd}^2 g_{ds}R_d + C_{gs}^2 g_{ds}R_s}{(C_{gs}+C_{gd})^2} \end{matrix}\right\}^{-1/2}$$

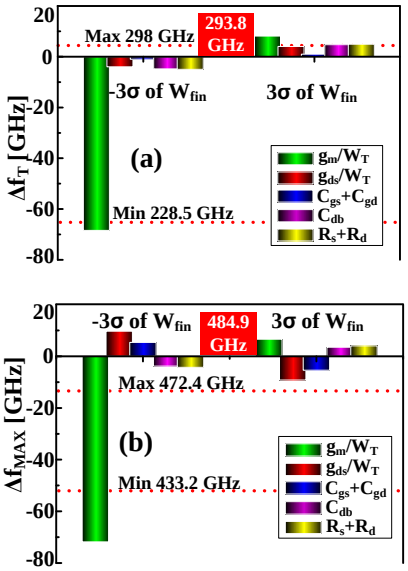

Figure 10(a) Δf_T and (b) Δf_{MAX} with individual parameter variation.

The RF equivalent circuit (Figure 9) and f_T and f_{MAX} (eq.(1)) are described using these parasitic components [4]. In nFinFETs, ΔW_{fin} is difficult to control, hence a f_T and f_{MAX} of $\pm 3\sigma$ W_{fin} were simulated at V_g=0.8 V and V_d=0.7 V, which has a high g_m. Among the reference parameters, only one parameter was changed to observe its effect on f_T and f_{MAX} (Figure 10). The $g_m(=\partial I_d/\partial V_g)$ predominantly affects f_T and f_{MAX}. The $g_{ds}(=\partial I_d/\partial V_d)$ and $C_{gs}+C_{gd}$ (proportional to C_{para}) are the main factors impacting f_{MAX} and compensate for the g_m effect. When ΔW_{fin} is -3σ, f_T and f_{MAX} degrade -22.2% and -10.7 %; however, when ΔW_{fin}=+3σ, they changed only 1.4% and -2.6%, respectively. Therefore, we should exercise caution in using FinFETs for analog/RF applications.

Table II Strategies for SOC considering variability of FinFET

	Single fin	**Multi fin (RF)**	**ROSC/SRAM**
Issue	variability	performance	delay/ΔV_T
Key Factor	ΔW_{fin}, ΔL_g	Δg_m, Δg_{ds}	C_{para}/ ΔW_{fin}, ΔL_g
Remark	- Extended L_g & W_{fin} (Fig. 3-4) - Doped epi S/D for reducing ΔW_{fin} & ΔH_{fin} (Fig. 5)	- I_{on} increase rather than variability (Fig.10) - multi-fin reduces the variability	- C_{para} of 3D interconnect >> C_{para} of device - Layout optimization

*Assuming that device performance meets the target.

IV. CONCLUSIONS

In this study, we investigated the impact of process-induced variability on device performance. The quantitatively extracted parameters allowed us to recommend a device design for improving the short channel margin in 14 nm bulk FinFETs. W_{fin} and L_g emerge as the two most important geometry parameters for controlling process-induced variability. A relaxed W_{fin} or a planar device might be feasible for analog/RF applications. We successfully identified a key factor for mitigating variability and proposed a strategy for reducing it (Table II).

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