Compact Model of Graphene Field Effect Transistors and Its Application in Circuit Simulation of RF Mixer Consisting of GFETs and CMOS

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Abstract—**An improved compact model of graphene field effect transistors (GFETs) is presented in this paper with the ability of capturing effect of back gate (BG) bias on adjusting both top gate (TG) Dirac point voltage (V_{Dirac}) and the contact resistance in source and drain (S/D) regime. This presented model is also implemented within Verilog-A for circuit simulation; calculation results of transfer characteristics of GFET obtained from Verilog-A model are compared with those obtained from the Matlab model for validation. A double-balanced RF mixer circuit with four GFETs is conducted and good mixer performance compared to single-GFET mixer and 0.18μm CMOS double-balanced mixer is achieved by exploring the large linear region in the output characteristics of GFETs.**

Keywords- ***GFET compact model, Verilog-A model, contact resistance, GFET mixer simulation***

I. INTRODUCTION

Graphene field effect transistors (GFETs) show great potential in analog and RF applications due to its ambipolar carrier transport characteristics. RF mixer and frequency multiplier based on single GFET have been reported in recent experimental studies [1], [2]. Compact model of GFETs has been developed based on our previous work [3] with improvement in capturing the effects of back-gate (BG) biasing on shifting the Dirac voltage (to be defined in the text) for carriers in graphene channel, and on reducing the source/drain (S/D) series resistances. The model presented is also implemented within Verilog-A, thus make it compatible for us to carry out circuit simulations in general Spice-type circuit simulators. In order to take advantage of large linear operation region in GFET's output characteristics, a double-balanced, passive mixer is realized using hybrid GFET/CMOS circuit configuration: four GFETs for multiplier and about a dozen of CMOS transistors for Op-Amp. The transistor-level circuit simulation shows GFETs with channel length as long as 5-μm can achieve equivalent performance as 0.18-μm CMOS technology. And the architecture of passive mixer implemented using GFETs achieves the superior performance as compared to that of its counterpart using single GFET [2].

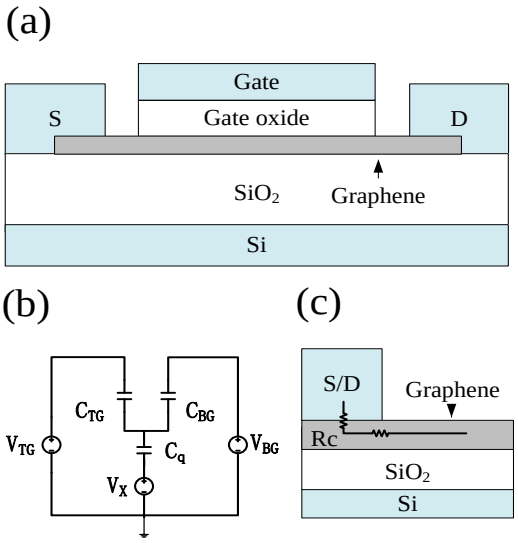

Figure. 1(a) Cross-section of dual gate GFET configuration. (b) Equivalent capacitance network of dual gate GFET. (c) Illustration of metal/graphene contact resistance in S/D regime.

II. COMPACT MODEL

A. Compact Model

Schematic diagram of dual-gate GFET is shown in Fig. 1(a). Considering graphene channel quantum capacitance, the equivalent capacitance network of dual gate GFET is presented in the Fig. 1(b). Drain current in GFET is calculated under the assumption of drift-diffusive carrier transport [4] in graphene channel using:

$$I_{DS} = \frac{q\mu W \int_{V_{CS}}^{V_{CD}} \rho_C(V_C) dV_C}{L - \mu \int_{V_{CS}}^{V_{CD}} \frac{1}{v_{sat}} dV_C}, \quad (1)$$

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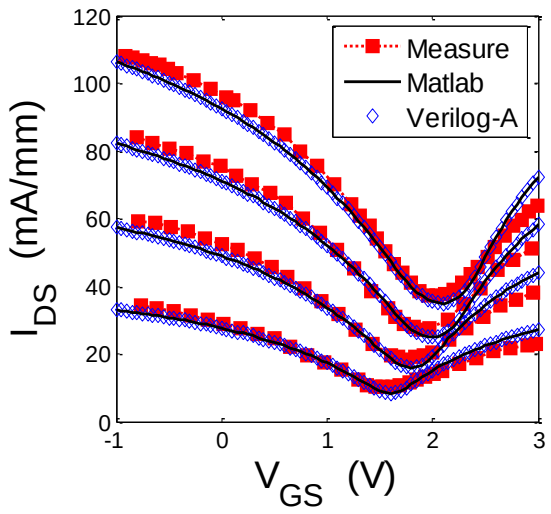

Figure. 2 Comparison between measurements and model calculations of transfer characteristic for GFET from Ref. [5]. Results from both Matlab and Verilog-A models are shown.

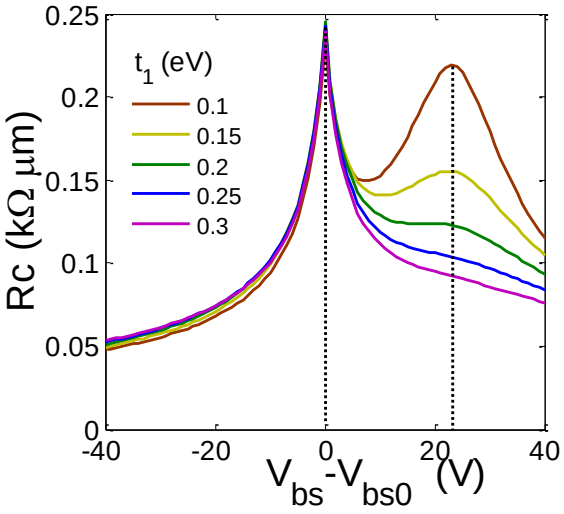

Figure. 3 Dependence of contact resistance (R_c) on effective BG bias (V_{bs}-V_{bs0}). T_{MTG}=T_{GTG}=1, t_2=117meV, η=5meV, t_1 varies from 100meV to 300meV. Peak values occur for BG voltage at the Dirac point of both channel and metal-covered graphene.

where q is the electron charge, μ is the low field mobility, and W and L are gate width and gate length respectively. ρ_C is the carrier sheet density expressed as $\rho_C=C_q|V_C|/2q+\rho_0$, where ρ_0 is residual carrier sheet density. Saturation velocity determined by optical phonon angle-frequency Ω in substrate and gate dielectric is given by $v_{sat}=\Omega/\sqrt{(\rho_C\pi)}$. Integrated variable V_C is the voltage drop across the quantum capacitance along the graphene channel with $V_C(x=0)=V_{CS}$ and $V_C(x=L)=V_{CD}$, which is determined by the capacity network shown in Fig. 1(b). According to the charge conservation law, the following relation is obtained:

$$V_C(x)=[V_{TG}-V_{TG0}-V(x)]\frac{C_t}{C_t+C_b+C_q/2}$$

$$+[V_{BG}-V_{BG0}-V(x)]\frac{C_b}{C_t+C_b+C_q/2}, \qquad (2)$$

where C_b and C_t are BG and TG capacitance respectively, quantum capacitance is $C_q=2q^3/\pi(\hbar v_F)^2$ with Fermi velocity of graphene $v_F=1\times10^8$ cm/s. V_{TG0} and V_{BG0} are Dirac voltage for TG and BG bias in dual gate respectively, and $V(x)$ is the electrostatic channel potential under zero gate bias with $V(x=0)=0$ and $V(x=L)=V_{DS}$.

This presented compact model is validated by fitting the current transfer characteristics of GFET from Ref. [5]. The device investigated is a TG GFET on SiO_2 substrate utilizing 15 nm Al_2O_3 gate dielectric (ε_r~7.04). L= 5 μm, W=10 μm. V_{TG0} is estimated to be 1.55 V. Symmetric carrier mobility μ=1500 $cm^2/V\cdot s$ is assumed for both electrons and holes. Contact resistance is considered in this compact model for the voltage drop on this series resistance will lead to reduction of effective drain-source bias: $V_{DS,eff}=V_{DS,ext}-I_{DS}\times R_c$, where $R_c=R_S+R_D$. Symmetric contact resistance of R_S=R_D=1.2 kΩ is used in calculations. Finally, residual carrier density of $\rho_0=5\times10^{11}$ cm^{-2} is applied to achieve better agreement near the Dirac point.

The comparisons between experimental results and compact model calculations are shown in Fig. 2 with good agreements obtained.

B. Realisitc Model

In realistic GFET, contact resistance and carrier mobility vary with respect to gate bias voltage, which results in nonlinearity in current transfer curves. In order to set up a more realistic compact model, we investigated the dependence of series contact resistance in S/D regime on BG bias voltage. The S/D regime metal/graphene contact resistance, as is shown in Fig. 1(c), is induced in the carrier transport process when carrier injected from the electrode transport to the metal-covered graphene and then to the graphene channel [6] and it will reduce the effective source/drain bias applied to the

channel as is discussed in section A, and impede the drain current. The value of metal graphene contact resistance can be calculated using extended Landauer's formula given as follows [6]

$$Gc = \frac{4e^2}{h}\int_{-Ec}^{Ec} dE_1 Voigt(E_1 - \Delta E_{FM}, t_1, \eta)\int_{-\infty}^{\infty} dE_2 G(E_2 - \Delta E_{FG}, t_2)$$

$$\frac{1}{W}\sum_{n=0}^{\min\{M_1,M_2\}} T(k_y = n\pi/W, E_1, E_2) \quad , \qquad (3)$$

Where Voigt function (convolution of Gaussian and Lorentzian function) and Gaussian function are used to describe the Density of States (DoS) broadening in metal-covered graphene and channel graphene separately; E_c is the cutoff energy of DoS broadening of metal covered graphene, t_1 and t_2 are the broadening factors, η is the coupling coefficient with empirical value of 5 meV, conduction model $M_{1,2}= W|E_{1,2}|/(\pi\hbar v_F)$, and k_y is perpendicular wave vector. The work function of source/drain metal electrode is also included in calculation of energy difference between Fermi level and Dirac point (ΔE_{FM}) in metal-covered graphene therefore the effect of metal materials in adjusting the contact resistance can be investigated as well. Since error occurs inevitably in experimental works, we now can merely use this Landauer approach to demonstrate the dependence of R_c on BG bias and make reasonable anticipation on device performance (Fig. 3). Contact resistance as well as series resistance remains an open issue for further research.

C. Verilog-A Model

In this paper, we also present a Verilog-A model for GFET which makes it possible to carry out circuit simulation of GFET based applications. We investigated experimental work by Han Wang et al. [5] , and fit the I-V curves with our compact model. The comparison results shown in Fig. 2 validate our compact model. The same curves of drain current acquired in HSPICE simulations are also shown in Fig. 2.

III. RF MIXER

A. GFET Mixer

Recently report of the single GFET mixers has been proved to be potential [1], [2]. However, the input frequencies in these reports, f_{LO} and f_{RF}, would penetrate through the single GFET mixers to the output. Also, the output power of unwanted higher-order frequency components in output signal, especially those in the vicinity of the frequencies of interest, are relatively high in single GFET mixers, due to the asymmetry in the ambipolar transport characteristics of GFET. Furthermore, single GFET mixers require large input RF signal (~1 $V_{p\text{-}p}$) to obtain good mixing quality, since the transconductance near the Dirac point is relatively low.

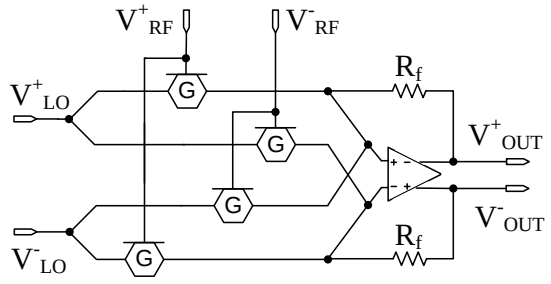

Figure. 4 Schematic of four-GFET double-balanced mixer.

B. 4-GFET Double Balanced Mixer

Applying the proposed GFET Verilog-A model, we designed and simulated a four-GFET double-balanced RF mixer circuit, as is shown in Fig. 4. The structure was originally used in CMOS technology and the frequency mixing is based on the voltage-controlled linear-resistance characteristics of MOS transistors in linear region [8]. Differential RF and LO signals are applied to gate and drain end of GFETs respectively. The output current flowing through the feedback resistors is the result of the multiplication of the RF signal applied to the gates of GFETs and LO signal applied to the drains. The feedback resistors and the operational amplifier then convert the current output into voltage output and enable the mixer to drive the next stage. The mixer cell consists of four GFETs and exhibits high linearity due to double balanced passive structure. The operational amplifier can be replaced by two identical common source voltage amplifiers with finite gain, such as NMOS common source voltage amplifier or single GFET common source voltage amplifier, and remain the same linearity.

The symmetric architecture of the four-GFET highly suppresses the common mode, the penetration of the input RF and LO frequencies, and the unwanted higher-order frequency components in the vicinity of the difference ($f_{IF}=f_{RF}-f_{LO}$) and sum frequency ($f_{RF}+f_{LO}$) of RF and LO. Linear output and transfer characteristics of GFET are highly in favored while using this structure, thus all the four GFETs are biased at the linear region on one side of Dirac point to act as unipolar FET.

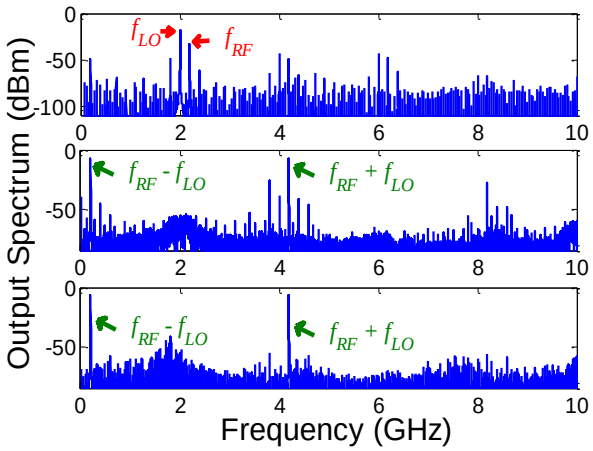

Figure. 5 Output spectrum of (a) single GFET mixer from Ref. [2], (b) four-GFET double-balanced mixer and (c) using BG instead of TG dc bias. Input RF and LO signals are 2.2 GHz 200mVp-p and 2.0 GHz 1Vp-p, respectively. Best results are obtained in case (c) for "cleanest" $f_{IF}=f_{RF}-f_{LO}$.

C. Back-gate Bias

Since BG bias can effectively shift the TG Dirac point, we also proposed an alternative biasing method for the mixer, which is to apply the dc bias on the back gate and connect only the RF signal directly to the top gate. The slope of linear shift of TG Dirac point V_{TG0} observed experimentally reflects the ratio between TG and BG capacitance [7]. V_{TG0}'= V_{TG0}-V_{BG}·C_b/C_t. In this way, the disturbance between the RF signal and the bias voltage is removed, and those unwanted higher-order frequency components are further suppressed as is shown in Fig. 5 (C).

D. Results and Analysis

Simulation results of 4-GFET double balanced mixer are shown in Fig. 5. This proposed four-GFET mixer structure highly suppressed the RF/LO signals frequencies and high order frequencies, compared to the single GFET mixer structure [2], which exhibits good performance only under large input signal. As expected, given the bias of V_{DS}=1.5V, V_{GS}=3.5V and V_{BS}=0V, this 4-GFET mixer shows good linearity and signal purity. Penetration of both f_{LO} and f_{RF} as well as the harmful high-order frequencies in the vicinity of the difference (f_{IF}) and sum frequency are saliently suppressed. If we use back-gate bias, giving the bias of V_{DS}=1.5V, V_{GS}=0V and V_{BS}=63.6V, the output power of frequencies in the vicinity of the difference and sum frequency are even weaker. Since the device we use is from Ref. [2] and the substrate oxide is as thick as 300nm, large V_{BS} is required. If the thickness of the substrate oxide is 90nm, the mixer only need V_{BS}=19.1V to obtain similar performance. By comparing the result with 180nm CMOS technology with input RF signal of 200mVp-p, we found long channel length (~5μm) GFET mixer can almost reach the same performance as short channel Si-MOS provide. We also acquired similar mixing performance using different input RF voltages from 1-2mVpp to 2Vpp. The wide range of the input signal voltage is achieved compared to single GFET mixers.

IV. Conclusion

In this paper we set up a compact model of dual-gate GFET which include the effect of BG bias on adjusting the TG V_{Dirac} and reducing S/D regime contact resistance, and a corresponding Verilog-A model to convey device level simulations is implemented. Device taken from recently reported experimental work is investigated, and good agreement has been achieved comparing simulation results and experimental data. A 4-GFET double-balanced RF mixer circuit simulation is designed and simulated and comparable performance compared to CMOS mixer is obtained by making use of the high linear output and transfer characteristics of GFET, and multiple GFETs symmetric structure are introduced to cancel out the input signal penetration and unwanted frequency components in single GFET structure.

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Reference

[1] Y.-M. Lin, A.Valdes-Garcia, S.-J. Han, D.B. Farmer, I. Meric, Y. Sun, Y. Wu,C. Dimitrakopoulos, A. Grill, P. Avouris, K. A. Jenkins., Science **332**, 1294 (2011).

[2] H. Wang, A. Hsu, J. Wu, K. Jing, T. Palacios, IEEE Electron Device Lett. **31**, 906 (2010).

[3] W. Zhu,J. Zhang, Z. Yu, Appl. Phys. Lett. **100**, 112104 (2012).

[4] D. Jiménez and O. Moldovan, IEEE Trans. Electon Devices **58**, 4049 (2011).

[5] H. Wang, A. Hsu, K. K. Kim, J. Kong, and T. Palacios, IEEE Microwave Symposium Digest (MTT) (2011).

[6] F. Xia, Vasili Perebeinos, Yu-ming Lin, Yanqing Wu and Phaedon Avouris, Nature Nanotech. **6**,179 (2011).

[7] D. B. Farmer H.-Y. Chiu, Y.-M. Lin, K. A. Jenkins, F. Xia and P. Avouris, Nano Lett. **9**, 4474 (2009).

[8] J. Crols and M. S. J. Steyaert, J. Solid State Circuits **30**, 736 (1995).