A Compact Model for Graphene FETs for Linear and Non-linear Circuits

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Abstract—**The graphene field-effect transistor has generated attention in recent years for its potential for fast electronics, with theoretical transit frequencies in the THz range, and fabricated devices operating at hundreds of GHz. Previously published models are based on numerical iteration or neglect the equilibrium quantum capacitance, leading to reduced accuracy around the Dirac point. We have derived a compact, physics-based closed-form equation for drain-source current that can be implemented in a circuit level simulator. This model demonstrates strong agreement with both DC and RF measurements, as well as linear and non-linear circuits. The model also enables simulation of circuits to enable design of topologies that take advantage of the unique properties of the graphene transistor. The model also affords parameter variation analyses to quantify the adverse effects of non-idealities such as contact resistance. Finally, we have developed a quantum capacitance limited model to benchmark the performance of realistic devices against the ideal quantum capacitance limit, and elucidate the effects of oxide scaling.**

Keywords - graphene; transistor; circuit model; RF performance

I. INTRODUCTION

Graphene field-effect transistors (GFETs) have generated significant interest during the last decade for their potential in analog and high-frequency circuits, and are an attractive candidate for post-silicon electronics[1]. The advantages of the GFET over conventional CMOS technologies include high saturation velocity[2], high current handling capabilities[3], and ultra-high mobility at room temperature[4]. For high-frequency performance, the GFET is a natural rectifier, enabling high frequency sources on chip. Additionally, performance at hundreds of GHz has been previously reported [5]. Finally, several graphene circuits have been demonstrated, including amplifiers[6, 7], mixers[8-10], and frequency multipliers[11-13].

The need to design graphene circuits on a larger scale necessitates the need for a compact model that encapsulates device characteristics including non-idealities, and small and large signal behavior. To be widely accepted, the model must be implemented in a circuit simulator that is widely used in the semiconductor industry, which can facilitate fast simulations with parameters and component configuration easily modified. There have been several circuit models published that encompass the device physics of the GFET, however, those models are generally not compact[14, 15]. The compact models tend to neglect the equilibrium quantum capacitance[16-18], leading to inaccuracies around the Dirac point, an operating point crucial to the performance of mixers and frequency multipliers.

In this work, we present a compact, physics-based closed-form equation for drain-source current, based on intrinsic parameters of the GFET device including quantum capacitance, oxide capacitance, mobility and velocity saturation. This model is then implemented in Agilent Advanced Design System (ADS), a SPICE-like circuit level simulator [19], enabling a multitude of simulation options from within a single environment. ADS is chosen for convenience and integration with measurement equipment, but other simulators such as Cadence can be used. The model has been validated against experimental graphene transistors from several research groups, showing good agreement. Additionally, we have developed an exactly solvable model based on the ideal quantum capacitance limited case, which enables us to predict upper bounds on GFET performance.

The model implementation in ADS enables simulations for new circuits that take advantage of the unique properties of the GFET, giving designers a straightforward way to try new circuit topologies. Parameter variation analyses are also easily achieved in ADS, enabling the designer to quickly quantify the adverse effects of non-idealities and parasitics, such as contact resistance, parasitic capacitance, and impurities.

We present demonstrations of the model, including fitting plots for both DC and RF performance. We also present parameter variation analyses to explore the effects of contact resistance, highlighting the consequences on negative differential resistance behavior. Finally, we benchmark the performance of realistic devices against the quantum capacitance limited model to examine the effects of oxide scaling.

II. DERIVATION OF MODEL

We first derive the properties of the intrinsic device from fundamental physics, including velocity saturation, charged impurities, and quantum capacitance (C_q) effects. A

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cross section of the modeled device is shown in Fig. 1(a), with the sum of all resistances due to contacts and access resistance indicated as R_c. Fig. 1(b) demonstrates the dependence of the surface potential φ_s on the oxide and quantum capacitances (C_{ox} and C_q, respectively), and Fig. 1(c) shows the compact model of the FET, with extrinsic resistances indicated as shown. The drain-source current I_D is calculated from the drift velocity (v_{drift}) and carrier density (n) as[17]

$$I_{DS} = q\frac{W}{L}\int_0^L n(x)v_{drift}(x)dx \tag{1}$$

where q is the charge of an electron, W is the width, and the position in the channel x is bounded by 0 and the length L. In this formulation, we examine only the intrinsic device without contact resistance, indicated in Fig. 1(c). All extrinsic effects added in the ADS model as appropriate; the biases used in the following equations are all intrinsic.

The drift velocity is represented as[20]

$$v_{drift} = \frac{\mu E}{\sqrt{\left(1+\left(\frac{\mu V_{DS}}{L v_{sat}}\right)^2\right)}} \tag{2}$$

where E is the transverse electric field and μ is the low-field mobility. The carrier density is a dilogarithmic function of surface potential[21]. However, by assuming symmetric hole and electron mobilities, the expression for carrier density simplifies to

$$n = n_o + \frac{(q\varphi_s(x))^2}{\pi\hbar^2 v_f^2} \tag{3}$$

Where n_o is the sum of the impurity concentration and intrinsic concentration (~1.6 x 10^{11} cm^{-2}), $\hbar$ is the reduced Planck's constant, and v_f is the Fermi velocity (~10^8cm/s). The surface potential can be calculated as indicated by Fig. 1(b) as

$$\varphi_s = \frac{C_{ox}}{C_{ox}+C_q(\varphi_s)}(V_{GS}-V_{CH}) \tag{4}$$

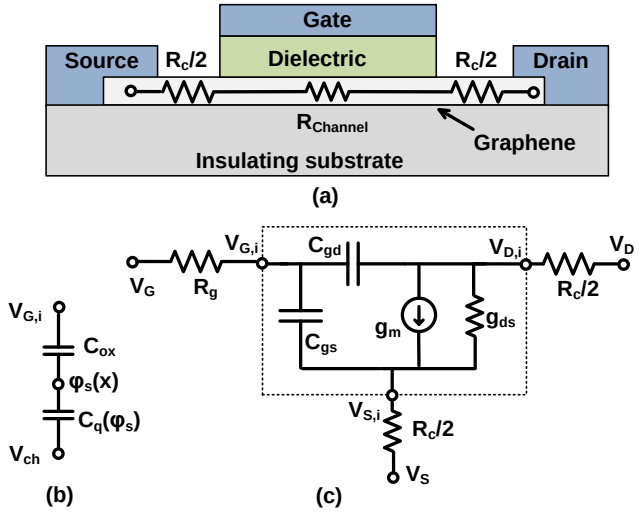

Figure 1. (a) Cross section of the modeled GFET. (b) Two-terminal capacitive divider model of the graphene channel, considering both the oxide and quantum capacitances. (c) Compact model of GFET; the intrinsic model is enclosed within the dashed lines.

Due to the logarithmic nature of the quantum capacitance dependence on surface potential[22], (4) is transcendental and does not have a closed form solution for φ_s in terms of the applied voltage.

A. *Finite oxide capacitance case*

Several published models neglect the quantum capacitance in the model formulation[16-18]. Additionally, numerous models approximate the quantum capacitance as a linear function of the surface potential[14, 15], which distorts the behavior near the Dirac voltage, an operating point crucial for frequency multipliers. Here, we use an analytical electron-hole symmetric expression that enables accurate approximation of C_q at both high gate bias, where the linear model excels, and low gate bias, which is absent in previous models. We approximate the quantum capacitance as proportional to the quadratic mean of the intrinsic quantum capacitance, C_{qo} = 8.426 fF/μm^2, and the linear function of quantum capacitance:

$$C_q \approx C_{qo}\sqrt{1+\left(\frac{q\varphi_s}{k_B T \ln 4}\right)^2} \tag{5}$$

Where k_B is Boltzmann's constant, and T is the temperature in Kelvin. This expression can then be used to derive a quartic relationship between the bias voltage and surface potential. Using a Maclaurin series expansion to retain accuracy around the Dirac point, the quartic equation is transformed to a pseudo-quadratic equation, and a closed form solution is found for the surface potential as a function of the gate voltage. The surface potential is then applied to the equation for carrier density to obtain the drain current equation:

$$I_{DS} = q\frac{W}{L}\mu_{eff}\Bigg(n_o V_{DS} + \Bigg(\frac{(\alpha+1)^2(k_B T\ln 4)^2}{4\pi\hbar^2 v_f^2(\alpha\ln 2+1)}\Bigg(-2V_{DS}+V_{DG}\sqrt{1+\delta^2 V_{DG}{}^2} + V_{GS}\sqrt{1+\delta^2 V_{GS}{}^2}+\frac{\operatorname{asinh}\delta V_{DG}+\operatorname{asinh}\delta V_{GS}}{\delta}\Bigg)\Bigg)\Bigg) \tag{6}$$

where $\alpha = C_{ox}/C_{qo}$, and

$$\delta = \frac{2\alpha\sqrt{(\alpha\ln 2+1)}}{(\alpha+1)^2}\frac{q}{k_B T\ln 4} \tag{7}$$

$$\mu_{eff} = \frac{\mu}{\sqrt{1+\left(\frac{\mu V_{DS}}{v_{sat}L}\right)^2}} \tag{8}$$

B. *Quantum Capacitance limited case*

The quantum capacitance limited case can be used to benchmark performance limits. As the oxide capacitance becomes much greater than the quantum capacitance for the bias points of interest, (4) simplifies to $\varphi_s = V_{GS} - V_{CH}$. This assumption simplifies (6) to

$$I_{DS} = q\frac{W}{L}\mu_{eff}V_{DS}\left(n_o + \frac{q^2}{\pi\hbar^2 v_f^2}\left(V_{GS}^2 + \frac{V_{DS}^2}{3} - V_{DS}V_{GS}\right)\right) \tag{9}$$

This equation reveals the intrinsically cubic dependence of the current on drain-source voltage. Additionally, quantities such

as the transconductance g_m and drain-source conductance g_{ds} can be derived from (9) to provide further insights on the intrinsic behavior of the graphene FET.

C. Implementation in ADS

Equation (6) is implemented in ADS as a voltage controlled current source, with transistor parameters and bias voltages as equation inputs. Gate-drain and gate-source capacitances are added to complete the intrinsic model. We estimate the total gate capacitance to be equal to C_{ox}, split equally between gate-drain and gate-source capacitances. Parasitics such as drain and source resistances, pad capacitances, and others are added extrinsically in the circuit schematic. A gate voltage, drain voltage, and ground potential are applied as appropriate.

III. Results

A. Model Validation

The model is compared with both long channel and short channel devices, and DC and doubler performance. Fig. 2 demonstrates the accuracy of the DC current calculation, with calculations performed for both short channel and long channel devices (Fig. 2(a) and Fig. 2(b), respectively).

Fig. 3 shows the measurement and simulation results for a GFET on a quartz substrate, shown in Fig. 3(a). The DC data simulation and measurement results are shown in Fig. 3(b) to demonstrate accurate fit around the Dirac point. Due to asymmetrical hole and electron mobilities, the fit is locally accurate, but parameters can be adjusted to find the best fit for hole and electron branches individually. Scattering parameters were simulated, and small signal current gain H_{21} was calculated for both simulated and measured data to extract the transit frequency as shown in Fig. 3(c). Finally, a harmonic balance simulation was performed to evaluate the device as a candidate for frequency doubling. Again we observe good agreement between measured data and the model, shown in

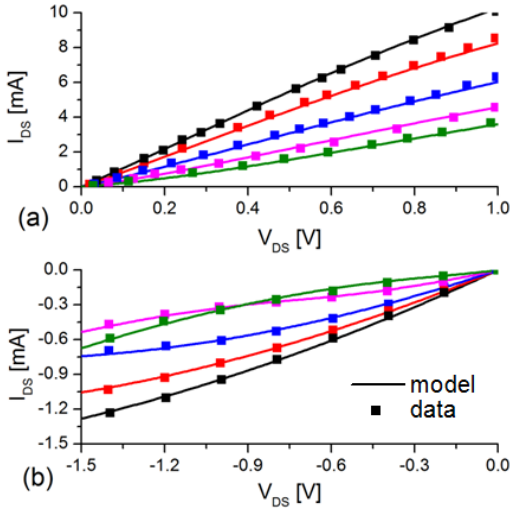

Figure 2. DC model validation with strong agreement between simulation (solid lines) and measured data (symbols) at several gate biases, for GFETs with length (a) 100 nm [23] and (b) 10 µm[24].

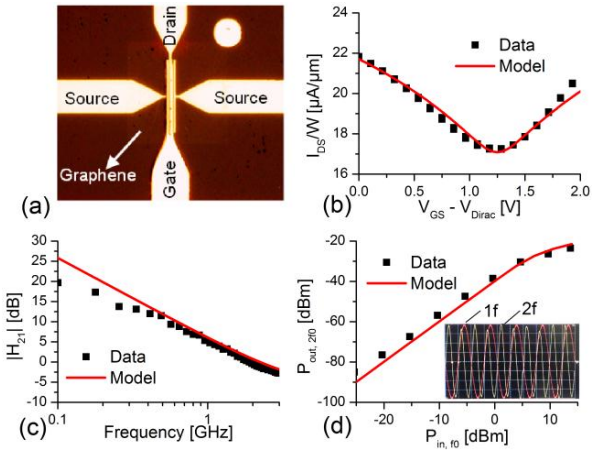

Figure 3. (a) Optical image of quartz GFET. (b) DC experimental and model data of pictured GFET (L = 500 nm). (c) Experimental and simulated small-signal current gain showing strong agreement with the extracted transit frequency f_t = 2 GHz. (d) Output power as a function of input power. The inset is a screenshot of the oscilloscope showing frequency doubling behavior.

Fig. 3(d), in regards to both quantitative output and compression behaviors.

B. Parameter variation

The use of a compact model within a circuit simulator allows for parameter variation analyses for any model parameter. First, we demonstrate the adverse effects of contact resistance on device transconductance in Fig. 4(a), showing the rapid decay in performance as contact resistance increases beyond 100 Ω·µm. We also quantify the required contact resistance, normalized to width, necessary to achieve 80% of the optimal transconductance, which is achieved in the ideal case of no contact resistance [Fig. 4(b)]. We also examine the obscuring effects of contact resistance on the newly observed negative differential resistance phenomenon[25], with drain current in Fig. 4(c) and drain-source conductance in Fig. 4(d).

Similarly, we present the effects of oxide capacitance scaling on transconductance and current by comparing to the optimal quantum-capacitance limited case, in the absence of contact resistance (Fig. 5). The plots show the bias conditions that enable the device to approach quantum-capacitance limited behavior. At the Dirac voltage (indicated by the dashed lines), the quantum capacitance is minimized, and quantum-capacitance limited behavior can be achieved even for oxide capacitance values only an order of magnitude larger than C_{qo}. However, as the gate bias is increased, the quantum capacitance is increased and the effects of the oxide capacitance become more significant in the device, deviating behavior from the quantum-capacitance limited behavior.

Figure 5 also illustrates the oxide capacitance required to approach quantum capacitance limited performance. For the low field case [Fig. 5(a) and Fig. 5(b)] an oxide capacitance value of 30 times the intrinsic quantum capacitance can yield current over half of the quantum-capacitance limited current. For the high field case [Fig. 5(c) and Fig. 5(d)], an oxide capacitance of over 100 times the intrinsic quantum capacitance is needed.

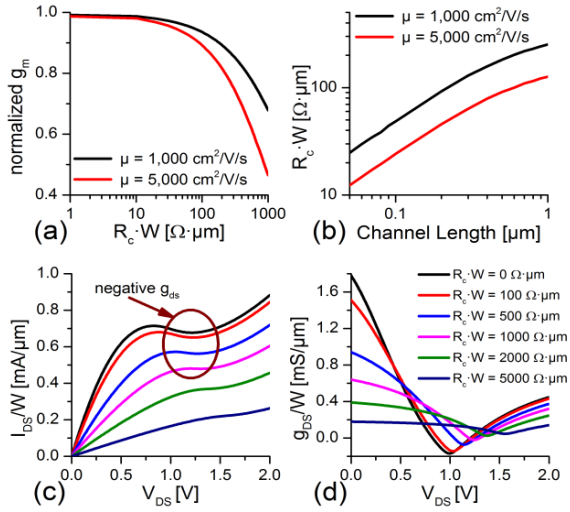

Figure 4. Effects of contact resistance (C_{ox} = intrinsic quantum capacitance C_{qo}, 8.426 fF/μm^2). (a) Transconductance as a function of contact resistance, normalized to R_c for constant transverse field E_{DS} = 1V/μm, V_{DS} = 0.5 V. (b) Maximum tolerable contact resistance needed to achieve 80% or better transconductance, compared to the ideal R_c = 0 case, with E_{DS} = 1V/μm. (c) Contact resistance obscures the intrinsic device physics including negative drain-source conductance g_{ds}. (d) g_{ds} for the device simulated in part (c).

IV. Conclusion

In this work we describe a compact equation for the drain current of a graphene device, accurate at both the Dirac point and for large gate voltages. The model demonstrates good agreement with DC characterization, doubler behavior, and transit frequency measurements. Parameter variation is performed with the model to demonstrate limiting behaviors and the effects of parasitics and non-idealities on device performance. Future work includes improved models of intrinsic capacitances, as well as the implementation of asymmetric electron and hole mobilities.

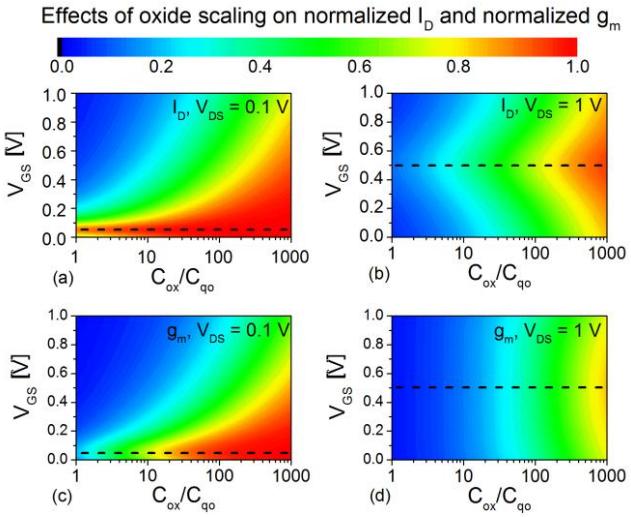

Figure 5. Normalized current (a, b) and transconductance (c, d) revealing the impact of oxide scaling. The values are normalized to current and transconductance in the quantum capacitance limit (L = 1 μm).The dashed line indicates the Dirac voltage, V_{GS} = V_{DS}/2.

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