Characterization of Time Dependent Carrier Trapping in Poly-Crystalline TFTs and Its Accurate Modeling for Circuit Simulation

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Abstract—We have investigated the influence of carrier traps on device characteristics in TFTs. In particular, our focus was given on transient characteristics influenced by the carrier trap, which occur during the device operation. A compact model for circuit simulation of TFTs has been developed by considering the time constant of the carrier traps. The model was verified with measured TFT characteristics.

Keywords- TFT; compact model; trap density; transient characteristics

I. INTRODUCTION (HEADING 1)

Thin-film transistors (TFT) have been applied for large area displays as well as for solar panels. As the substrate not only silicon related materials such as the poly-crystalline silicon but also organic materials are widely investigated. Our focus is given on the poly-crystalline silicon TFTs, for which it has been demonstrated that the laser annealed technique makes the device applicable even in the high-frequency operating range [1]. Our purpose is to achieve accurate prediction of TFT circuit performances under such fast switching operations. It is known that trap sites located at the grain boundaries of the poly-silicon are still partly remained even after the annealing and strongly influence on device performances. Therefore, we have experimentally characterized the transient behavior of the poly-silicon TFTs on focus of the traps. The trap/detrap time constant is shown here to be long in comparison to the achievable switching speeds. We develop a compact model considering this time constant for circuit simulation. It is shown that this rather long time constant for trapping events result in a history effect, similar to the one resulting for mobile-charge accumulation in SOI-MOSFETs. Measured transient TFT characteristics are well reproduced with this new dynamic charge-trapping model, and a resulting history effect is observed as expected.

II. TRAP PROPERTIES IN TFTS

Measured I_d-V_g characteristics are shown in Fig.1 for two different devices A and B on the same wafer at V_d =0.1V. The reason for the small V_d is to exclude the hot electron effect in our investigation. Even though the device size is the same, a big variation in the current characteristics is observed. Measured switching performances of the same devices (Device A and Device B) are shown in Fig. 2, which verifies a drastic current decay after the applied bias saturates. The decay is stronger for Device B, for which the I_d-V_g characteristic is strongly degraded.

It is known that a specific feature of TFTs is the high density of trap states induced at the boundaries of crystallized domains. The current decay observed in Fig. 2 is attributed to the carrier trap increase in accordance with the long duration of the carrier injection into the substrate. Therefore the different I_d-V_g characteristics of Device A and B are attributed to the different trap densities. Fig. 3 shows that the same waveform is observed for pulse repetition without degradation of the current.

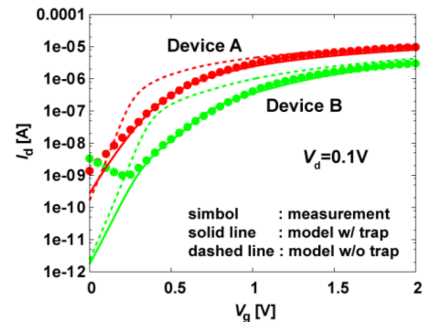

Fig. 1. Comparison of model calculation results with measurements at V_d for two different devices (Device A and Device B) as a function of V_g. Calculation results without trap densities are also depicted by dashed lines.

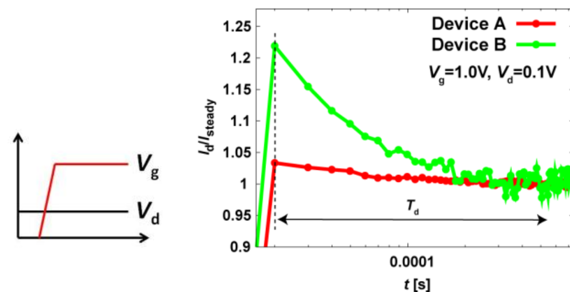

Fig. 2. Measured transient current response under constant drain voltage V_d of 0.1V. The currents are normalized by the saturation values. The measurement condition is shown in the left-hand-side figure.

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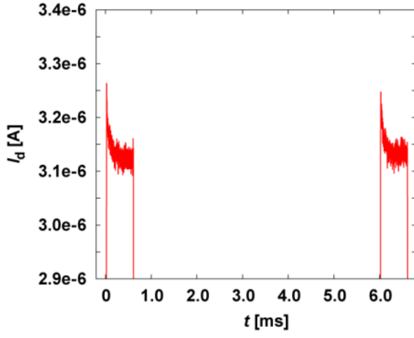

Fig. 3. Measured transient current response for repeated pulse input. The measurement condition is the same as that shown in Fig. 2.

III. 2D-DEVICE SIMULATION

To develop a compact model for the measured transient characteristics caused by the carrier trapping, an analysis with 2D-device simulations was carried out. Fig. 4a shows the energy distribution for the three different trap density-of-states studied, A, B, and C. The vertical lines denoted by I, II, and III describe the E_{fn}-E_c values at three different V_g of 0.5V, 1.0V, and 2.0V, respectively. Fig. 4b shows simulated normalized drain current as a function of time for three V_g values with different densities A, B, and C. The current value used for the normalization is the value of the trap density B, and the same switching condition as shown in Fig. 2 is applied. For the V_g=0.5V case (I), the B shows the highest trap density, resulting in the most pronounced current decay. For the V_g=2V case (III), the characteristics of the simulated currents are as expected from the density of state. These results demonstrate that the saturated currents after long switching on duration are mainly determined by the trap density for the corresponding E_c-E_f value at each given V_g.

Fig. 5 demonstrates the reason for the feature that the deep trap state influences the current at low V_g value and the shallow trap state influences at high V_g value. For small V_g values, the Fermi level, where the most occupation of trapping occurs, moves near to the middle of the bandgap. For large V_g values, on the contrary, the Fermi level approaches to the conduction-band edge. This leads the situation that carriers are mostly affected by traps with the shallow density-of-states. It is noticeable that the shallow trap density is mostly responsible for normal operation conditions.

IV. MODELING AND CALCULATIONRESULTS

We included the trap density in the Poisson equation explicitly as [2]

$$\nabla^2\phi = \frac{q}{\varepsilon_s}\left(p - n + N_D - N_A + N_{trap_D} - N_{trap_A}\right) \qquad (1)$$

where the donor like trap density N_{trap_D} is ignored in this study and only N_{trap_A} is considered, because we investigate here nMOSFET where major carriers are electrons under normal operation conditions. We implemented into HiSIM2, which can solve the above Poisson equation explicitly without any approximations.

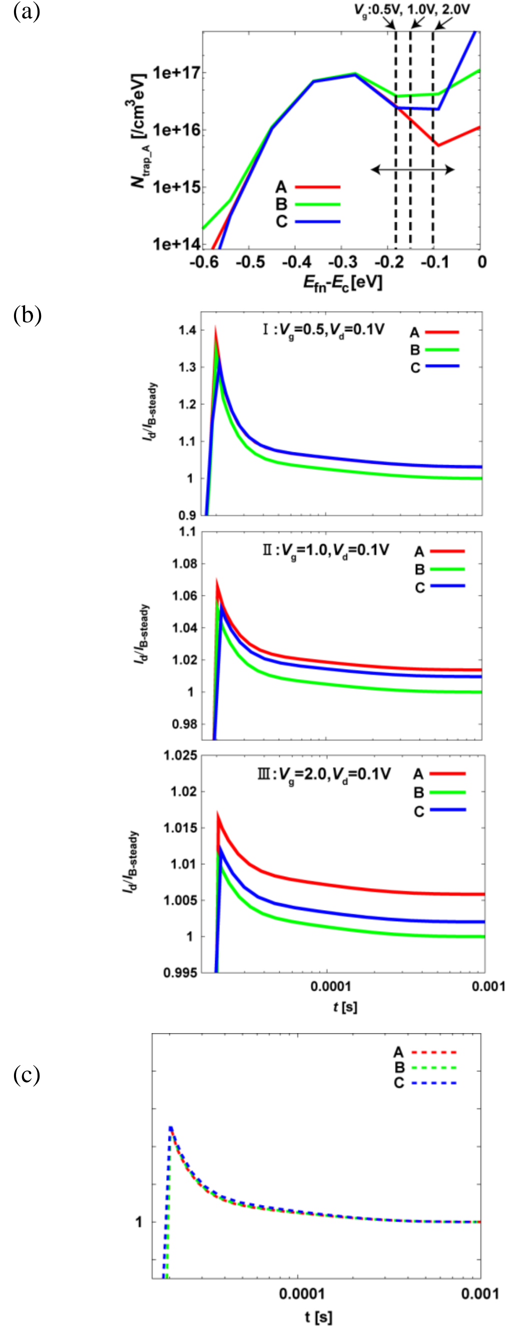

Fig. 4. (a) Trap density-of-states v used for 2D-device simulations. (b) Simulated transient characteristics for three different trap density-of-states (A, B, C) at three different V_g values (I, II, III). The current is normalized with each minimum values. The input pulse waveform is the same as shown in Fig. 2. (c) The same simulation results shown (b) at V_g=1.0V normalized for both initial and saturation currents.

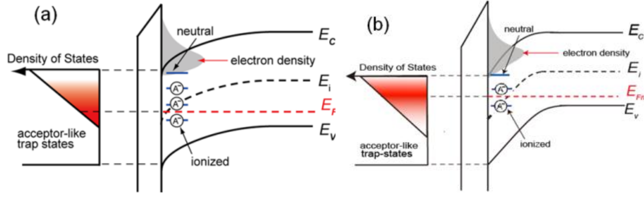

Fig. 5. Linearly distributed density of acceptor-like trap states within the bandgap and the Fermi level depicted (a) for relatively small V_g and (b) for relatively large V_s. For relatively small V_g the Fermi level lies nearly in the middle of the bandgap. The large V_g causes strong band bending, resulting in the Fermi-level movement to the conduction-band edge. This results in the increase of the shallow trap occupation.

Circuit simulators only work with node potentials. Therefore, the density-of-states must be integrated with respect to the energy and calculated as a function of E_f-E_c [3]

$$N_{\text{trap-A}} = N_0 \exp\left(\frac{E_f - E_C}{E_s}\right)$$

$$N_0 = g_c E_s \frac{\frac{kT}{qE_s}}{\sin(\frac{kT}{qE_s})} \quad (2)$$

where g_c is the density at E_f-E_c=0, and the inverse of E_s is the slope of the density of state. The energy difference E_f-E_c can be written as a function of the surface potential ϕ_s to transform into a function of V_g [4],

$$E_f - E_C = -\left(V_{ds} - E_V - kTln\frac{N_V}{N_A}\right) + \left(\phi_s - E_C\right) \quad (3)$$

It is observed that carriers require time to be trapped by grain boundaries. The time constant T_d of the trap/detrap process is modeled as the delay required for trap filling [5]

$$N_{\text{trap}}(t) = N_{\text{trap}}(t - \Delta t) + \Delta t / (\Delta t + T_d)\left(N_{\text{trap}}\left(V(t)\right) - N_{\text{trap}}\left(t - \Delta t\right)\right) \quad (4)$$

where $N_{\text{trap}}(V(t))$ gives the trap density at the bias condition of $V(t)$ without delay. This $N_{\text{trap}}(V(t))$ is extracted with measured *I-V* characteristics shown in Fig. 1. The extracted trap density as a function of E_f-E_c is shown in Fig. 6. Calculated *I-V* characteristics with the extracted trap densities are depicted in Fig. 1 together with the measurements. The time constant T_d is extracted to reproduce measured transient characteristics shown in Fig. 2. Fig. 7a depicts the normalized transient current as shown in Fig. 4c. The same decay characteristics are observed both for Device A and B. This concludes that the delay T_d is independent of the trap density. The same result is also observed in 2D-device simulation results (see Fig. 4c). The transient simulation results with the extracted time constant T_d accurately reproduces measured switching characteristics as shown in Fig. 7b. The drastic current reduction with the high trap density is well reproduced. The current reduction is attributed to the increase of the trapped charges, and the current reaches a steady state when the all possible trap states are filled by carriers, electrons for the studied case.

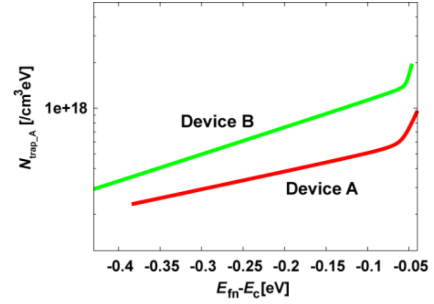

Fig. 6. Extracted trap density-of-states from Fig. 1 , where only $N_{\text{trap_A}}$ is depicted.

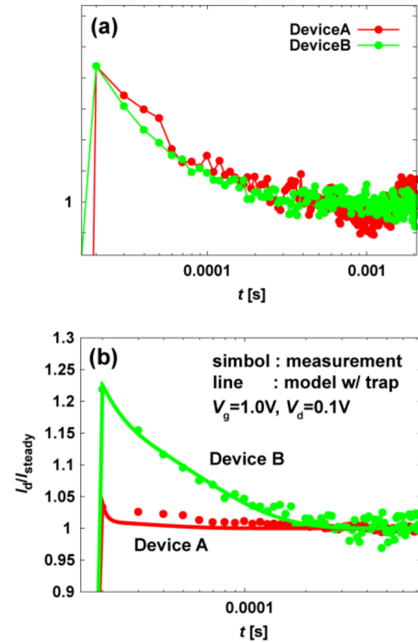

Fig. 7. (a) The same plot as shown in Fig.4c for the measured result shown in Fig. 2. (b) Comparison of model calculation results with the measured results as a function of time for the two studied devices (Device A and B). Currents normalized by the steady state current are depicted.

V. DISCUSSIONS

With use of the developed model, we investigate how the trap states affect transient characteristics of TFTs under device operation. First, we investigate the influence of V_g. Fig. 8 shows the relationship between V_g and trap density distribution. It is seen that the E_f-E_c value moves drastically to

the midgap, if V_g decreases down to 0.5V. This means that the relatively shallow trap sites influence on the device performances under normal operation conditions.

Fig. 9 shows the V_g dependence of the transient characteristics. The developed model can reproduce characteristics observed by the 2D-device simulation. Fig. 10 compares the dependence of the current response on the rise time of the pulse given as V_g. From this figure, the longer rise time t_r, the more current peak get smaller.

Simulation results with different pulse durations are shown in Fig. 11. For the simulation three different pulse durations are investigated; one is with very long duration of the V_g stress, medium frequency repetition of on/off, and rather high frequency. It can be seen that the high frequency operation shows negligible current degradation by trapping, while relatively slow switching demonstrates an obvious history effect. This concludes that a constant trap density extracted from I_d-V_g measurements cannot predict the accurate switching performance of circuits. Inclusion of a time constant for trap filling, resulting in a dynamic variation of the trapped charges, is the key to enable accurate simulation of TFT circuits.

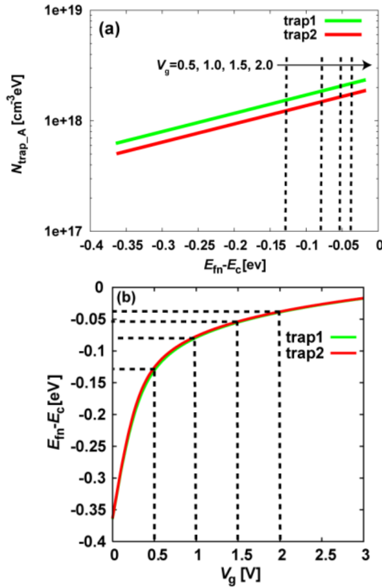

Fig. 8. (a) acc-like Density of States were plotted as a function of energy. (b) energy was plotted as a function of energy. Comparison these figure, we can know the relationship between V_g and energy.

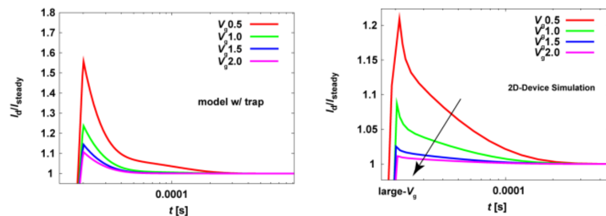

Fig. 9. Comparison of calculated transient characteristics for various V_g values with the developed model and the 2D-device simulator ATLAS.

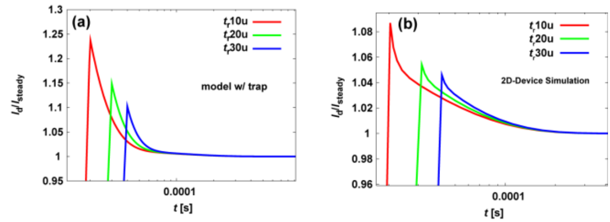

Fig. 10. (a) Calculated transient current response with the developed model for different rise times of the V_g switching. The bias condition is the same as shown in Fig. 2. (b) The same transient currents of 2D-device simulation results.

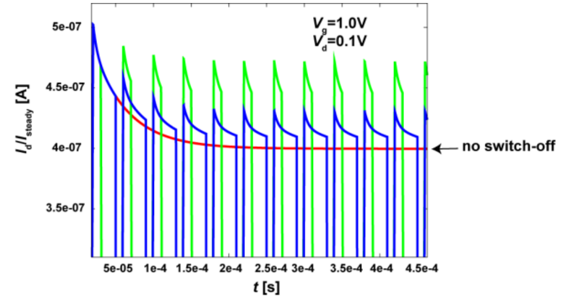

Fig. 11. Calculated transient currents in response to sequential input pulses of different durations. A clear history effect after the 1st input pulse is verified for long duration cases.

VI. Conclusion

We have developed a TFT model for accurate simulation of transient circuit performance by considering the time constant of carrier trap/detrap processes. It is verified that the model can reproduce measured results. The modeling concept is also applicable and essential for advanced ultra scaled MOSFET, where the influence of dynamic charge trapping cannot be neglected.

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