CoolSPICE: SPICE for Extreme Temperature Range Integrated Circuit Design and Modeling

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Abstract—**We developed a compact modeling methodology as well as a niche SPICE design suite to enable integrated circuit design for extreme environment operation. This new design suite, CoolSPICE™, with its low temperature models is expected to significantly improve reliability, performance and lifetime of electronics that are used for space or low temperature niche applications. CoolSPICE™ with its graphical user interface including schematics editor and plotter, as shown in Fig. 1, offer a convenient and accurate way to design wide temperature range integrated circuits.**

Keywords: SPICE, low temperature modeling, compact models, cryogenic electronics.

I. INTRODUCTION

Most electronic components are built for ambient room temperature and terrestrial applications. Most of the electronics design software that has been developed does not even give results for extreme temperature conditions. On a more basic level, distributed and compact device simulation codes have previously been developed mainly for the design of components that operate at ambient room temperature, or within the limits of commercial (-40 °C to 85°C) or military (-55°C to 125°C) temperature range of operation. The details of the semiconductor physics that occur at cryogenic temperatures simply has not played a sufficiently large role in electronics design development to provide the existing knowledge base necessary for robust cryogenic development.

We developed CAD tools, models and methodologies for design of integrated circuits that operate in extreme environments with focus on cryogenic temperatures down to 4K. These new tools and methodologies will give rise to circuit designs that minimize the requirements for external heat sources that are currently often necessary for operation of electronics in the very cold environments of space. Cryogenic technology would significantly improve reliability, performance and lifetime of electronics that are used for space applications, especially for space exploration.

For instance, in Fig. 2 we show test devices and circuits that were fabricated in a Silicon-on-Sapphire (SOS) technology and tested at cryogenic temperatures and under total ionizing dose radiation environments. Compact models in Verilog-A and C-programming languages were developed for these devices which allowed us to successfully simulate circuit operation at temperatures as low as 5K. Further, we also developed physics based distributed models for SOI devices that provided insight into device operation at temperatures as low as 20K. The new cryogenic models will greatly reduce the chances of error during actual circuit implementation, and thus reduce the number of design cycles, and decrease fabrication times and expenses.

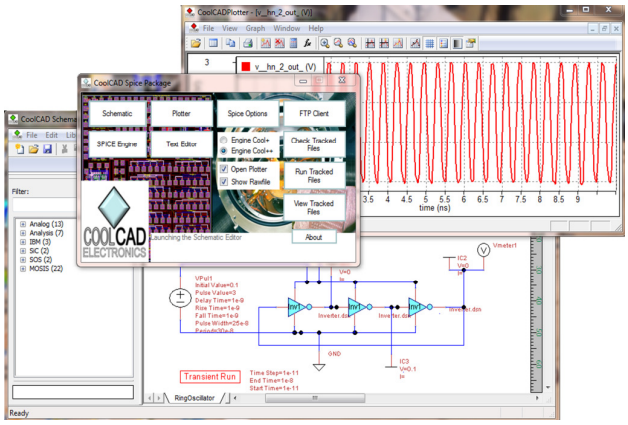

Fig. 1: CoolSPICE console, schematics editor and plotter.

II. COMPACT MODEL DEVELOPMENT FOR CRYOGENIC ELECTRONICS

A. *Method*

Low temperature compact models for various process design kits are developed using unique circuits and models, which are derived from novel physics-based modeling techniques and verified by experiments. More specifically, to develop extreme environment compact models and SPICE tools, we follow a multi-tiered approach as detailed below.

• Design and layout of test structures in the desired technology node using its process design kit. An example test IC laid out and had been fabricated is shown in Fig. 2.

o Different length and width MOSFETs: corner (small/large length and narrow/wide width) devices, as well as length-, width- and length-width scale MOSFETs.

o Fundamental circuits such as ring oscillators and current amplifiers for assessing DC, AC and transient operation.

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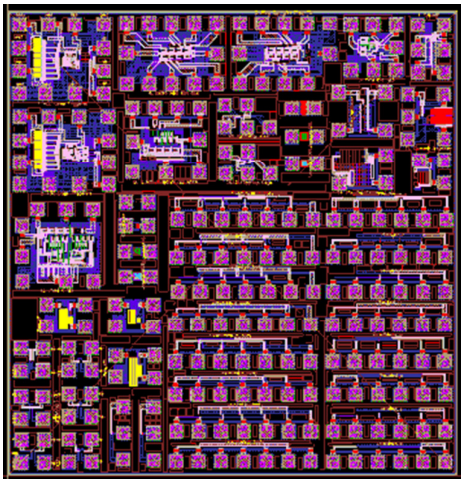

Fig. 2: A 3mm×3mm 0.5µm Silicon-on-Sapphire (SOS) test chip designed and fabricated in Peregrine's 0.5 µm process.

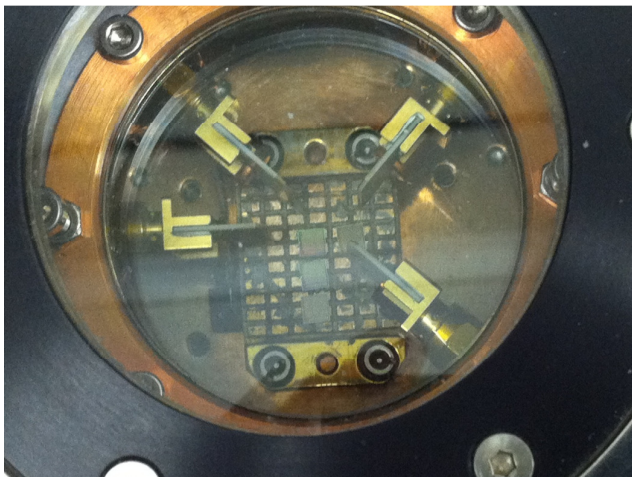

Fig. 3: Cryogenic chamber and test ICs measured.

• Cryogenic experiments to obtain current-voltage characteristics of test structures at temperatures ranging from 4K to 300K. These measurements are performed in a cryogenic chamber as shown in Fig. 3, or in a 6K cryostat.

• SPICE model development for the technology node measured.

o Identification of technology and low temperature related equations.

o Extraction of model parameters including those used in the standard BSIM model as well as the newly added equations.

o Incorporation of the new model into the SPICE code.

o Creation of model symbols, and related CoolSPICE™ accessories.

B. Extreme Temperature Compact Model

Compact models refer to sets of analytical equations that provide the output characteristics of a device based on given inputs. In the case of a MOSFET, the inputs are terminal voltages (biases applied physically to gate, drain, source, and in some cases to body connections) and the outputs are generally the currents flowing through these terminals. Since compact models are composed of algebraic equations relating voltages to currents, they are significantly faster than the differential equation based distributed models. This enables simulating large circuits at relatively fast speeds, enabling performance predictions of integrated circuits with millions of transistors. Hence compact models are at the forefront of circuit design. They give rise to first-pass chip designs, saving money and time.

Among the compact models already established for room temperature circuit design (and commonly used in very large scale integrated circuit design), we have chosen the BSIM compact model. (Just to give an idea about the complexity of the model, we would like to mention that the BSIM equation set accepts roughly 800 independent parameters and the source code written in C language is approximately twenty-thousand lines.) This decision is based on its wide usage by prominent foundries such as IBM and Peregrine.

The failure of existing models to predict low temperature operation is not related to a fundamental change of the standard conceptual framework of MOSFET operation. It is rather related to the numerical approach of compact model derivation as well as new physics that affect operation at low temperatures [1-5]. The MOSFET channel forms for large enough gate biases and the source/drain retain their high conductance due to dopant impurity band formation and its merging with the silicon conduction band. However the low temperature operation introduces additional physics that needs to be included into the room temperature equation set to obtain matches between experiments and simulations. To this end, we build on the standard model, and modify the BSIM4 code to account for these new phenomena [1,2]. Some of these modifications account for the following:

• Partial dopant ionization.

• Impact ionization.

• Changes in channel quantization, drain induced barrier lowering, and channel modulation.

• Channel-source barrier injection.

• Temperature and bias dependent mobility, and subband formation.

For example, we discuss the dopant ionization model next. More specifically, previous low temperature models include partial ionization of the lightly doped drain region at very low temperatures as follows [3,6]:

$$R_{SD}(E_{LDD}) = R_{SD0}\frac{1}{D^+/_D}, \quad (1)$$

$$D^+/_D = 1 + \left(D_O^+/_D - 1\right)/(1 + \gamma_o exp(-B/E_{LDD})), \quad (2)$$

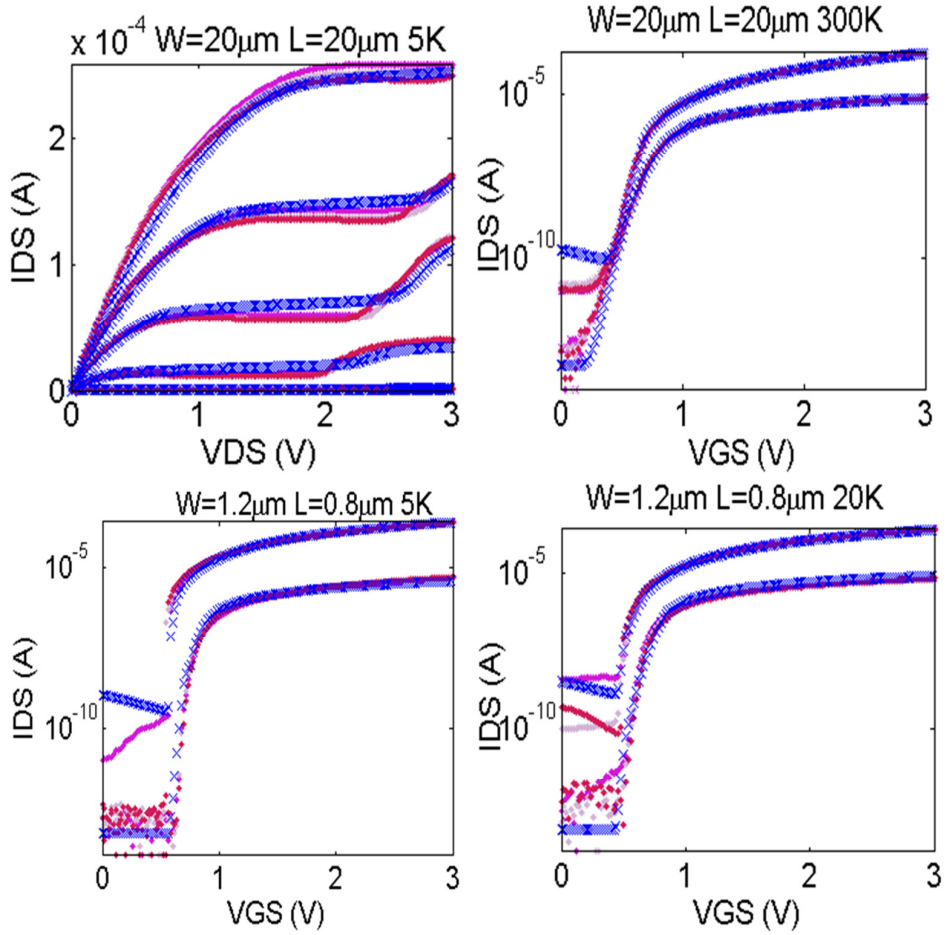

Fig. 4: Example comparisons of small and wide 0.5µm SOS MOSFET measurements (several dies) with CoolSPICE™ compact models (blue curves) at 5K, 20K and 300K. Fits were obtained for various length- and width-scale MOS devices at several temperatures in the 5K-300K range.

where R_{SD0} is the minimum source-drain series resistance, ${D^+}/{_D}$ is the ratio of ionized dopants to total dopant concentration, E_{LDD} is the drain induced electric field, and the other parameters are empirically determined fitting parameters. Here the ionization is assisted by the drain field, and the ionization is partially due to shallow dopant impact ionization.

Our investigations indicate that the dopant ionization at the edges of the channel (for example at the lightly doped drain region) is affected by the gate field as well as the drain field. Therefore, we introduce a drain and gate voltage dependent series drain and source resistance to be used in our compact cryogenic MOSFET model, as follows:

$$R_{SD}(VDS, VGS) = R_{SD0}\frac{1}{{D^+}/{_D}}, \quad (3)$$

$${D^+}/{_D} = 1 + [g(VDS) - 1]/[1 + f(h(VGS))] \quad (4)$$

Here $g(VDS)$ is an exponential function of VDS with two fitting parameters, as written below:

$$g(VDS) = A \times \exp(B \times VDS). \quad (5)$$

Additionally, $f(h(VGS))$ is a function of $h(VGS)$ with two fitting parameters, and $h(VGS)$ is equal to the T2 [=m*×(VGSe-VTH)/(n×Vt)] variable defined in BSIM4 [7], as shown below:

$$f(h(VGS)) = C \times T2^D. \quad (6)$$

Similar to the Fermi level, T2 takes on rapidly changing values in the subthreshold region of operation, and it remains relatively constant in the linear and saturation regions of operation.

C. *Example Experiments and Simulations*

The open source Spice3 circuit simulator along with the BSIM source code has been adapted to include the low temperature models described in the previous section as well as new geometry dependent parameters for BSIM4 modeling of SOS devices at various temperatures. The geometry dependence is provided using a custom-written table modeling approach (in Verilog-A built-in library items were used, but in C source code such functions do not exist, and therefore we needed to write custom functions to achieve interpolation and

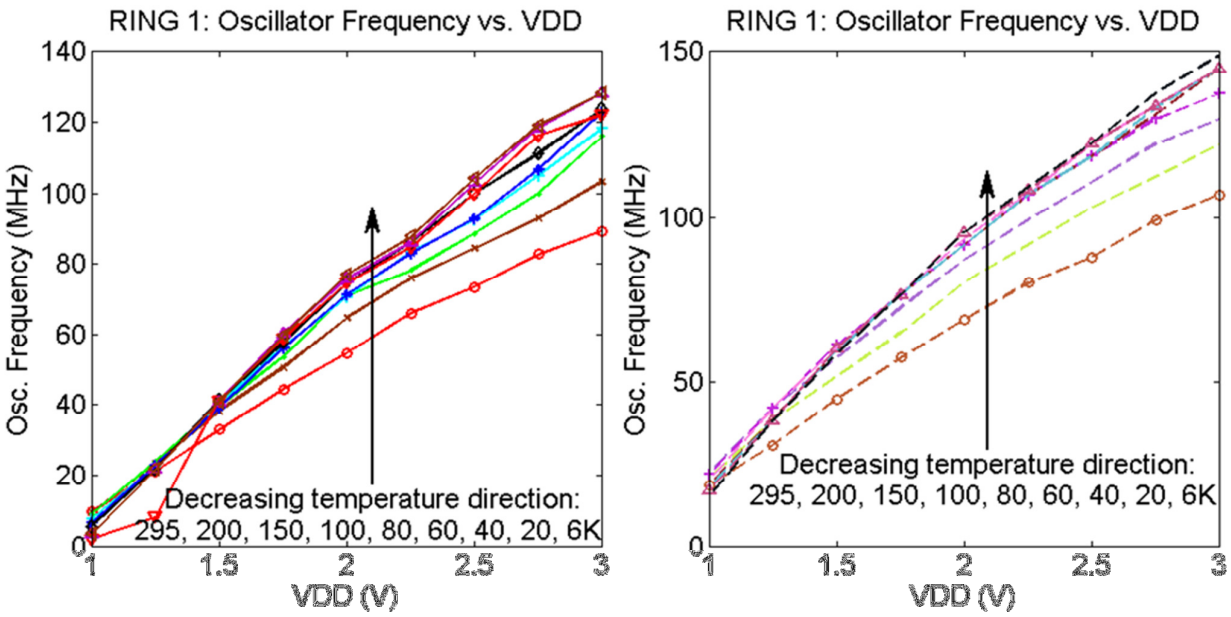

Fig. 5: Measured (left) and simulated (right) ring oscillator curves at temperatures ranging from 6K to 300K

extrapolation for different width, length and temperature scales). In addition, new parameters were added to the BSIM4 model. The Spice3 implementation was tested and verified against the Verilog-A implementation of the table model and also with experimental data.

As an example, we show in Fig. 4, current-voltage comparisons of small and wide 0.5 µm SOS MOSFET measurements (several dies) with CoolSPICE™ compact models (blue curves) at 5K, 20K and 300K.

We have chosen a standard ring oscillator (an odd number of inverter circuits, composed of an NMOS and a PMOS, connected in series with the output of the last stage connected to the input of the first stage) as one of our test circuits for cryogenic model evaluation. Figure 5 shows measured and simulated ring oscillator curves at temperatures ranging from 6K to 300K. As can be seen in Fig. 5, the simulated data match the measured data reasonably well. We attribute the differences between experimental and calculated (especially for the circuit that does not account for any internal parasitics) curves to internal capacitive and resistive parasitics, and the external resistances on the supply lines (due to long lines needed from inside the cryostat where circuits were cooled to outside). The internal parasitics can directly lower the oscillation frequency by increasing the circuit time constants. The latter can give rise to reduced oscillation frequencies due to voltage drops on resistive elements, resulting in lower biases on the actual circuit.

III. Conclusion

In summary, we developed a low temperature compact modeling suite compatible with standard SPICE engines. To achieve this, we obtained cryogenic models and equations that reflect low temperature operation of MOS devices and circuits. The new simulator CoolSPICE™ offers a SPICE-type tool to perform circuit design at extreme environments for a given process design kit, and therefore obviates the need for redundant circuits and exotic processes for achieving first-pass circuit operation.

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