Correlation between Gate Charge and Gate Capacitances of Power MOSFETs and Extraction of Related BSIM3/4 Model Parameters

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***Abstract*— Gate charge of power MOSFETs is one of the dominant power switching loss factors in high-speed power converters [1]. Understanding its correlation with gate capacitances can provide useful insights on device performance and driver circuit design [2].**

In this paper, the correlation between gate charge and gate capacitances is studied. We show that gate charge transient signals $V_{\rm GS}(t)$ and $V_{\rm DS}(t)$ can be derived directly from gate capacitance measurements. An accurate method to extract BSIM3/4 model parameters related to capacitance modeling of power MOSFETs is also developed. Excellent agreement between simulation and measurement is demonstrated.

Introduction

Power MOSFETs, such as DMOS, LDMOS, IGBT, etc have been used in a wide range of power applications involving switching and amplification [3]. To design power circuits and systems, it is necessary to fully understand and make use of gate charge information of power devices [4]. A typical gate charge curve shows gate-to-source voltage of a power device as a function of total gate charge (charging time $\times$ gate charging current). Designers can use this information to conveniently calculate the switching time and switching power losses.

Several studies have been published on the understanding and simulation of gate charge [3], [4]. In this work, we first review the gate charging dynamics based on classical MOSFET theory. Then, we show how gate charge is correlated to the nonlinear gate capacitances of power MOSFETs. This correlation is also verified using measurement data.

Compact models are often used to simulate electrical behaviors of power MOSFETs [5], [6]. Model parameters of a selected model need to be extracted from electrical measurement. To correctly simulate gate charge, it is important to extract parameters related to gate capacitance model accurately. In [7], a method to extract parameters from gate charge measurement was proposed for IGBT devices. The structure and operation of low-voltage power MOSFETs (LDMOS and DEMOS) devices are different from IGBT devices. BSIM3/4 [8] based subcircuits are popular for modeling these devices [6]. BSIM3/4 are the standard MOSFET models widely used in industry. It provides accurate modeling of all nonlinear gate capacitances. Based on device physics, a new method to extract these key parameters of BSIM3/4 from gate charge measurement is developed.

Generalized Gate charging dynamics

A basic gate charge measurement setup is shown in Fig. 1. A constant independent current source of $I_{\rm G}$ is applied to the gate and charging the gate capacitances. We have

$$I_{\rm G} \equiv \frac{dQ_{\rm G}(t)}{dt}\,, \tag{1}$$

or explicitly

$$\begin{aligned}\frac{dQ_{\rm G}(t)}{dt} &= \frac{\partial Q_{\rm G}}{\partial v_{\rm G}}\frac{dv_{\rm G}}{dt} + \frac{\partial Q_{\rm G}}{\partial v_{\rm D}}\frac{dv_{\rm D}}{dt} + \frac{\partial Q_{\rm G}}{\partial v_{\rm S}}\frac{dv_{\rm S}}{dt} + \frac{\partial Q_{\rm G}}{\partial v_{\rm B}}\frac{dv_{\rm B}}{dt} \\ &= C_{\rm GG}\frac{dv_{\rm G}}{dt} - C_{\rm GD}\frac{dv_{\rm D}}{dt} - C_{\rm GS}\frac{dv_{\rm S}}{dt} - C_{\rm GB}\frac{dv_{\rm B}}{dt}.\end{aligned} \tag{2}$$

Here $C_{\rm GG}$ is the total gate capacitance, and $C_{\rm GS}$, $C_{\rm GD}$, $C_{\rm GB}$ are gate-to-source, gate-to-drain, gate-to-body capacitances, respectively. They are bias-dependent and contain both intrinsic (channel) and extrinsic (overlap regions) contributions. Usually the source and body are grounded. Thus, (2) can be simplified as

$$I_{\rm G} = C_{\rm GG}\frac{dV_{\rm GS}}{dt} - C_{\rm GD}\frac{dV_{\rm DS}}{dt}\,. \tag{3}$$

A typical gate charge curve is shown in Fig. 2. Starting from time $t = 0$, the gate voltage $V_{\rm GS}$ begins to increase while the gate is being charged. When $t < t_1$, there is no current flowing between the drain and the source since $V_{\rm GS}$ is below threshold voltage $V_{\rm TH}$. The driving current $I_{\rm DC}$ is flowing through the diode D (or a rectifier). $V_{\rm DS}$ remains at supply voltage $V_{\rm DD}$ because the voltage drop across the diode is negligible. Hence, $dV_{\rm DS}/dt = 0$, and

$$I_{\rm G} = C_{\rm GG}\frac{dV_{\rm GS}}{dt}\,. \tag{4}$$

It should be pointed out that all three capacitances ($C_{\rm GS}$, $C_{\rm GD}$, and $C_{\rm GB}$) are being charged. In this charging phase, $C_{\rm GS}$ may be dominant for DMOS transistors

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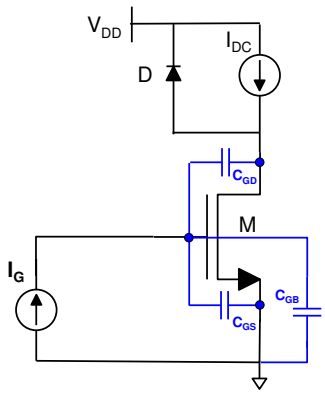


Fig. 1. A basic power MOSFET gate charge measurement setup. $I_{\rm G}$ is the charging current, $I_{\rm DC}$ is the driving current in parallel with a diode D. A simple lumped MOSFET capacitance model is also shown to illustrate the charging components.

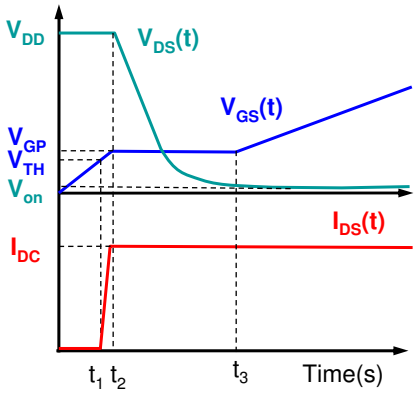


Fig. 2. Typical gate charge waveforms of power MOSFETs.

[9]. For LDMOS, $C_{\rm GB}$ will be dominant. Also, $C_{\rm GD}$ can be comparable to $C_{\rm GS}$ because of the contribution of drift region capacitance. This needs to be considered in parameter extraction and simulation of gate charge for LDMOS.

When $V_{\rm GS}$ reaches $V_{\rm TH}$ at time t_1, the drain current starts to increase rapidly until it reaches $I_{\rm DC}$ at time t_2. $V_{\rm DS}$ remains at $V_{\rm DD}$ as long as the diode is still conducting. The first charging phase ($0 < t < t_2$) is usually called "turn-on region".

In the second phase of gate charging process ($t_2 < t < t_3$, also called "gate plateau region"), the drain current remains at $I_{\rm DC}$ and thus $V_{\rm GS}$ is constant, i.e. $dV_{\rm GS}/dt = 0$. $C_{\rm GS}$ is no longer charged by $I_{\rm G}$. (3) is simplified to

$$I_{\rm G} = -C_{\rm GD}\frac{dV_{\rm DS}}{dt}\,. \tag{5}$$

Here $C_{\rm GD}$ is a highly nonlinear function of $V_{\rm DS}$ and increases as $V_{\rm DS}$ decreases.

After $t > t_3$, the device enters linear operation region (third charging phase). $V_{\rm DS}$ remains at a small value $V_{\rm on} = R_{\rm DS,on} \times I_{\rm DC}$, where $R_{\rm DS,on}$ is the on-resistance. $V_{\rm GS}$ continues to increase proportionally to the charging current as controlled by (4).

Correlation between gate charge and gate capacitances

As discussed in the previous section, $V_{\rm DS}(t)$ and $V_{\rm GS}(t)$ are governed by nonlinear gate capacitances through (4), (5). When $t < t_2$, integrating (4) gives

$$t = \frac{1}{I_{\rm G}}\int_0^{V_{\rm GS}} C_{\rm GG}(V_{\rm DS} = V_{\rm DD})dV'_{\rm GS}\,. \tag{6}$$

It means in the first charging phase $V_{\rm GS}(t)$ can be reconstructed by integrating total gate capacitance $C_{\rm GG}$ measured at $V_{\rm DS} = V_{\rm DD}$ from $V_{\rm GS} = 0$ to $V_{\rm GP}$.

Similarly, in the second charging phase, integrating (5) gives

$$t = t_2 + \frac{1}{I_{\rm G}}\int_{V_{\rm DS}}^{V_{\rm DD}} C_{\rm GD}(V_{\rm GS} = V_{\rm GP})dV'_{\rm DS}\,, \tag{7}$$

where $V_{\rm on} \le V_{\rm DS} \le V_{\rm DD}$. $V_{\rm DS}(t)$ can be derived from $C_{\rm GD}$ measured at $V_{\rm GS} = V_{\rm GP}$ while sweeping $V_{\rm DS}$ from $V_{\rm DD}$ to $V_{\rm on}$.

When $t > t_3$, $V_{\rm GS}(t)$ can be obtained from $C_{\rm GG}$ measured at $V_{\rm DS} = V_{\rm on}$ through the following integral

$$t = t_3 + \frac{1}{I_{\rm G}}\int_{V_{\rm GP}}^{V_{\rm GS}} C_{\rm GG}(V_{\rm DS} = V_{\rm on})dV'_{\rm GS}\,. \tag{8}$$

Fig. 3 shows the gate charge comparison between calculation and direct measurement for an LDMOS device.

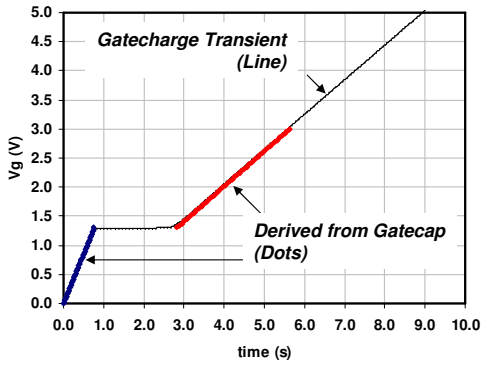
BSIM3/4 parameter extraction method suitable for low voltage DE/LD MOSFETs

Fig. 4 shows the cross-section of an LDMOS transistor. The relative diffusion of pwell into nwell underneath the gate poly defines the channel. This device can be modeled by a basic, simplified subcircuit as shown in Fig. 5. It consists of a core MOS modeled by BSIM3/4, an external drain resistor R and a source-to-drain diode (source and body are grounded). The capacitance of the lightly doped drift region is bias-dependent. In this subcircuit, it is modeled as the overlap capacitance.

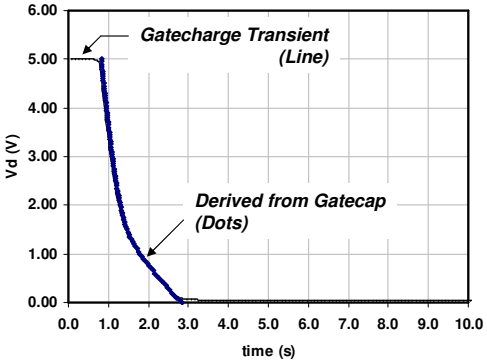
In BSIM3/4, the (drain-side) overlap charge equation is given by

$$\frac{Q_{\rm ov}}{W} = (\texttt{CGDO} + \texttt{CGDL})V_{\rm ov} - \texttt{CGDL} \times \left[V^*_{\rm ov} + \frac{\texttt{CKAPPA}}{2}\left(-1 + \sqrt{1 - \frac{4V^*_{\rm ov}}{\texttt{CKAPPA}}}\right)\right] \tag{9}$$

where W is the device width, $V_{\rm ov}$ is the voltage across the gate-drain overlap region and $V^*_{\rm ov} = 0.5(V_{\rm ov} + \delta_1 - \sqrt{(V_{\rm ov} + \delta_1)^2 + 4\delta_1})$, $\delta_1 = 0.02$. CGDO, CGDL, and



(a) $V_{\mathrm{GS}}(t)$ transient.



(b) $V_{\mathrm{DS}}(t)$ transient.

Fig. 3. Comparison of $V_{\mathrm{GS}}(t)$, $V_{\mathrm{DS}}(t)$ transient between calculation (dots) and direct measurement (lines) for an LDMOS device.

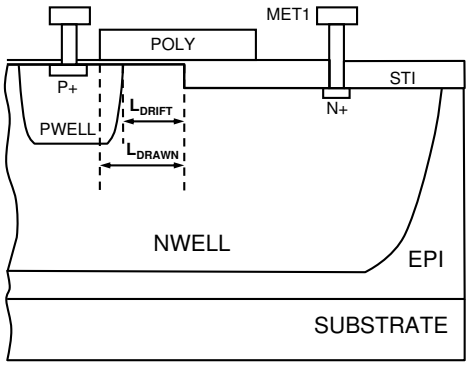


Fig. 4. Cross-section of an n-type LDMOS transistor. L_{DRIFT} is the length of drift region (n-type), and L_{DRAWN} is the drawn channel length of the device.

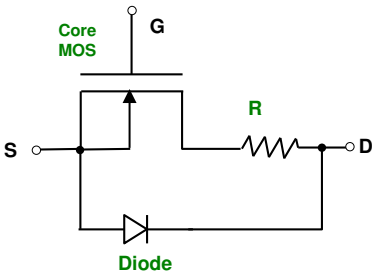


Fig. 5. A basic subcircuit to model low voltage LD MOSFETs.

CKAPPA are model parameters. Overlap capacitance is given by $\partial Q_{\mathrm{ov}}/\partial V_{\mathrm{ov}}$.

During the first phase of the gate charging process, $V_{\mathrm{DS}} = V_{\mathrm{DD}}$, $V_{\mathrm{GS}} < V_{\mathrm{TH}}$, $V_{\mathrm{GD}} \approx -V_{\mathrm{DD}}$, the device is off and there is no inversion capacitance. C_{GS} and C_{GD} only contain overlap capacitances. From (9) C_{GD} can be approximated as

$$C_{\mathrm{GD}} = W(\mathtt{CGDO} + \alpha_1 \mathtt{CGDL}), \tag{10}$$

where $\alpha_1 = 1/\sqrt{1 + 4V_{\mathrm{DD}}/\mathtt{CKAPPA}}$.

The total capacitance seen at the gate node is

$$C_{\mathrm{GG}}^{\text{phase 1}} = C_{\mathrm{GS}} + C_{\mathrm{GB}} + W(\mathtt{CGDO} + \alpha_1 \mathtt{CGDL}). \tag{11}$$

According to (4) , $C_{\mathrm{GG}}^{\text{phase 1}}$ can be found from the slope of $V_{\mathrm{GS}}(t)$ in this region. Denoting the slope as

$$S_1 = \left.\frac{\partial V_{\mathrm{GS}}(t)}{\partial t}\right|_{0<t<t_1}, \tag{12}$$

we have

$$C_{\mathrm{GG}}^{\text{phase 1}} = \frac{I_{\mathrm{G}}}{S_1}. \tag{13}$$

In the second phase of the gate charging process, $V_{\mathrm{GS}} = V_{\mathrm{GP}}$, and V_{DS} decreases rapidly after $t > t_2$. When $V_{\mathrm{DS}} > V_{\mathrm{GP}}$, the device is in saturation. C_{GD} is still mainly overlap capacitance and can be approximated as

$$C_{\mathrm{GD}}^{\text{phase 2}} = W(\mathtt{CGDO} + \alpha_2 \mathtt{CGDL}) \tag{14}$$

where $\alpha_2 = 1/\sqrt{1 + 4(V_{\mathrm{DD}} - V_{\mathrm{GP}})/\mathtt{CKAPPA}}$. According to (5), $C_{\mathrm{GD}}^{\text{phase 2}}$ can also be calculated from the slope of the linear part of $V_{\mathrm{DS}}(t)$,

$$C_{\mathrm{GD}}^{\text{phase 2}} = I_{\mathrm{G}} \left(-\left.\frac{\partial V_{\mathrm{DS}}(t)}{\partial t}\right|_{t_2<t\ll t_3} \right)^{-1}, \tag{15}$$

When $t > t_3$, $V_{\mathrm{DS}} \approx 0$ and $V_{\mathrm{GS}} > V_{\mathrm{GP}}$, the device is in linear region. C_{GG} contains both channel and overlap capacitances

$$C_{\mathrm{GG}}^{\text{phase 3}} = C_{\mathrm{GS}} + W\left[(L - \Delta L)C_{\mathrm{ox}} + \mathtt{CGDO} + \mathtt{CGDL}\right], \tag{16}$$

where $C_{\mathrm{ox}} = \epsilon/t_{\mathrm{ox}}$ is the channel capacitance per unit area. $\Delta L = 2\mathtt{DLC}$ where DLC is also a BSIM3/4 model parameter. Since the channel is inverted, contribution from the gate-to-body capacitance is ignored. Again,

$$C_{\mathrm{GG}}^{\text{phase 3}} = I_{\mathrm{G}} \left(\left.\frac{\partial V_{\mathrm{GS}}(t)}{\partial t}\right|_{t>t_3} \right)^{-1} \tag{17}$$

The total gate capacitance measured at $V_{\mathrm{GS}} = 0$, $V_{\mathrm{DS}} = 0$ is given by

$$C_{\mathrm{GG},0} = C_{\mathrm{GS}} + C_{\mathrm{GB}} + W(\mathtt{CGDO} + \mathtt{CGDL}). \tag{18}$$

Here $C_{\rm GS}$ and $C_{\rm GB}$ have the same values as in (11). Combining (18) and (11), one obtains

$$\texttt{CGDL} = \frac{C_{\rm GG,0} - C_{\rm GG}^{\rm phase\ 1}}{W(1-\alpha_1)}\,. \tag{19}$$

Substituting CGDL into (14),

$$\texttt{CGDO} = \frac{C_{\rm GD}^{\rm phase\ 2}}{W} - \alpha_2 \texttt{CGDL}\,. \tag{20}$$

Substituting (19), (20) into (16), one has

$$\texttt{DLC} = \frac{1}{2}\left[L - \frac{C_{\rm GG}^{\rm phase\ 3} - W(\texttt{CGDO}+\texttt{CGDL})}{WC_{\rm ox}}\right]\,. \tag{21}$$

In (21), $C_{\rm GS}$ has been neglected.

To use this method, BSIM3/4 DC parameters including $t_{\rm ox}$ are extracted first from data. DC characteristics fitting is important to model $V_{\rm GS}(t)$ in the plateau region. Then, CGDO, CGDL, DLC are calculated from (19)-(21).

We have applied the new extraction method on several DEMOS and LDMOS components of different voltage ratings. Fig. 6 shows the results for a 30V LDMOS transistor, demonstrating excellent agreement between simulation and measurement of gate charge. Fig. 7 shows that gate-to-drain capacitance $C_{\rm GD}$ is well modeled. To fit the peak and drop of $C_{\rm GD}$ at $V_{\rm GS} > 0$, it requires physical modeling of the channel lateral nonuniform doping effect and bias dependence of the drain resistance [10], which is beyond the scope of this work.

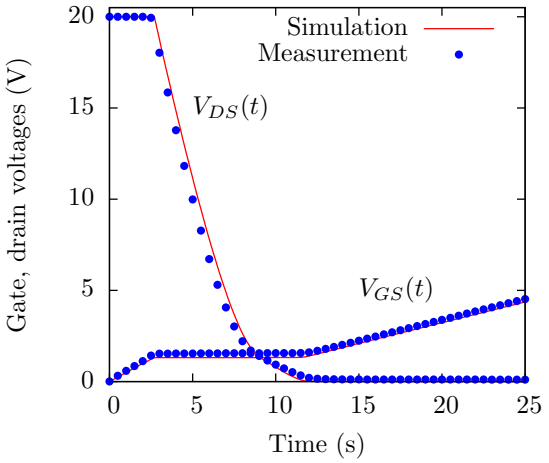


Fig. 6. Comparison between gate charge measurement and simulation for an LDMOS transistor.

Conclusion

We show that gate charge transient signals of power MOSFETs can be reconstructed from three individual gate capacitance measurements. An efficient and accurate method is also developed to expedite BSIM3/4 model parameter extraction process.

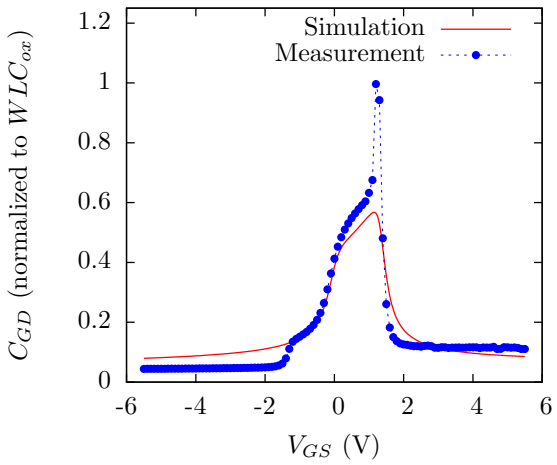


Fig. 7. Comparison of $C_{\rm GD}$ between measurement and simulation using model parameters (CGDO, CGDL, DLC) extracted directly from gate charge measurement.

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References

[1] R. Hueting *et al.*, "Gate-drain charge analysis for switching in power trench MOSFETs," *IEEE Trans. Electron Devices*, vol. 51, no. 8, pp. 1323 – 1330, 2004.

[2] V. Krishnamurthy *et al.*, "Simple gate charge (Qg) measurement technique for on-wafer statistical monitoring and modeling of power semiconductor devices," in *IEEE Int. Conf. on Microelectron. Test Structures*, march 2012, pp. 98 –100.

[3] R. McArthur, "Making use of gate charge information in MOSFET and IGBT data sheets," *Application note*, Advanced Power Technology, 2001.

[4] International Rectifier, "Use Gate Charge to Design the Gate Drive Circuit for Power MOSFETs and IGBTs", *Application note* AN-944, 2001.

[5] Y. Oritsuki *et al.*, "HiSIM-HV: A compact model for simulation of high-voltage MOSFET circuits," *IEEE Trans. Electron Devices*, vol. 57, no. 10, pp. 2671–2678, 2010.

[6] E. Seebacher *et al.*, "High voltage MOSFET modeling," in *Compact Modeling: Principles, Techniques and Applications*, G. Gildenblat, Ed. New York: Springer-Verlag, 2010, pp. 105–136.

[7] A. Claudio *et al.*, "Parameter extraction for physics-based IGBT models by electrical measurements," in *Power Electron. Specialist Conf. (PECS)*, vol. 3, 2002, pp. 1295–1300.

[8] *BSIM3 Version 3.3 User's Manual*. University of California, Berkeley, USA,

[9] B. Baliga, *Fundamentals of power semiconductor devices*. Springer Verlag, 2008.

[10] Y. Chauhan *et al.*, "Compact modeling of lateral nonuniform doping in high-voltage MOSFETs," *IEEE Trans. Electron Devices*, vol. 54, no. 6, pp. 1527–1539, 2007.