Predictive TCAD Approach for the Analysis of Hot-Carrier-Stress Degradation in Integrated STI-based LDMOS Transistors

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***Abstract*— A physically-based approach suitable for TCAD analyses has been developed for the hot-carrier-stress (HCS) degradation prediction in lateral DMOS transistors with shallow trench isolation (STI). The measured linear drain-current degradation ($\Delta I_{D,lin}$) induced by HCS is nicely reproduced by TCAD results for different LDMOS devices at significant stress conditions on an extended range of stress times and current drifts. A quantitative understanding of the generation kinetics and spatial distribution of the interface-trap concentration (N_{it}) along the Si/SiO_2 interface is obtained. TCAD results confirmed that interface traps are mainly formed at the STI corner, where the use of the charge-pumping technique fails due to the thickness of the STI oxide which limits the effects of the applied gate biases.**

I. Introduction

Lateral DMOS transistors are widely used to realize integrated high-current high-voltage devices in mixed-signal technologies due to their compatibility with standard CMOS devices. The extended drain architecture with shallow trench isolation oxide (STI) and the “RESURF” effect [1] gives a good specific resistance versus breakdown voltage trade-off. The high operating biases and the structure of the device make STI-LDMOS devices particularly susceptible to hot-carrier stress (HCS) degradation [2], [3], [4], [5]. TCAD tools are commonly used to tailor the doping profiles to avoid hot-carrier spots along the current path. However, they do not provide a quantitative prediction of the device HCS degradation.

In this work, a degradation model for hot-carrier stress has been incorporated into the framework of the Synopsys TCAD tool [6]. The experimental results of the linear drain-current drifts ($\Delta I_{D,lin}$) have been nicely predicted over an extended range of biases, confirming that the hot-carrier spot at the STI corner leads to a significant interface-trap (N_{it}) generation and to the consequent linear current degradation.

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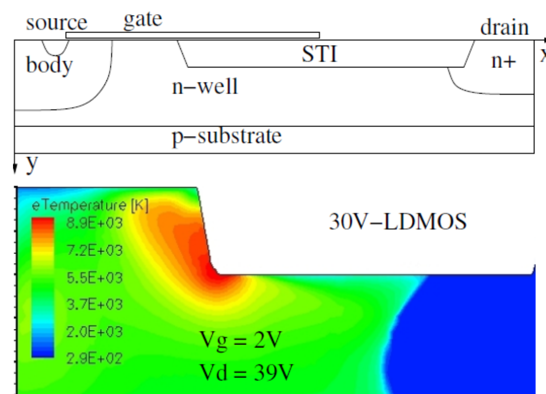

Figure 1. (Top) Schematic view of the STI-based LDMOS under study. (Bottom) 2D plot of the electron temperature in the LDMOS device at V_{GS}=2 V and high V_{DS}.

II. Device Description and Numerical Methods

Fig. 1 reports the 2D schematic view of the n-channel STI-LDMOS transistors investigated in this paper. A comprehensive TCAD-based analysis of the device behavior has been already presented in [7]. The simulation set-up was calibrated to experiments in DC and TLP regimes. The device geometry was directly derived from its layout and the description of the doping profiles was obtained from spreading resistance profiling data, secondary ion mass spectrometry measurements, and process simulation results.

Two-dimensional TCAD simulations have been carried out using [6]. Drift-diffusion equations have been solved coupled with the heat transfer equation. The electron temperature (T_n) is calculated as a post-processed solution of the energy-balance equation. At low V_{GS} and high V_{DS}, a clear peak of T_n is observed at the STI corner (Fig 1, bottom). The presence of a large density of highly energetic electrons flowing close to the Si/SiO_2 interface leads to a large trap generation. The consequent trapping of charges in the on-

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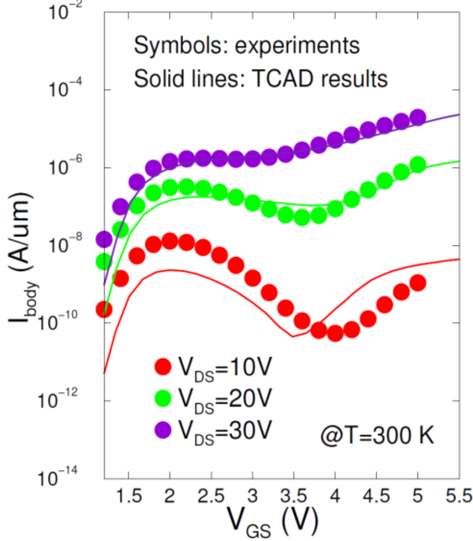

Figure 2. Body current vs. V_{GS}. Simulations have been carried out by using the thermodynamic transport model. At low V_{DS}, the gate-voltage modulation of the drain junction depletion is clearly observed. At high V_{DS}, impact ionization at the drain becomes dominant. The contributions are well predicted by the TCAD results.

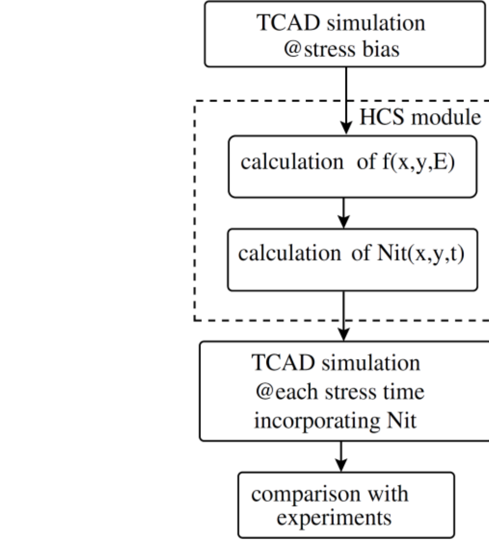

Figure 3. Simulation flow-chart. The HCS module calculates N_{it} by using the TCAD results at the stress bias. The DF is determined in each position (x,y) along the Si/SiO_2 interface by means of the non-Maxwellian formulation. The workflow ends with the simulation of the turn-on characteristic of the device in stressed conditions.

current condition causes large shifts (degradation) of the drain current itself.

A few investigations have been carried out on test devices with separated source and body contacts to further check the simulation deck. The body current characteristics are nicely reproduced on an extended range of biases (Fig. 2). The conventional worst-case condition of HCS corresponding to $V_{GS} \approx 2V$ is clearly observed and fairly predicted. At higher V_{GS}, impact ionization plays its major role and further increases the body current.

III. HCS DEGRADATION MODEL

The proposed degradation analysis is based on the incorporation of the N_{it} maps generated by an in-house solver into the TCAD device simulation. The simulation flowchart is shown in Fig. 3. The N_{it} distribution is computed for each stress time and at each node of the Si/SiO_2 interface by means of a physically-based model which considers the interplay between single-electron (SE) and multiple-vibrational (MVE) modes in microscopic scattering rates [8, 9]. They are controlled by integrals with the same functional structure. For the SE model, the scattering rate integral directly gives the forward reaction rate k_{SE}:

$$k_{SE} = \int_{E_A}^{\infty} f(E) g(E) v(E) \sigma(E) dE,$$

where E_A is the activation energy, f is the electron distribution function (DF), g and v are the density of states and group velocity, and σ is the reaction cross-section, given by:

$$\sigma(E) = \sigma_0 \left(\frac{E - E_A}{k_B T_L} \right)^p,$$

with p = 11 [8] and σ_0 are the model parameters. The MVE model has been implemented following [9].

The scattering rates have been calculated by accounting for the full band dispersion relation for the solution of the Boltzmann Transport Equation by means of the Spherical Harmonics Expansion [6]. Preliminary numerical results show that, due to the longitudinal lengths characterizing LDMOS devices, the observed DF are approximately local functions of the electric field and show features that can be properly captured by an analytical non-Maxwellian formulation like, e.g., the one proposed in [10]. Thus, an analytical function accounting for a numerical description of the band structure and emulating the carrier density and T_n given by the electro-thermal solution has been used obtaining an accurate description of the distribution function with efficient simulation times. In Fig. 4, the analytical distribution functions in different positions along the interface of the device has been compared with the numerical SHE-BTE data [6], showing a fair agreement up to very high energies.

The scattering rate models have been further modified in order to take into account the finite distribution of the activation energies for the Si/SiO_2 bonds in a disordered medium like the amorphous SiO_2 [11] [12], eliminating the assumption of discrete E_A values. Therefore, single E_A values are substituted by a bond-dispersion energy distribution and the reaction rates become functions of the bond energy. Following [11], the SE reaction rate has been modeled as:

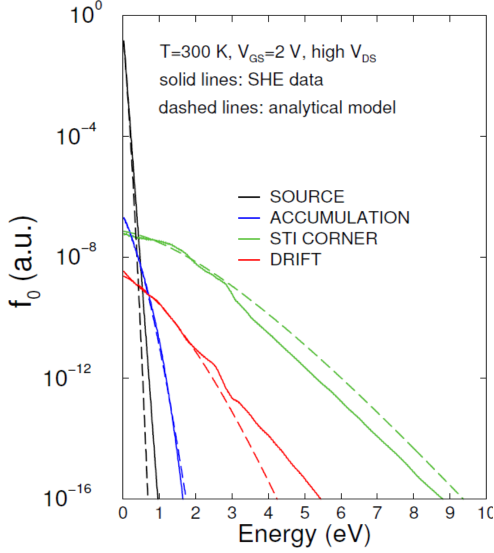

Figure 4. Comparison of the electron distribution function obtained from the SHE-BTE solution and from the analytical model for different positions along the Si/SiO_2 interface.

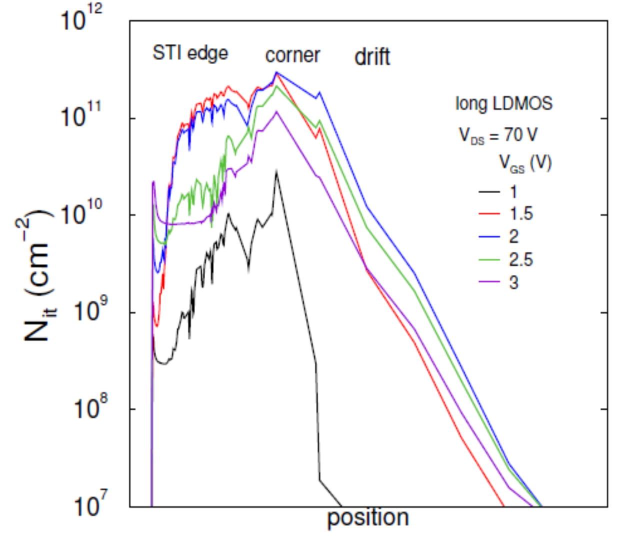

Figure 5. Interface trap concentration as a function of the position along the Si/SiO_2 interface for different stress biases at a fixed stress time.

$$k_{SE}(E) = k_{SE}(E_A)\exp\left[-\frac{E-E_A}{\lambda k_B T_n}\right],$$

where λ is a model parameter accounting for the effect of the tail of the distribution function.

In Fig. 5, the N_{it} profiles for different stress biases are reported, showing a strongly localized peak at the STI corner which is correlated to the high-energy tail of the electron distribution function. In such region, the major role is played by the single-electron contributions. No significant self-heating effects are found at such biases, and no hot carriers are expected in the channel and drift regions.

The time evolution of N_{it} at the STI corner is shown in Fig. 6 for two different devices: the curves follow a fast degradation trend for lower N_{it}, changing to a gradually saturating behavior for higher trap densities.

The N_{it} rate equations have been solved by assuming that the effect of the trap generation is negligible on the device stress kinetics, thus keeping the temperature and field distributions of the fresh condition. In addition, the models, modified in order to take into account the finite distribution of the activation energies, show the gradual change in the curve slopes which nicely correlates with the $\Delta I_{d,lin}$ experimental results.

IV. Results and Discussion

The model parameters have been calibrated by comparing the predicted $\Delta I_{d,lin}$ drifts with experiments. In Fig. 7, the $\Delta I_{d,lin}$ drifts measured at a fixed stress V_{DS} and long stress times are reported as a function of the stress V_{GS}. The experiments show

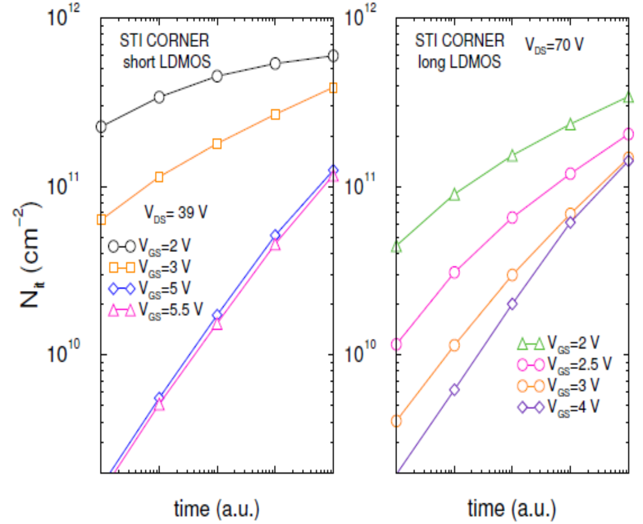

Figure 6. Interface trap concentration as a function of stress time for different stress biases in a (left) short and (right) long LDMOS device.

that the maximum current drift takes place at V_{GS} about 2 V, corresponding to the relative maximum of the body-current curves reported in Fig. 2. When further increasing the stress gate bias, the electric field at the source-side corner of the STI is reduced below critical levels, leading to a less severe HCS degradation. TCAD simulations have been performed with the new degradation model: the predicted $\Delta I_{d,lin}$ reported in Fig. 7 for different V_{GS} nicely compare with experiments. For low V_{GS}, the major role is played by the SE hot-carrier trap formation, which gives a peak of N_{it} localized at the STI corner as confirmed by the N_{it} profiles shown in Fig. 5 at different V_{GS} biases.

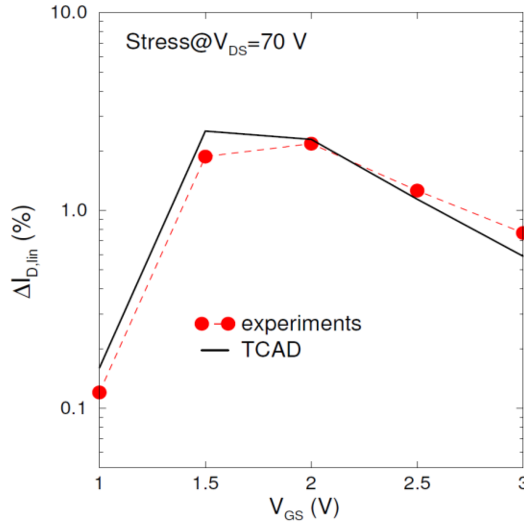

Figure 7. Linear drain-current relative variation as a function of the gate stress bias. The stress time is the same assumed in Fig. 5. TCAD data nicely predict the worst-case condition.

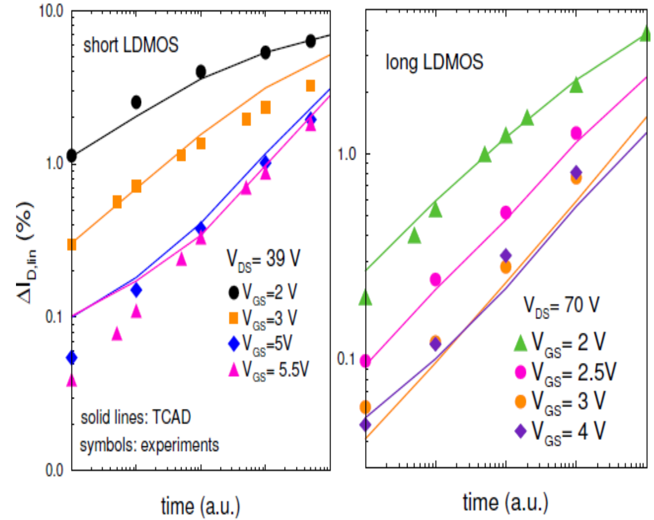

Figure 8. Linear drain-current relative variation as a function of time in a (left) short and (right) long LDMOS. The saturation of the HCS degradation is observed at V_{GS} = 5, 5.5 V and V_{GS}= 3, 4 V for the short and long device, respectively. TCAD data nicely predict experiments.

At V_{GS} > 3 V, a reduction of the $\Delta I_{d,lin}$ drifts is further observed with a minimum at $V_{GS} \approx 4$ V (not shown), in agreement with the N_{it} curves in Fig. 5. In such regime, different roles are played by the hot-carrier SE and MVE processes giving N_{it} distributed at the STI edge and along the drift region. In addition, the role played by N_{it} localized along the drift region clearly showed the need of using different model parameters along the planar interface with respect to the non-planar one. It is worth observing that a different orientation is experienced at the STI edge, leading to different physical and chemical features. Thus, two parameter sets have been separately calibrated on the short-LDMOS experiments and finally validated on the long-LDMOS ones.

The reduction of the SE degradation with increasing V_{GS} has been verified on both devices at different stress times (Fig. 8). In both cases, at $V_{GS} \geq 4$ V, the electron temperature is no longer localized at the STI corner but distributed along the whole Si/SiO_2 interface. The superposition of the degradation effects localized at the STI edge and in the drift region has been properly captured and the predicted $\Delta I_{D,lin}$ curves are nicely compared with the experimental data on the whole range of stress times and biases making use of the same parameter sets for the simulation of both devices.

V. Conclusions

A new approach for a fast TCAD degradation analysis suited for STI-LDMOS devices has been presented and verified. By using an analytical formulation of the electron distribution function accounting for the effects of a full band structure, the HCS worst-case conditions of two LDMOS devices are nicely predicted on an extended range of drift variations.

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