Failure Analysis of Power MOSFETs based on Multi-finger Configuration under Unclamped Inductive Switching (UIS) Stress Condition

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Abstract—**Failure analysis of power devices under avalanche breakdown condition during Unclamped Inductive Switching (UIS) stress is presented. This study provides a clear understanding of the dependency of various failure mechanisms on multi-cell or finger structures in n-type LDMOS power devices investigated by 2D and 3D technology-computer-aided-design (TCAD) simulation. The maximum amount of UIS energy (EAS) sustained by the device before failure is evaluated and is found to have a linear relationship with number of device finger and device-width. At a fixed inductive load, the dominant failure mechanism observed in devices with fewer fingers is current-failure. Time in avalanche, t_{AV} gets prolonged in multi-finger device design. As a result, self-heating is more resulting in temperature-failure in device with higher finger numbers.**

Keywords –Unclamped Inductive Switching (UIS); multi-fingers; n-LDMOS; time in avalanche (t_{AV}); current-failure; temperature-failure; Energy in Avalanche, Single pulse, (EAS).

I. INTRODUCTION

An increased level of reliability must be ensured for power devices used as switches for inductive load as in automotive Electronic Control Units (ECUs). Inductive load forces the power device into avalanche and possible device-failure due to significant over-voltage transient resulting during device switch-off [1, 2]. UIS test determines the maximum sustainable energy before device failure due to high current or temperature. An unclamped inductive load presents an extremely stressful switching condition for power MOSFETs since all the energy stored in the inductor during on state is dumped directly into the device during its turn off. Thus the UIS test condition represents the circuit switching operation to evaluate the ruggedness of power device, which specifies the maximum amount of avalanche energy that can be absorbed by the device prior to its catastrophic failure [3, 4].

Previous studies show various failure mechanisms for power MOSFETs based on the inductance value of the external load [3-8]. Among them, the current failure mode is said to be dominant at small inductances whereas temperature failure is seen in the device connected to large inductive loads [4-7].

The purpose of this paper is to provide a clear understanding of the failure mechanism of n-LDMOS at fixed inductance in power device applications and to evaluate the ruggedness, which characterizes the device's capability to withstand inductively induced over-voltage spikes [7]. The results investigated by 2D and 3D technology-computer-aided-design (TCAD) SYNOPSYS simulator [4-6] show the dependency of different failure mechanisms on device-finger numbers. This work also demonstrates that the relationship between device finger number or device width and maximum energy handling capability of the device is linear in nature.

II. UIS TEST SET-UP

A. *Test circuit and Schematic waveform*

Fig. 1 shows the common circuit and schematic waveforms of UIS test system [4-8]. The device is pulsed ON for a certain time period T_{ON}. During this time, current starts ramping up linearly to Ipeak as a function of the applied voltage V_{DD} and the inductor value L, as shown in (1).

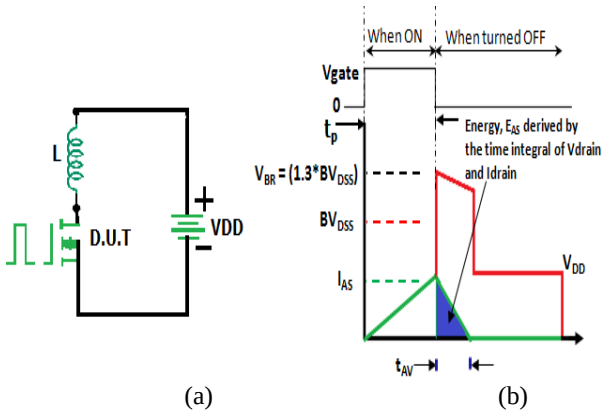

Figure 1. (a) The common UIS test circuit, (b) Current and voltage waveforms of the DUT under UIS test conditions

ISBN 978-0-615-71756-2

$$I_{PEAK} = (V_{DD}/L)*T_{ON} \quad (1)$$

The electrical energy stored in the inductor during T_{ON} is given by (2).

$$E = 1/2 * L * (Ipeak)^2 \quad (2)$$

When the device is switched-off, the energy built up on the inductive load is discharged to induce a high avalanche voltage (V_{BR}), which usually exceeds the device breakdown voltage (BV_{DSS}) by over 33% on the drain. During the switch-off transient time, current decreases linearly with a different slope given by (3). Consequently, a great deal of device self-heating is induced from the static isothermal level during the gate pulse time period [6-9]. As device has passed the avalanche test, the breakdown voltage falls towards its static level and the drain voltage goes down to supply voltage (V_{DD}).

$$di/dt = - (V_{BR} - V_{DD})/L \quad (3)$$

B. *Device Under Test (DUT)*

Fig. 2 shows the cross-sectional view of a MOS cell and its multi-finger structures with fingers ranging from 8 to 100 used as DUT to evaluate the maximum energy handling capability during UIS test. The single cell has a rated breakdown voltage and threshold voltage of around 42V and 1.2V respectively.

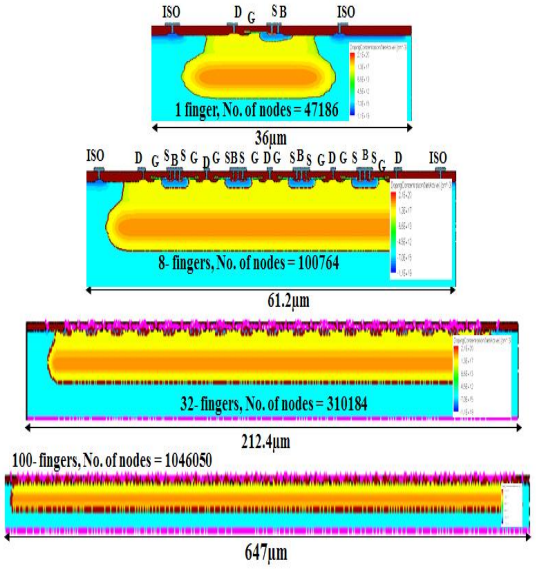

Figure 2. 2-D cross-sectional view of single cell n-LDMOS and its multi-finger (8, 32 and 100) structures with geometrical dimension

NPN parasitic transistor is comprised among the N+ layer on the source side, P-type buried layer that forms a channel, and the N- layer on the drain side. In addition, devices with different widths ranging from 1 to 5µm were performed using 3D Synopsys TCAD simulation for 8 and 16-fingers as shown in Fig. 3 to study the width-effect on maximum energy handling capability.

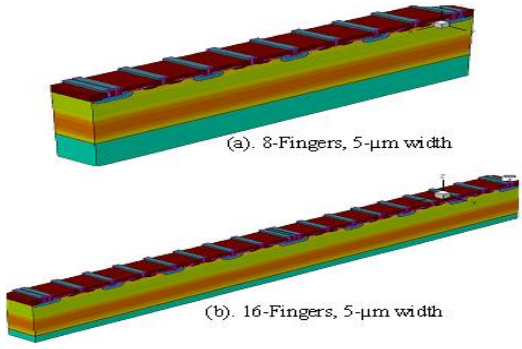

Figure 3. 3-D visualization of 8 and 16 -finger n-LDMOS device structure having width 5 µm

III. RESULT AND DISCUSSION

UIS Failure Mechanisms

When UIS stress is applied to power MOSFETs, two failure modes exist during the avalanche operation - current failure, which is initiated by biasing on the parasitic n-p-n transistor or by localized impact ionization and temperature failure, which results when the instantaneous chip temperature reaches critical value i.e. silicon-junction breakdown temperature (~650K) during the course of power MOSFET energy dissipation [6, 7]. Prior work inferred that current failure mode is dominant at small inductive loads while temperature failure usually occurs in device connected to large external inductances during UIS test [4-8]. However, the failure mechanism of device with multi-finger configuration has not been studied so far. Hence UIS test simulation was performed on multi-finger devices of various finger number and width at fixed value of inductive load.

During UIS test, voltage V_{BR} is applied at drain, which results in avalanche current, I_{AV}, flowing from the drain, through the resistance (R_B) of the P layer, to the source. The maximum energy, absorbed by the device is calculated considering the pass test-case prior to catastrophic device failure point by time integrating the drain voltage and drain current during avalanche duration (t_{AV}). Fig. 4 (a) shows the pass case for 8-finger n-LDMOS DUT during UIS test performed with a specific inductor value of 0.5 mH. When the applied gate-pulse width is increased, I_{AV} increases so that voltage on both ends of R_B rises above the V_{BE} on voltage of the parasitic NPN transistor, triggering it to on-state. As a result, an excessive current, which has been amplified by the parasitic transistor, flows to the collector side. The heat generated due to high current eventually destroys the parasitic transistor and hence contributes to failure of the DUT as shown in Fig. 4(b).

Fig. 5 shows the current distribution in the device with respect to Fig. 4(b) at different times. At time 294ns, high current flows through the device leading to device-failure. Current failure can be avoided by lowering the parasitic resistance component (R_B). Lower value of resistance will keep the voltage across R_B below the V_{BE} on voltage of the

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parasitic NPN transistor, thus not allowing the transistor to turn on.

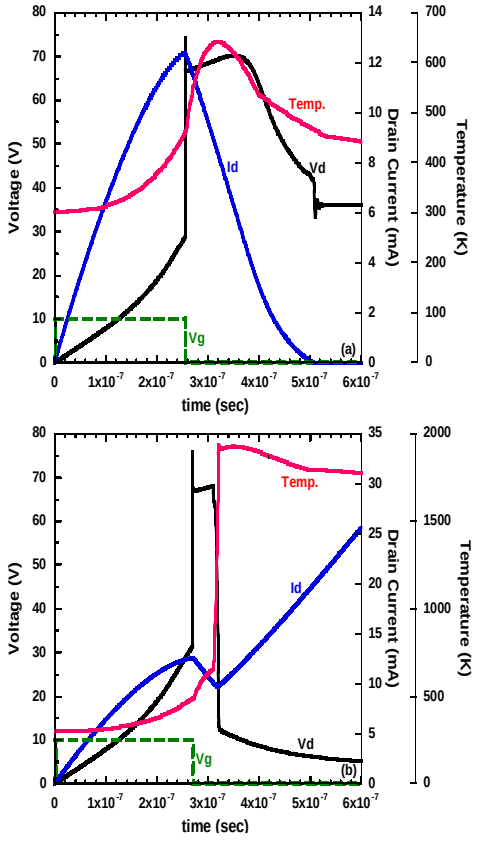

Figure 4. UIS waveforms show (a) pass case and (b) failure case for 8-finger device

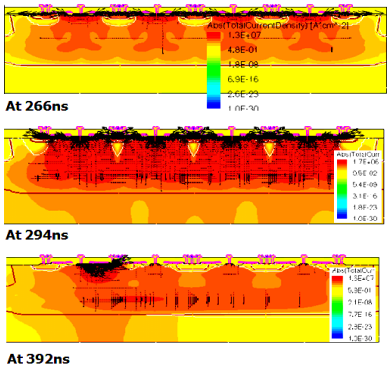

Figure 5. Current distribution in device during current failure

In multi-finger LDMOS the equivalent parasitic resistance gets lowered due to the parallel connection of parasitic resistance of all individual MOS cells hence avoiding the possibility of current failure. On the other hand, junction temperature rise due to self-heating during the UIS is more prominent in this case because larger devices cannot dissipate heat easily [7, 9].

Fig. 6 and 7 show the UIS failure waveforms for 32 and 100 finger devices respectively. Failure occurs due to the device temperature reaching the silicon junction breakdown temperature (650K).

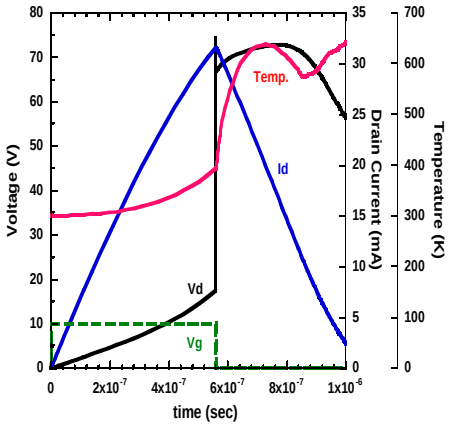

Figure 6. UIS waveforms showing failure case for 32-finger device

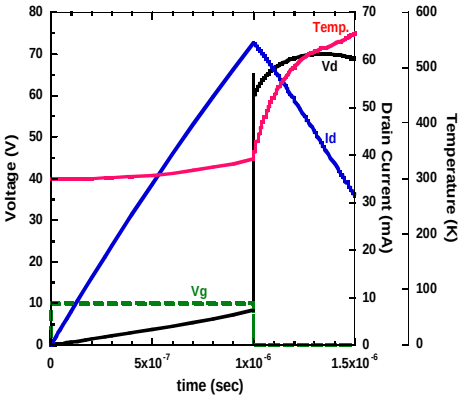

Figure 7. UIS waveforms showing failure case for 100-finger device

As can be seen from waveforms in Fig. 6 and 7, failure occurs mainly due to the critical temperature reached (~650K) while current during that time is seen to decrease linearly which is expected when the device is switched OFF. Knowing the peak transient junction temperature (Tmax) will help in predicting the MOSFET survival time during stress.

Fig. 8 shows the comparison of the UIS waveforms for devices with different finger number, ranging from 8 to 100 fingers, demonstrated by TCAD simulation. It clearly shows that the avalanche time is longer in device with more fingers. The variation of drain current with avalanche time, i.e., di/dt, is also determined by the RL time constant. The time constant of a series RL circuit (τ=L/R) determines the inductor charging and discharging time. For device with fewer fingers, the equivalent resistance of the multi-finger device is large and hence τ becomes small whereas, for device with more fingers, the equivalent resistance becomes small, hence τ increases.

Hence as finger number increases, the charging and discharging time becomes larger due to which drain voltage after Gate-pulse is OFF seems more flat for increasing finger

number. As a result, the generated heat is more thus causing temperature-failure in devices with higher number of fingers.

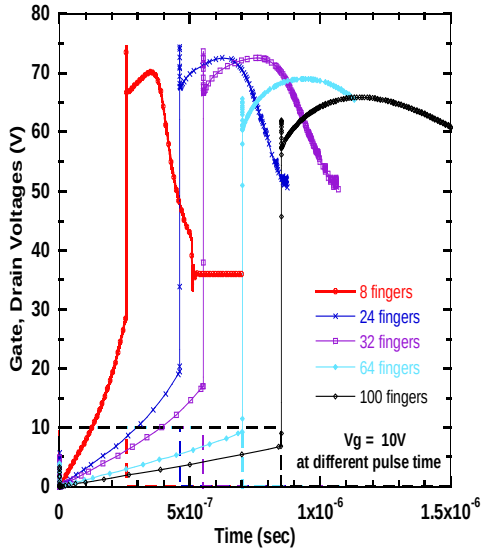

Figure 8. Gate and Drain voltage vs. time for increasing number of device fingers during UIS test

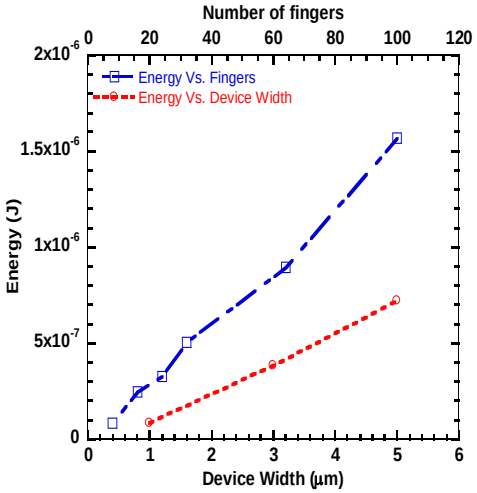

Figure 9. Energy in Avalanche, Single pulse, (EAS) vs. device finger numbers (8, 16, 24, 32, 64 and 100) and device width (1, 3 and 5µm)

Fig. 9 shows maximum avalanche energy versus device width and fingers. Due to increased area and more number of drain terminals in multi-finger devices, higher current density is observed in the device. This increased current leads to higher energy [$E = 1/2 * L * (Ipeak)^2$]. For a given inductance and bias conditions, the relationship between device finger number or device width and maximum energy handling capability of the device is linear in nature.

IV. CONCLUSION

Prior UIS failure criteria were based on the value of external inductive load. In this work, UIS test simulation was performed on multi-finger devices of various finger number and width at fixed value of inductive load. Devices with less number of fingers (tested till 8-fingers) fail due to current failure mechanism whereas temperature failure was observed in all cases of higher fingers, ranging from 16 to 100 fingers. It is also demonstrated that time in avalanche, t_{AV}, gets prolonged in multi-finger device design. As a result, self-heating is more resulting in temperature-failure in device with higher finger numbers. A linear relationship is shown between Energy in Avalanche, Single pulse (EAS) and device finger numbers or device width.

ACKNOWLEDGMENT

We are grateful to the National Center, Taiwan for supporting us with High-performance computing and National Science Council, through contract number NSC 100-2221-E-468-002 for supporting us. In addition, we would like to thank Vanguard International Semiconductor Corporation, Taiwan for their great support and helpful discussion.

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