On the design of 2-port SRAM memory cells using PNPN diodes for VLSI application

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Abstract—**A novel 2-port vertical PNPN diode memory cell expected to increase the SRAM integration density was proposed in this work. Its optimization design to meet the power consumption and the operational speed requirements in conventional VLSI applications were discussed. The memory cell was fabricated. Its static I-V curve and low-frequency write operations were tested. Based on the test results, high-frequency simulations were further conducted with Sentaurus TCAD tools. At last, a SRAM circuit using this new cell with a cross-point structure was proposed. The disturb modes in operations were analyzed and mixed-mode simulation was used upon this circuit. The mixed-mode simulation result proves that this circuit design is feasible in advanced VLSI applications.**

Keywords-SRAM; PNPN diode; TACD; cross-point

I. INTRODUCTION

SINCE the channel length has shrunk to 22 nm, the further scaling of MOSFET has become very difficult because of the short-channel effect (SCE) and the process variations [1][2]. The widely used SRAM cell, i. e. 6-T cell [3], consists of 6 MOSFETs. Not only the SCE and the process variations, but also the complicated layout of 6-T cell ($90-150F^2$) [4] have limited the increase of conventional SRAM integration density.

To reduce the memory cell area to increase the SRAM integration density further, several novel memory cells have been investigated, they are all based on the PNPN structure, such as the V-PCD [5], the 3-terminal gate-control PNPN cell [6], and the NDR-based SRAM cell [7]. Nevertheless, they were not put to practical use. The V-PCD cell has a structure of lateral design, so the cell area is still large. Moreover, a large number of excess charges are stored in the base regions (the center two layers of the PNPN structure are called base regions) when the memory cell is in "1" state, so the turn-off time is long, i. e. the write-0 speed is slow. Later on, the write-0 speed was increased in the 3-terminal gate-control PNPN cell and the NDR-based SRAM cell, but they both need a MOSFET to control the base-region charges, so the cell area can't be significantly reduced either.

In this work, a novel 2-port vertical PNPN diode memory cell was proposed. Its structure is shown in Figure 1(a). It is a silicon-based semiconductor device that has four layers with alternate doping types. This new memory cell has large potential for scaling: it isn't limited by SCE; it is fabricated using a simple process flow, therefore process variations can be potentially reduced; it has the smallest cell-layout ($4F^2$) [8].

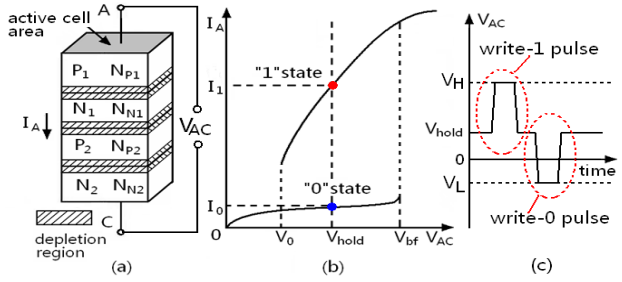

Figure.1 (a) the 2-port vertical PNPN diode memory cell, (b) the static I-V curve of the PNPN diode with latch-up effect and (c) the write operations of the memory cell.

Noted that the new memory cell only has 2 ports, we can introduce the cross-point structure [9] into the SRAM design. When the transistor-level 3-D integration technology [10] is still immature, the cross-point structure is seemed as the next generation memory array design that can achieve the highest integration density in the planar technology and have good potential to expand to 3-D integration. The adoption of the cross-point structure can increase the SRAM integration density further. Currently, 2-port memory cells like RRAM [11], PCM [9] have been investigated, their reported operation speeds are slow and their power consumptions are large, so they are not fit for SRAM application.

II. THE NOVEL MEMORY CELL

The static I-V curve of the PNPN diode is shown in Figure 1(b), which has been widely known as the latch-up effect [12] in CMOS technology. The memorization function is that: when V_{AC} is applied between V_0 and V_{bf}, there are two stable states for the leakage current that can be defined as "1" or "0" (I_1 or I_0 respectively), and "1" or "0" can be stably conserved once V_{AC} keeps constant.

As the PNPN diode is at "0" state, a positive voltage pulse is used between port A and port C to inject charges into N_1 and P_2 region (base regions), i. e. to latch-up the diode [13]. After the pulse is over for a period of time that depends on the device design, the diode gets into "1" state. As the PNPN diode is at "1" state, a negative voltage pulse is used to move the excess charges out of base regions, i .e. to switch-off the diode [13]. After the pulse is over for a period of time that depends

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on the device design, the diode gets into "0" state. Therefore, this PNPN diode is used as a binary memory cell.

A. *Memory cell design*

The common PNPN diode can't be directly used as a memory cell because of three problems: 1) I_1 is very high, which causes high power consumption in SRAM applications; 2) the time needed to write "1", i. e. write-1 delay, is so long that reduces the write-1 speed; 3) last but not the least, a large number of excess charges are stored in base regions when the memory cell is at "1" state, which increase the switch-off delay, i. e. reduce the write-0 speed. To make the original PNPN diode fit for the SRAM application, device design is required.

I_1 is directly proportional to the active cell area (active cell area definition is shown in Figure 1 (a)), so I_1 can be reduced by decreasing the active cell area. Write-1 delay can be reduced by increasing V_H or by decreasing V_{bf}. V_H is determined by peripheral circuits, reducing V_{bf} is mainly applied in this work. V_{bf} can be reduced by increasing doping densities ratio N_{P1}/N_{N1} or N_{N2}/N_{P2} [14]. Moreover, write-1 delay also decreases with the increase of V_{hold}. I_1 increases with the increase of V_{hold}, so optimizations are required between write-1 speed and power

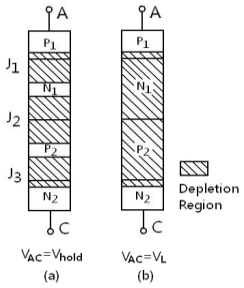

Fig. 2 The soft "punch-through" design is the design that the base regions are fully depleted when VAC = VL. It is used to optimize the write-0 speed.

consumption. To optimize the write-0 speed for ns range applications without increase the device complexity, the memory cell is designed to be at soft "punch-through" state [15][16], namely, both of the base regions are fully depleted when $V_{AC}= V_L$ (V_L is defined in Figure 1 (c)), as shown in Figure 2. Even though the soft "punch-through" effect is a terrible issue in the CMOS device, it is found to be beneficial to the high-frequency write-0 operation. The negative voltage pulse magnitude needed to induce the soft "punch-through" effect decreases with the shrinks of neutral regions. So the neutral-region widths can be reduced to decrease V_L. At the same time, the stability of storing "1" and process variations must be considered.

B. *Experiments for functional verifications*

The memory cells were fabricated with a small V_{bf} (the soft "punch-through" design wasn't introduced in the fabrication, it will be included in simulations in later sections). The fabrication process flow is simple, only few steps are needed to make this device, as shown in Figure 3 (a). The static I-V test of the fabricated cell is shown in Figure 4 (a). As the active cell area was scaled to 30 nm×30 nm, which is available with the state-of-the-art lithography technology [17], I_1 can be reduced to about 2 nA (V_{hold} is chosen to be 0.75 V for ns range operation), which meets the power consumption requirement.

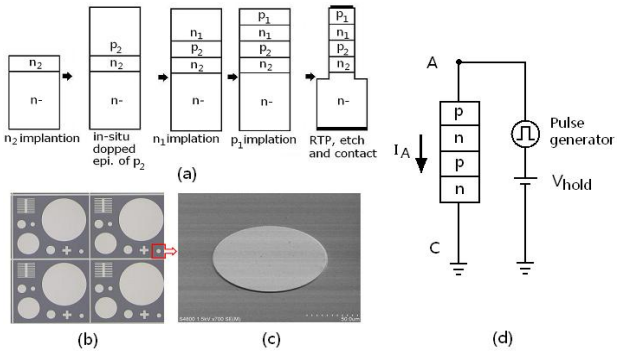

Fig. 3 (a) The process flow of the memory cell fabrication, (b) the top-down microscope view of the fabricated memory cells of different active areas, (c) the SEM bird's eye view of the 50 μm-radius memory cell and (d) the write-operation test circuit diagram.

Write-operation tests were further conducted, as shown in

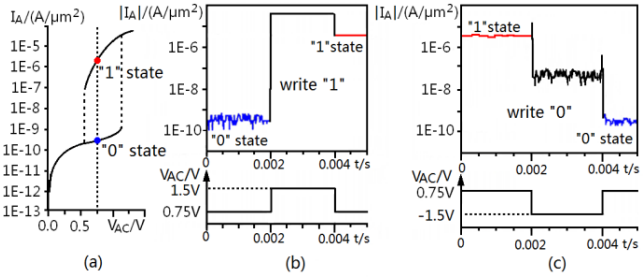

Fig. 4 (a) the tested static I-V curve of the fabricated memory cell, (b) the write-1 operation test result and (c) the write-0 operation test result.

Figure 4 (b) and (c). Although the fabricated memory cell was only tested at low frequency because of the test equipment limit, the test results indicate that the memory cell is functional feasible. Moreover, the experiments offered the datum for model-parameter calibrations in further high-frequency simulations.

C. *High-frequency simulations*

To study the high-frequency performances, simulations were applied. The memory cell with the optimized design was first created with Sentaurus Process simulation tool (cell area is 30 nm×30 nm) [18]. Then, Sentaurus Device simulation tool [18] was used upon this created cell (to achieve the accurate device simulation results, the device simulation model parameters had been calibrated according to the experimental

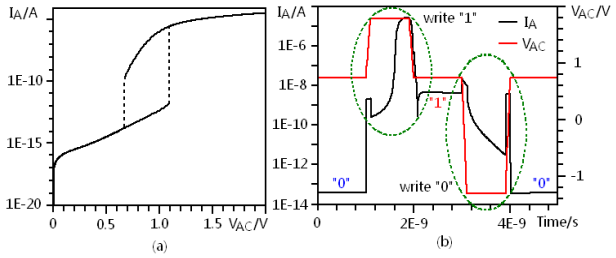

Fig. 5 (a) the static I-V curve simulation, the cell area is 30 nm×30 nm, (b) the simulation results of the write operations in ns range.

results). Its static I-V simulation result is shown in Figure 5 (a), and the write-operation simulation results are shown in Figure 5 (b), which indicates that the memory cell can be operated in ns range with available V_H and V_L.

III. THE SRAM CIRCUIT

A. The circuit design

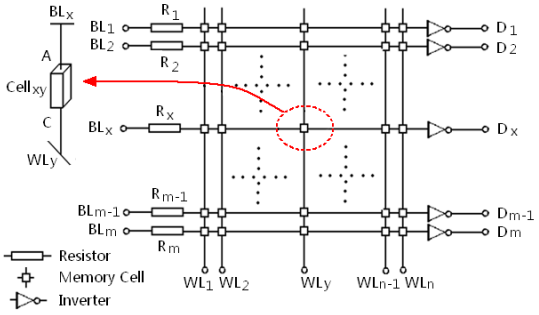

Fig. 6 the proposed SRAM circuit diagram with cross-point design.

The SRAM circuit using the 2-port vertical PNPN diode memory cell with cross-point structure was proposed, as shown in Figure 6. Inverters are used in peripheral circuits as sensing amplifier.

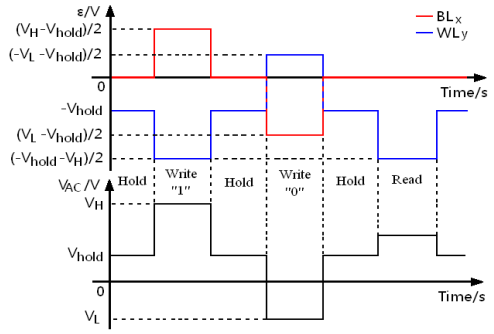

Fig. 7 the hold, write-1, write-0 and read operations of the SRAM.

B. The SRAM operations and disturb modes

1) Hold operation: The electric potential of BL_x is at 0 V and the electric potential of WL_y is at $-V_{hold}$, which is close to $V_{AC} = V_{hold}$ (ignoring the voltage drop on the resistor R_x). Once the potentials on BL_x and WL_y keep constant, "1" or "0" can be stably stored in $Cell_{xy}$. For hold operation, there is no voltage variations, so disturb modes don't exist.

2) Write "1" operation: In write-1 operation, to locate $Cell_{xy}$ that is selected to be written, the electric potentials on the bit line BL_x and the word line WL_y are both changed as shown in Figure 7. These electric potential changes are equivalent to the write-1 voltage waveform that we have discussed in previous section. In write-1 operation, cells linked with BL_x and WL_y are disturbed by half write-1 waveforms. For cells storing "0" states, they can't be latched-up with the half-write waveforms. If no latch-up exist, the base-region charge distributions can hardly be changed, so cells storing "0" get back to "0" state immediately when disturbs are over. For cells storing "1" state, they can be charged or discharged very fast due to the high current density level in the whole disturb process, so they can get back to "1" state almost without time delay when disturbs are over.

3) Write "0" operation: In write-0 operation, to locate $Cell_{xy}$ that is selected to be written, the electric potentials on the bit line BL_x and the word line WL_y are both changed as shown in Figure 7. These electric potential changes are equivalent to the write-0 voltage waveform that we have discussed. In write-0 operation, cells linked with BL_x and WL_y are disturbed by the half write-0 waveforms. For cells storing "0" states, they are immune to the half write-0 waveforms because there is no more state below "0". For cells storing "1" states, their base-region charges are partly moved out. When the disturbs are over, they get into an unstable state with low current density. In this case, the lost base-region charges can not be resupplied through I_As in a short time, so the disturbed cells can't get back to "1" in ns range. To solve this problem, aditional refresh waveforms are needed to help these cells to get back to "1" state, which will be shown in later mixed-mode simulation results.

4) Read operation: A negative voltage pulse with half write-1 magnitude is applied on WL_y to read, as shown in Figure 7. Under this bias, the draining currents flowing through 1-state cells on the row that linked with WL_y are driven to a high level (10μA), but for 0-state cells, draining currents can hardly increase due to the large resistance of the 0-state. With the resistor, a △V bettween "0" and "1" in read operation is achieved. For inverters with nanometer CMOS technology, a △V of 0.15V is large enough for the output voltage transformation.

C. The Mixed-mode simulation

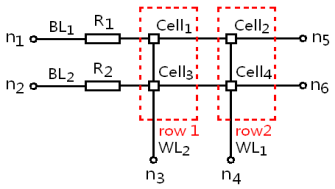

Fig. 8 the circuit diagram for the mixed-mode simulation with a 2×2 array

Mixed-mode simulation [18][19]was used upon this SRAM circuit structure with a 2×2 cell array (sensing amplifiers were not used in the simulation, n_5 and n_6 are directly used as the output nodes), as shown in Figure 8. Mixed-mode simulation enables circuit simulation using the physically-based models. It can link the devices created by process simulations into a SPICE circuit. It reduces the device molding time but needs large computational cost. The simulation result of the SRAM circuit is shown in Figure 9. The resistance of the resistors is 2×10^4 Ω in this circuit design, which brings a △V of 0.15V without obvious RC delay. Noted that $Cell_2$ and $Cell_3$ are both in "1" states, when write-0 operation is applied on $Cell_1$, the

original "1" states in $Cell_2$ and $Cell_3$ are disturbed. As talked in previous section, additional pulses name "refresh row 1" and "refresh row 2" are used to pull back $Cell_2$ and $Cell_3$ to "1" states. The mixed-mode simulation proves that this SRAM structure is functionally feasible and meets the speed requirement of VLSI applications.

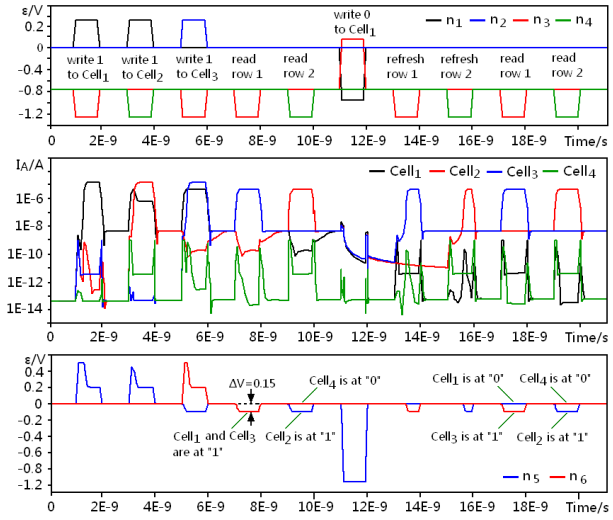

Fig. 9 the mixed-mode simulation of the 2×2 SRAM operations

IV. CONCLUSION

The tests of fabricated memory cell and device simulation results prove that the vertical PNPN-diode can be designed to be a SRAM memory cell. The new cell can offer high integration density, low power consumption and high operation speed. The mixed-mode simulation result proves that this SRAM circuit has good potential for the SRAM of next generation.

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