Multi-Via Electromigration Lifetime Model

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***Abstract*—In this paper, we propose a model and an algorithm for calculating currents in multi-via structures. We project the via array electromigration (EM) lifetime based on random via failure sequences, and demonstrate that the computed via array EM lifetime distribution model correlates well with experimental results.**

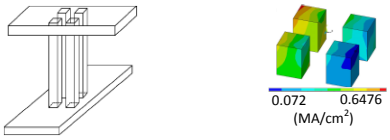
Keywords-electromigration; multi-via; uneven current distribution; failure sequence

I. INTRODUCTION

When electric current flows through a wire, moving electrons collide with metal atoms and cause a gradual ion movement. This current-flow-induced material transport is referred to as electromigration (EM) and is a major reliability concern for modern ICs. The International Technology Roadmap for Semiconductors (ITRS) [1] reports a rapid current density increase and wiring pitch decrease in sub-65nm technology nodes. Large currents are required to achieve better performance, and EM imposes a cap on wire current density. This trend indicates that satisfying EM reliability constraints poses a huge challenge.

In ICs, vias are very sensitive to EM degradation and most of the EM-caused defects are associated with vias or wire segments near vias. Therefore, multi-vias are commonly used in order to support greater current density; for example in the power/ground network. Although EM failure mechanism of a single via has been well studied, the failure characteristics of a via array are very different and analyzing them is non-trivial. There is a need to carefully study multi-vias to correctly project their lifetime and provide appropriate design guidelines.

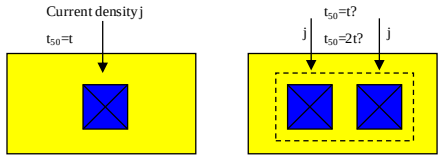
Currents in multi-vias connecting wires on different layers usually split unevenly. Although this effect had been observed before [3] and related EM violations have been reported [4], the uneven current split in multi-vias has not been widely noticed in practice due to two main reasons: 1) a lumped via model is typically used in electrical analysis; 2) EM test structures with multi-vias are often symmetric with equal currents flowing through them. However, in via arrays extracted from real circuits, currents indeed distribute unevenly and we also observe such behavior in ANSYS simulations of currents in multi-vias. In our experiments, we solve thermal-electric coupled Maxwell's and Joule heating equations using finite element method (FEM.) In Figure 1 (b), we show FEM simulation results for a 2 x 2 via array in Figure 1 (a), which is a typical regular array of evenly spaced vias connecting two orthogonal metal wires. No quantitative analysis of via array current distribution exists in literature, which motivates us to develop a model for fast calculation of currents flowing in individual vias and to explain the cause of the observed uneven current distribution.



(a) Structure (b) Simulation

Figure 1. FEM Structure and Simulation

Another important behavior of multi-vias is their redundancy which improves EM reliability. A simple example demonstrating this effect is shown in Figure 2 where a single via with current density *j* is compared to two vias each with the identical current density *j*.



(a) Single via (b) 1x2 via array

Figure 2. Single via vs. multi-vias

Assume that the mean time to failure (MTTF or t_{50}) is *t* for a single via with current density *j*. What would t_{50} be for the 1x2 via array? We answer this question in Section IV. We also show how via failure sequences and Monte Carlo approximations can be used to estimate the overall EM reliability of a via array.

II. UNEVEN CURRENT DISTRIBUTION IN VIA ARRAYS

A. Simulation Based Current Distribution

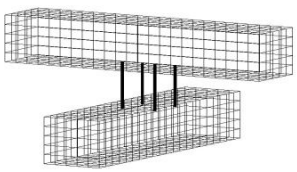


Figure 3. 3D grid model used in SPICE simulations

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We use FEM simulation to capture via array uneven current distribution. Our experiments include several cases of 4x4 arrays with different currents on top and bottom wires. From experimental results, we observe that there appears to be a linear dependency of via current on four wire currents. This motivates us to replace complex FEM analysis with a simpler model. An intuitive choice is to use a resistive SPICE mesh model. An example is shown in Figure 3, where each line segment represents a unit resistance.

This model mimics FEM but captures only resistive effects. We compared SPICE and FEM simulation results and they match well with a difference less then 1%.

B. *Fast Via Current Distribution Calculation*

Approximation methods for solving resistive networks can be much faster than SPICE without significant accuracy loss. Here, as an example, we use a 4x4 array composed of equal size vias uniformly spaced in horizontal and vertical directions. The current calculation method can be easily extended for any general *N* x *N* array.

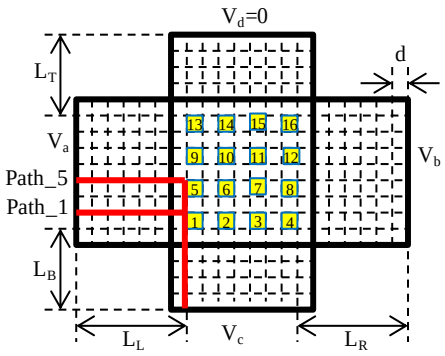


Figure 4. 4x4 via array

Consider two orthogonal wires on *metal 1* and *metal 2* connected through a 4x4 via array as in Figure 4. Vias are placed in the center of the wire intersection. The lengths of wires extending from the intersection area are L_T, L_B, L_L and L_R (assume $L_T = L_B$ and $L_L = L_R$) and their resistances are R_T, R_B, R_L and R_R. The unit length of mesh gird is d and resistance r. Voltages V_a, V_b, V_c and V_d are applied at the wire ends. V_d is set to be a reference voltage (V_d=0). Our objective is to compute current flowing through each via, given the wire dimensions, applied voltage, and via resistance R_{via}.

We solve the system three times and apply superposition. Each time only one voltage source is present and all others are shorted to ground. Due to symmetry of the system, when only V_a is applied, $I_{1\_a\_via}=I_{13\_a\_via}$, $I_{2\_a\_via}=I_{14\_a\_via}$, etc., where $I_{i\_a\_via}$ denotes the current flowing through via i when V_a is applied. The currents $I_{1\_a\_via}$, $I_{2\_a\_via}$, $I_{3\_a\_via}$ and $I_{4\_a\_via}$ are different due to the voltage gradient between the left and right ends of the horizontal wire. This is the forward voltage gradient of V_a. The currents $I_{1\_a\_via}$, $I_{5\_a\_via}$, are different due to the voltage gradient between left end of horizontal wire and bottom end of vertical wire. This is the lateral voltage gradient of V_a.

The forward gradient is defined as $f = V_{1a}/ V_{2a}$, where V_{ia} denotes voltage of via i top surface, when V_a is applied. We compute f using resistance divider shown in Figure 5. The values of R, R_{left}, R_{right} and R_1 can be extracted from the wire dimensions, grid branch resistance r and via positions. $R_{via}+R$ is the equivalent resistance from a via to ground and $R = R_B // R_T$.

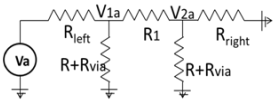


Figure 5. Equivalent circuit for computing forward gradient

For the configuration in Figure 5, we have

$$f = \frac{V_{1a}}{V_{2a}} = \frac{3r + R_R}{2r + R_R} = \frac{I_{1\_a\_via}}{I_{2\_a\_via}} \quad (1)$$

The lateral voltage gradient, defined as $l=V_{1a}/V_{5a}$ is computed using resistances approximated by shortest paths shown in Figure 4. There are two shortest length path_5 and path_1, and only one passes through via 5. Thus the resistance difference between path_5 and path_1 is $r/2$. Therefore, we have

$$l = \frac{V_{1a}}{V_{5a}} = \frac{R_{total\_path}}{R_{total\_path} - r/2} = \frac{R_L + R_B}{R_L + R_B - r/2} \quad (2)$$

For horizontal and vertical wire segments of unequal length, let $L_R=L_L+\Delta L_1$ and $L_B=L_T+\Delta L_2$; we can scale the wires such that horizontal and vertical segments are of equal length by replacing voltage V_b and V_c by

$$V_{b\_eq} = V_b \pm \frac{\rho \cdot \Delta L_1}{S_2} I_b, \quad V_{c\_eq} = V_c \pm \frac{\rho \cdot \Delta L_2}{S_1} I_c \quad (3)$$

In equation (3), S_i denotes the cross sectional area of a wire on metal layer i, ρ is the resistivity, I_b is the current in the right wire segment when V_b is applied, I_c is the current in the bottom wire segment when V_c is applied. The correcting terms have positive or negative signs depending on current directions.

Based on this analysis, we can express all via currents first in terms of $I_{1\_a\_via}$, and value of $I_{1\_a\_via}$ can be derived using forward and lateral voltage gradients. Experimental results for 4x4 arrays indicate that the maximal inaccuracy in computing via currents is less than 1% of the total current value. This error is contributed mostly by the inaccuracy of forward gradient computation. Our method can be extended to *N* x *N* via array by modifying equivalent circuit and shortest paths. We note that the analysis developed in this Section also provides an explanation why current distributes unevenly in multi-vias.

III. VIA ARRAY EM FAILURE

A. *Basic Assumptions*

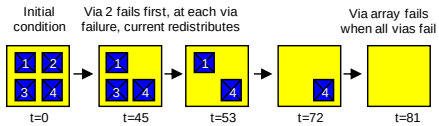


Figure 6. Sample via failure sequence

Via current distribution analysis serves as a basis for the multi-via lifetime projection. To enable complete analysis,

we assume that EM via failure manifests itself as a sudden significant jump in via resistance [2]. This assumption justifies a simple via failure cycle: a via fails, it is removed, current redistributes, then a new via fails. Figure 6 shows a sample via array failure sequence for a 2x2 via array.

B. Single Via EM Failure

Single via failure has been well studied. Variability in via failure time is due to the random microstructure of copper body/surface. The cumulative distribution function (CDF) of a single via failure is found to be well described by a lognormal distribution [5] (equation (4)) with two parameters: t_{50} and σ. t_{50} is the mean time to failure (MTTF), σ is a shape factor.

$$F(t;t_{50},\sigma)=\int_0^t \frac{1}{\sqrt{2\pi}\sigma t} e^{-(\ln t-\ln t_{50})^2/2\sigma^2} \quad (4)$$

In typical EM failure analysis, the t_{50} value is a function of current, whereas σ is assumed to be constant for a specific technology. Black's equation [6] is used to model the dependence of t_{50} on current density:

$$t_{50} = Aj^{-n} e^{\left(\frac{E_a}{kT}\right)} \quad (5)$$

In equation (5), A is an experimental constant, j is the current density, n is a scaling factor, E_a is the activation energy, k is Boltzmann constant, and T is the absolute temperature. In general, it is believed that for void nucleation n=2; for void growth n=1; and with Joule heating $n > 2$. Most of the EM failures involve both void nucleation and growth. In our work, we assume n=2. Typically in EM experiments $t_{50stress}$ and σ_{stress} are measured as reference MTTF and shape factor. With a reference $t_{50stress}$, other t_{50} values for different current densities can be easily determined, and σ is always equal to σ_{stress}.

C. Via Array EM Failure

The difficulty of projecting a via array lifetime distribution is that vias have memory of previous stress. Therefore, when and which via fails next depends on previous via failures. To model this we first define a via failure sequence V_f.

Definition: $V_f = [(t_1,k_1),(t_2,k_2),\ldots,(t_N,k_N)]$, is a sequence that records via failure time t and index k of a failing via; N is the total number of vias.

A sample via failure sequence in Figure 6 is [(45,2), (53,3), (72,4), (81,1)]. The time and via index are random numbers, therefore, theoretically we need to traverse all possible failure sequences and compute distributions for all t and k. This is impractical due to exponential search space implied. Our goal is to determine only the distribution of the *last* via failure time t_N and the intermediate distributions are of no interest. We use a Monte Carlo approximation to sample intermediate t and k instead of considering all possible values. In this way, as long as the previous via failure sequence is determined, the next via failure time and index number are easy to calculate. This method has a linear complexity on N.

Knowing the previous via failure sequence, stress time translation is used to account for the memory effect. The translation rule is given by equation (6).

$$\left(\frac{i_{m-1}}{i_m}\right)^n = \frac{t_{m-1}'}{t_{m-1}} \quad (6)$$

In equation (6), n is the same exponent in equation (5) (n=2 in our analysis); i_{m-1} and i_m are previous and present currents through a via; t_{m-1} is the previous via failure time; t_{m-1}' is the translated stress time. For example, in Figure 6, assume via *3* carries current of density 10mA/μm^2 from t=0 to 45s, and after via *2* fails, it carries current of density 15mA/μm^2. The stress of 10mA/μm^2 for 45s can be translated to an equivalent stress of 15mA/μm^2 for 20s.

Now, given the condition that via *3* does not fail under 15mA/μm2 for 20s, the conditional CDF of via *3* is given by equation (7), where k is the via index, in this particular case, k=3 and t_{m-1}'=20s.

$$F_k'(t) = \frac{F_k(t+t_{m-1}') - F_k(t_{m-1}')}{1-F_k(t_{m-1}')} \quad (7)$$

Since vias are connected in parallel, the weakest via is the next one to fail. The conditional via failure CDF is then combined to determine the next via using equation (8), and the probability of next via failure to be via k is given by equation (9).

$$F_{next}(t) = 1-\prod_{k\in V_g}(1-F_k'(t-t_{m-1})) \quad (8)$$

$$P_{next=k} = \int_{t=0}^{\infty}\left[f_k'(t)\cdot\prod_{l\neq k, l\in V_g}(1-F_l'(t))\right]dt \quad (9)$$

V_g denotes the set of vias that are still conducting and $f_k'(t)$ is the probability density function (PDF) for $F_k'(t)$. With the above equations, a Monte Carlo approximation can sample t and k accordingly at each via failure step and generate the via failure sequence. The averaged results from multiple Monte Carlo runs are used to approximate the overall via array CDF.

IV. Experiemental Results

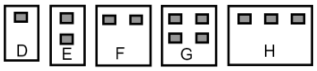


Figure 7. Via array layout

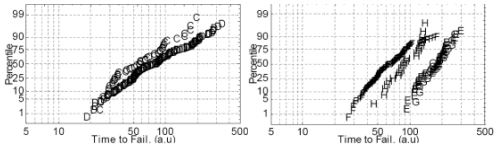


Figure 8. Via array EM failure test restults [2]

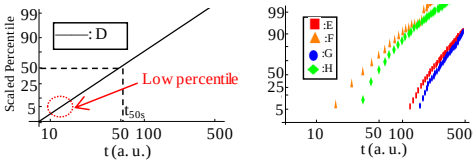
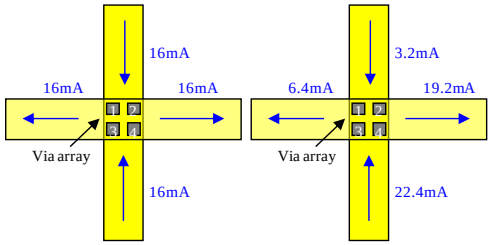


Figure 9. Via array EM failure analysis results

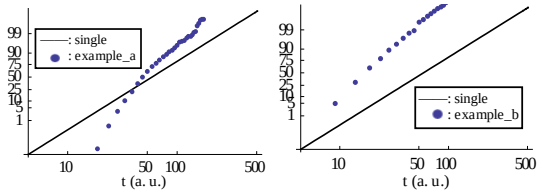
We now apply our analysis on typical via arrays. In reference [2], measured results are reported for several via arrays shown in Figure 7. The nominal via size is 0.14μm x 0.14μm and the wire thickness is 0.19μm. Test stress at 300℃ is under 25mA/μm^2. Figure 8 shows EM test results from [2]; Figure 9 shows projections computed using our method.

The overall EM failure distribution characteristics obtained from the stress tests and analyses are very similar. Note that case D is a single via, therefore a simple straight line analytical solution can be derived. The low percentile part is of more interest for reliability. Solutions for other cases are from Monte Carlo approximation. We observe that for some cases (such as F) t_{50} can be smaller than for the single via case, however because of a small σ, the lower percentile reliability for case F still wins. Note that case F configuration is the same as that in Figure 2(b).



(a) even current distribution (b) uneven current distribution

Figure 10. 4x4 multi-via test examples



(a) CDF for case (a) (b) CDF for case (b)

Figure 11. CDF comparison

Our analysis is also applied to some power grid via array structures constructed based on the IBM power grid benchmarks [7], with current values corresponding to benchmark solutions. To generate the vias we use the following additional industrial geometric parameters: wire thickness is 0.6μm, wire width is 2μm, via size is 0.8μm x 0.8μm. We assume 10mA/μm^2 is the EM current limit for a reference single via with t_{50ref}. We consider two cases shown in Figure 10: case (a) all wires carry the same current of 16mA, leading to evenly distributed via currents; case (b) the wires carry unequal currents of 3.2mA, 6.4mA, 19.2mA and 22.4mA thus the via array has highly uneven current distribution. The total current passing through the via array is 25.6mA.

Traditional EM rules assume an even current distribution, so for case (a), the current through each via is computed as 10.25mA/μm^2, which indicates a violation of the EM current limit. For case (b), the current through each via is 10mA/μm^2, which is within the EM current limit. However, the via array EM reliability cannot be determined based on just the average currents. It requires that uneven current distribution and multi-via redundancy effects are considered jointly. The initial via current distribution for case (b) are calculated to be 7.36mA/μm^2, 10.08mA/μm^2, 10.24mA/μm^2 and 12.32mA/μm^2 using the model from Section II. In Figure 11, the via array lifetime distributions for cases (a) and (b) are plotted against the reference of a single via lifetime.

The results are counter-intuitive and do not agree with the traditional EM reliability evaluation. For case (a), t_{50} is close to t_{50ref}, and the small σ makes it an EM reliable design at lower failure percentiles. On the other hand, for case (b), t_{50} is obviously worse than t_{50ref}. For lower percentiles it appears better than the reference single via due to a relatively small σ, but it is very close to the reliability boundary and should be considered EM-unsafe. These two examples contradict common belief and demonstrate a need for a proper method to evaluate multi-via EM reliability as discussed in this paper.

V. Conclusions

Multi-vias are widely used to connect wires from different layers to improve EM reliability, but no detailed via array lifetime evaluation methods exist. In this paper, we demonstrate that current distributes unevenly in multi-vias and explain why. We develop a fast model to calculate currents flowing through individual vias, and propose a step-by-step multi-via failure model. Each time a via fails, current redistribution is calculated and the via memory effect is accounted for using stress time translation. We apply a Monte Carlo approximation to generate via failure sequences and the overall via array lifetime distribution. Experimental results show that our predicted lifetimes correlate well with EM stress test results. For multi-vias, both the redundancy effects and uneven current distributions affect reliability, leading to counter-intuitive results in real circuits when the unevenness of current distribution is high.

Acknowledgment

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