RTS Amplitude Distribution in 20nm SOI FinFETs subject to Statistical Variability

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Abstract—**We presents a comprehensive simulation study of random telegraph signal (RTS) amplitude distributions under the influence of statistical variability in 20nm gate-length, lightly-doped channel FinFETs on an SOI substrate. The distribution of threshold voltage RTS shifts, due to single-charge trapping at the interface, is inherently affected by statistical variability sources including random discrete dopants (RDD), gate- and fin- edge roughness (GER and FER), and metal gate granularity (MGG). The threshold voltage RTS amplitudes in SOI FinFETs deviate from an exponential distribution with a reduced tail, but it increases with increased statistical variability. Moreover, the electrical transfer characteristics due to single charge trapping vary with gate-bias.**

Keywords- FinFET; RTS; threshold voltage; variability

I. INTRODUCTION

FinFETs with 3D architecture are being introduced at the 22nm technology generation in response to requirements for better electrostatic integrity and reduced statistical variability [1]. Previously, comprehensive studies on statistical variability in FinFETs on SOI substrate have been presented, for which the time-zero variability is significantly reduced, mainly due to the FinFET's tolerance of ultra-low channel doping [2]. However, spatially random interface charge trapping in progressive N/PBTI degradation increases the transistor's parameter variations. In [3], we have shown that the random telegraph signal (RTS) amplitude is dependent on the charge trapping position and complex current density distribution in the fin channel, and is affected by statistical variability. However, a comprehensive study of statistical reliability in the presence of the inherent statistical variability in nanoscale FinFETs is still lacking. This paper presents a systematic study showing that the RTS amplitude distribution inherently depends on the statistical variability sources. This is a starting point in the understanding of the BTI behaviour of contemporary FinFETs, which is a manifestation of multiple charge trappings.

II. SOI FINFET AND SIMULATION METHOD

The 'template' SOI n-channel FinFETs used in this study feature a 20nm gate length, fin height/width ratio of 25/10nm, and high-k/TiN metal gate stack, with device parameters listed in TABLE I. A low channel doping of 1×10^{15} cm^{-3} is assumed, and the source/drain extension doping follows a Gaussian profile, shown in Figure 1. In addition, alternative channel dopings of 1×10^{17} and 5×10^{17} cm^{-3} are studied for comparison.

TABLE I. 20NM SOI FINFET PARAMETERS

Lg (nm)	20
EOT (nm)	0.83
Hfin/Wfin (nm)	25/10
Vdd (V)	1.0
Idsat (mA/μm)	1.411
Ioff (nA/μm)	97
SS (mV/dec)	76.8
DIBL (mV/V)	46.7

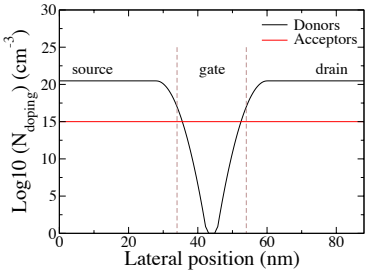

Figure 1 The doping profiles along the channel of the nFinFET.

On such a small nanometre scale, the quantum confinement effects of the four-sided oxide barrier of the fin-channel are significant. Moreover the discrete dopants and trapped charges create coulomb potential wells and peaks. Density gradient quantum corrections are essential when employing the drift-diffusion simulations in the presence of discrete charges. The GSS "atomistic" simulator Garand is used in this study [4] allowing for large-scale cluster-based numerical simulations. The FinFET is strained to improve mobility. The spacer and source/drain extension are optimised. The Id-Vg characteristics are illustrated in Figure 2 achieving the performance prescribed by the ITRS.

Random discrete dopants (RDD) are included in the 'atomistic' simulations although their effect is greatly reduced due to the low channel doping. Gate line edge roughness (GER) practically exists in all types of transistors. The fin edge roughness (FER) is a new variability source in FinFETs.

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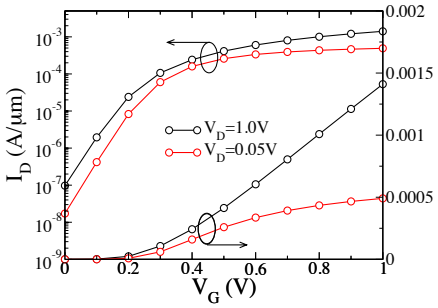


Figure 2 The Id-Vg characteristics of the 'uniform' SOI nFinFET.

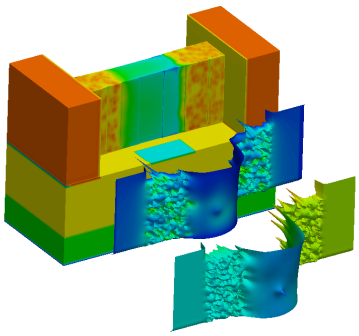


Figure 3 One sample of an 'atomistic' channel FinFET subject to statistical variability sources including RDD, GER, FER and MGG, with a charge trapped at the sidewall interface of narrowed fin, and under a TiN metal-grain with low work-function [3].

Compared to variations of fin-width, fin-height and fin-shape in bulk FinFETs, in this study FER leads to the variation of fin-width in SOI FinFETs. LER is parameterized using correlation length of 30nm and varying RMS. The possible metal gate granularity (MGG) formed by the thermal process in gate-first high-k/metal gate stacks is included in the simulations for completeness of this study. Ensembles of 1000 samples with/without average trap charge density of 1×10^{11}cm^{-2} subject to RDD, GER, FER, and MGG are simulated using Garand, and around 375 pairs of transistors with/without a single trapped charge are selected.

Figure 3 illustrates the 3D electron density variation in one "atomistic" n-channel FinFET on an SOI substrate. In addition the front slice shows the potential and the middle slice shows the current density. In this figure a trapped charge is located at the sidewall interface of a narrowing region of the fin, and is under a TiN metal grain with lower work-function compared to other metal grains in the width direction.

III. RTS Amplitude Distribution

It has been previously reported that the threshold voltage RTS-amplitude distribution is exponential, and the large threshold voltage shift (ΔV_T) at the tail is created by the interaction of trapped charges with the underlying random dopants in traditional bulk MOSFETs [5][6]. When channel dopants are removed in FinFETs, the other statistical variability sources such as FER and MGG will become prominent, and the random interface trapped charges accumulate with progressive N/PBTI degradation and will increase the time-dependent variability. In this section, the interaction of trapped charge with the major statistical variability sources, including RDD, FER, GER and MGG, is examined respectively.

A. FER and GER

The complicated current density distribution in the fin-channel depends on the oxide-barrier, fin-geometry, bias conditions, and the trapped charge located near the high current path can cause a large RTS threshold voltage shift [3]. The complementary cumulative density function (CCDF) of V_T RTS amplitude has been examined. The CCDF of V_T RTS amplitude in bulk transistors has well documented exponential behaviour. Four different RMS amplitudes are simulated to investigate LER effects, especially FER effects on RTS amplitude in SOI FinFETs. Shown in Figure 4 the RTS V_T shift distribution deviates from exponential profile in the tail, but large threshold-voltage shifts start to appear in the 'atomistic' FinFET with larger LER amplitude. Larger LER can extend the bounded tail to larger values. One FinFET with the largest RTS V_T-shift has been examined closely. Figure 5 illustrates the fin thickness variation in this device and a charge is accidentally trapped at a sidewall interface of the narrowing region at the source side of channel. With the large current flows through this narrowed region the trapping-induced coulomb peak can cause large current reduction in subthreshold, leading to large V_T-shifts. In the figure, the current flow bypasses the trapped charge and becomes strongly depressed in its vicinity. Similar situation is also illustrated in Figure 3. Therefore, regions with fin narrowing due to FER are more sensitive to interface trapping.

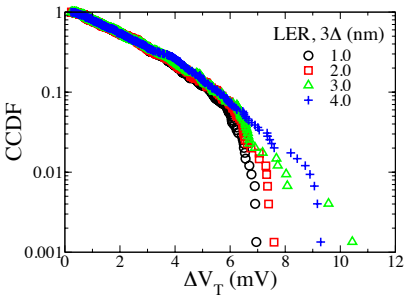


Figure 4 The distribution of threshold-voltage RTS amplitudes in the presence of gate-LER and fin-LER. Rougher gate- and fin-edges increase the V_T shift due to single trapping.

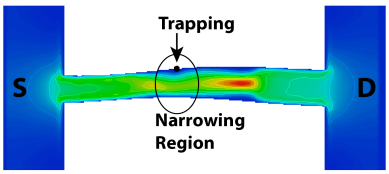


Figure 5 The top-view of current density inside the fin of the extreme device in Figure 4. Trapping occurs at the sidewall interface of a narrowed fin which significantly changes and reduces the current flow in the narrow region.

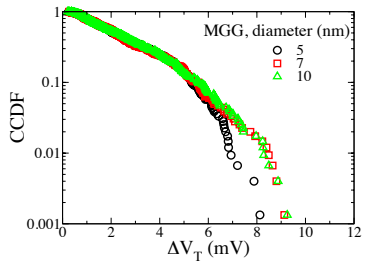


Figure 6 The distribution of threshold voltage RTS amplitudes in the presence of MGG-induced work-function variation. Larger metal grains lead to a larger spread in the RTS distribution.

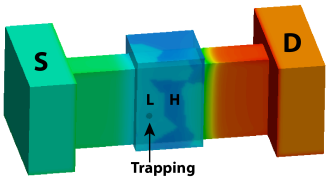


Figure 7 The 3D view of potential of the extreme case in Figure 6. The trapping occurs at the source side of channel barrier at high drian-bias, where is modulated by local work function variation. Vd=1.0V.

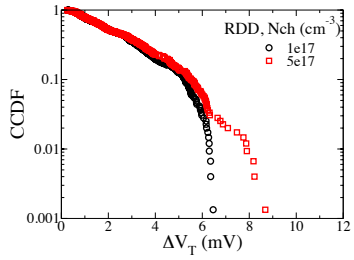


Figure 8 The distribution of threshold voltage RTS amplitudes in the presence of random dopants. With increasing channel doping the RTS amplitude distribution tail extends.

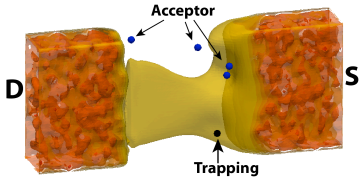


Figure 9 The contour of electron density inside the fin of the extreme case in Figure 8. Four ionised acceptors located, in this case, inside the upper fin-channel block the current here, creating a bottom percolation where a charge is trapped at the sidewall.

B. MGG

Work function variation due to metal gate granularity gives rise to surface potential fluctuations in the channel. Along the width direction, a low channel-barrier region always has higher current density. The local low work-function region in n-FinFETs corresponds to a low barrier. In Figure 6 the CCDFs of ΔV_T are examined in respect of an exponential distribution. The increase in the metal grain average diameter from 5nm to 7nm extends the distribution tail, although the increase saturates from 7nm to 10nm. With less self-average in larger metal grain gate, a charge trapping happening in a larger area of local low channel-barrier region can reduce more efficiently the current. Therefore transistors with larger metal-gate grains have larger V_T shifts in the distribution tail. The extreme case with the largest V_T-shift in Figure 6 is illustrated in Figure 7. The charge is trapped under a metal grain with low work-function above the fin at the source-side. Although a metal grain with high work-function is located in the same channel-direction as the trapped charge at the drain-side, at high drain-bias the drain-side channel potential barrier is largely lowered by DIBL. The source-side potential barrier is critical at high drain bias.

C. RDD

Unlike bulk conventional transistors, the channel doping is greatly reduced in the SOI FinFETs, and current flows in the middle of fin in the subthreshold regime. Although rare, statistically possible random dopants located in the middle of fin can cause large current reduction. Figure 8 shows the extension of the V_T RTS amplitude distribution in the presence of elevated channel doping. With increased channel doping, there is more chance for FinFETs to have dopants located inside the middle of channel, leading to larger V_T. Figure 9 demonstrates what happens in the extreme V_T shift case from Figure 8. Four acceptors in the upper part of the fin limit the current flow, creating high density current path at the bottom of the fin. The trapping happening at this critical path, leads to a large V_T-shift.

D. Statistical Variability Dependence

The V_T RTS amplitude dependence on statistical variability is examined. The average V_T RTS amplitude illustrated in Figure 10 increases with the increase in the statistical variability magnitude in the corresponding fresh/virgin devices. While increasing statistical variability magnitude from LER and MGG can give rise to an increase in the average RTS amplitude, the increase of RDD-induced statistical variability leads to the largest increase of average V_T RTS amplitude. Moreover, stronger dependence of the standard deviation of ΔV_T is observed in Figure 11. Therefore, V_T RTS amplitude inherently depends on statistical variability magnitude and statistical variability sources.

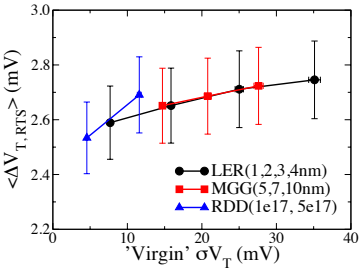


Figure 10 The dependence of average single-trapping V_T-shift. The devices with larger V_T variation seem to have larger average V_T RTS amplitude.

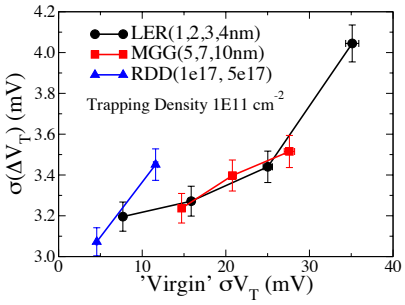
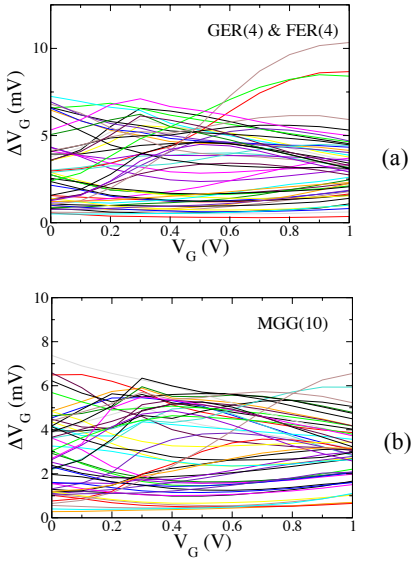


Figure 11 The dependence of standard deviation of V_T shift on the "virgin" device variability, in the average interface trapping density of 1×10^{11} cm^{-2}.

IV. Impact on Transfer Characteristics

The gate voltage shift, ΔV_G, required to produce the same drain current in the presence of trapped charge as the current in a fresh transistor, is also examined in Figure 12 for several particular variability sources with large variability. At different gate biases the compensational ΔV_G fluctuates in magnitude, and with locally increasing or decreasing trends. This indicates the challenge for compact models in taking into account the impact of the individual charge trapping. Figure 13 illustrates the ΔV_G distribution at the I_{ON} gate voltage. The distributions show a trend change at ~3mV which is the average ΔV_G. The rest of the distribution tail diverges depending on the statistical variability sources.



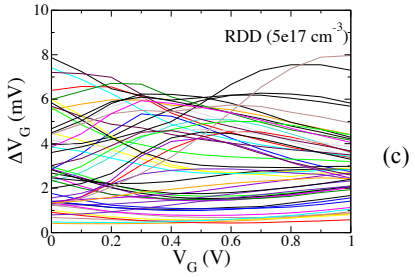


Figure 12 The fractional gate-voltage characteristics in the single-charge trapped devices subject to gate and fin LER with 3Δ of 4nm (a), MGG with average grain diameter of 10nm (b), RDD with channel doping 5×10^{17}cm^{-3} (c).

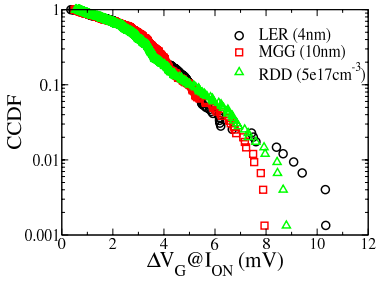


Figure 13 The compensation gate voltage distributions (at Ion) in the single-trapped-charge "atomistic" devices subject to different variability sources.

V. Conclusions

This paper presents a comprehensive simulation study of threshold voltage RTS amplitude distribution in the presence of different statistical variability in SOI FinFETs. The statistical variability induced by FER, GER, MGG and RDD can extend the RTS distribution tail increasing the RTS amplitude and its variation. In addition, the charge trapping can greatly alter the shape of the transfer characteristics depending on the gate bias.

References

[1] C. Auth, C. Allen, A. Blattner, et al., "A 22nm High Performance and Low-Power CMOS Technology Featuring Fully-Depleted Tri-Gate Transistors, Self-Aligned Contacts and High Density MIM Capacitors," in *VLSI Tech. Dig.*, 2012, pp.131-132.

[2] X. Wang, A.R. Brown, B. Cheng, and A. Asenov, "Statistical variability and reliability in nanoscale FinFETs," in *IEDM Tech. Dig.*, 2011, pp.5.4.1–5.4.4.

[3] X. Wang, A.R. Brown, B. Cheng, and A. Asenov, "Statistical distribution of RTS amplitudes in 20nm SOI FinFETs," in *Proc. Silicon Nanoelectronics Workshop*, 2012, pp.77-78.

[4] Garand, [online] http://www.goldstandardsimulations.com/

[5] B. Kaczer, et al., "Statistics of multiple trapped charges in the gate oxide of deeply scaled MOSFET devices—application to NBTI," *IEEE Elec. Dev. Lett.*, Vol.31, no.5, May 2010, pp. 411-413.

[6] J. Franco, et al., "Impact of single charged gate oxide defects on the performance and scaling of nanoscaled FETs," in *Proc. IRPS*, 2012, pp.5A.4.1-5A.4.6.