On the nonlocal modeling of tunnel-FETs

Device and Compact models

Koichi Fukuda, Takahiro Mori, Wataru Mizubayashi, Yukinori Morita,
Akihito Tanabe, Meishoku Masahara, Tetsuji Yasuda, Shinji Migita, and Hiroyuki Ota
Collaborative Research Team Green Nanoelectronics Center (GNC),
National Institute of Advanced Industrial Science and Technology (AIST)
Ibaraki, Japan

Abstract—**Based on a nonlocal band to band tunneling model, consistent device and compact models for tunnel-FETs are developed. For the device model, several new physical aspects such as volume effects are incorporated into the nonlocal model, and it shows good agreement with our measurements. For the compact model, nonlocal aspects of band to band tunneling phenomena are successfully incorporated by adopting simple assumption in source-gate overlap potential. Consequently, the new model becomes a powerful physics-based tool for active usage in developing tunnel-FETs.**

Keywords-tunnel FET; compact model; TCAD; nonlocal; band to band tunneling

I. INTRODUCTION

To realize ultimate low power LSI's, sub-threshold slope is one of the limitations of conventional CMOS devices, which is restricted to higher than 60(mV/decade) at room temperature even by advanced tri-gate approaches. To overcome this limitation, the tunnel-FET (TFET) has emerged as most promising candidate alternative to CMOS because of its steeper sub-threshold slope. To reach required and ideal TFET performances, many types of TFETs, using different materials and device structures, have already been proposed by many groups, using not only device fabrications but also TCAD simulation approaches. Since TFETs actively use the band to band tunneling (BTBT), improvement of its physical model in device simulation is highly required, compared with the model quality used in conventional CMOS GIDL analyses. Furthermore, a compact model with physics-based model is urgently required to study pros and cons of using TFETs in circuit design, including impacts of their source-drain asymmetric characteristics.

In this paper, assumptions behind nonlocal band to band tunneling model in device simulation are re-examined, including tunnel path estimations, volume effects, tracing directions and so on. Influences from these assumptions are discussed, and consequently some advancements of the nonlocal BTBT model are achieved. Compact modeling of TFETs is a difficult challenge because of the nonlocal aspects of BTBT phenomena. We also tackled to expand nonlocal BTBT model to an analytical compact model, by introducing approximated formula of vertical and lateral potential profiles around source gate overlap regions.

II. DEVICE MODELING

Semiconductor device simulation is a powerful tool especially for new concept devices such as TFETs. Based on semiconductor device equations and macroscopic physical model, precise microscopic physics in the new devices is numerically solved multi-dimensionally. It is used to find new device ideas, to understand device behaviors, to optimize the devices, to develop new analytical device models for circuit simulation of the new devices. On the other hand, the assumptions of basic equations and physical models used in the device simulation are critical for their predictions.

For the device simulation of TFETs, the present approach is based on nonlocal BTBT model, in which conduction band and valence band are multi-dimensionally traced to get tunnel paths and tunnel lengths as one-dimensionally explained in Fig.1. The nonlocal electric field *Enonl* defined as averaged electric field along the traced tunnel path, is used in famous Keldysh and Kane's formula of BTBT generation rates. This approach enables analyses of devices even with band modulation such as TFETs with semiconductor hetero junctions [1].

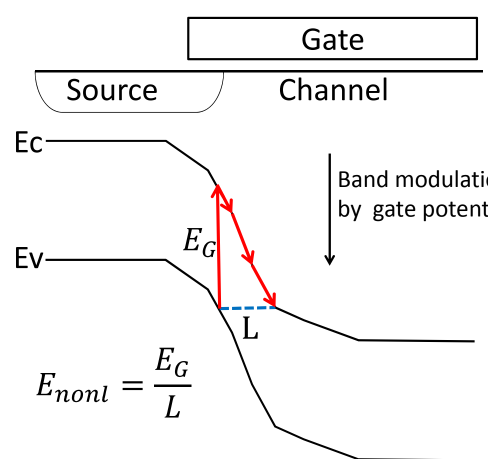

Figure 1. Concept of our nonlocal electric field using band diagrams, together with a TFET schematic view. Tunnel length *L* is determined by tracing conduction band *Ec* and valence band *Ev* to find the same energy levels. The nonlocal electric field *Enonl* is defined by averaged field through the tunnel path.

ISBN 978-0-615-71756-2

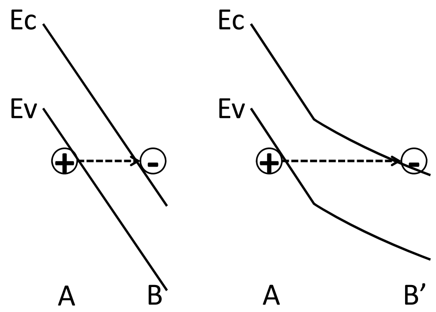

Figure 2. Differences of BTBT in constant electric field (left) and rapidly changing electric field (right) expressed in 1-dimensional. Valence band electrons at position *A* tunnel to position *B* or *B’*.

BTBT in one dimensional view is shown in Fig.2. In constant electric field, valence electrons tunnel from position *A* to *B*, and the tunnel distance can be easily obtained by electric field. In case of rapidly changing electric field, the electrons tunnel from *A* to *B’* and the tunnel distance is not obtained by local electric field. In the realistic devices, there are multi-dimensional effects of BTBT paths. In TFETs, BTBT occurs mainly at source gate overlap regions, where electric field is strongly bended by source, drain and gate voltages. This is the reason why we need nonlocal approaches of BTBT modeling.

Based on this concept, several advancements are implemented and tested, such as,

a) *using short-cut tunnel distance instead of accumulated distance,*

b) *generating electrons and holes at individual points,*

c) *tracing in the reverse direction.*

As summarized in Fig.3, *b)* (generation position) is not so critical for TFETs without hetero junctions, but *a)* (tunnel distance) and *c)* (trace direction) cause critical differences. To solve the trace direction dependencies, volume effects are newly considered, and differences caused by trace directions have been eliminated.

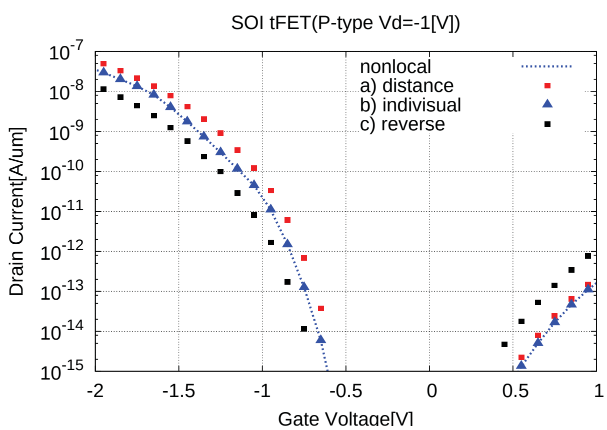

Figure 3. Some advanced options of nonlocal BTBT implementations. Especially the tunnel direction dependence is artificial, and should be eliminated by introducing volume effects consideration.

The concept of the volume effects of BTBT in this work is schematically shown in Fig.4. As shown by arrows in the figure, tunnel directions in devices are not essentially parallel since they depend on electric field which is not isotropic in devices. Gathering and spreading effects of BTBT in devices differently affect the tunnel generation rates through integrated density of states (DOS) at both tunnel start and end points.

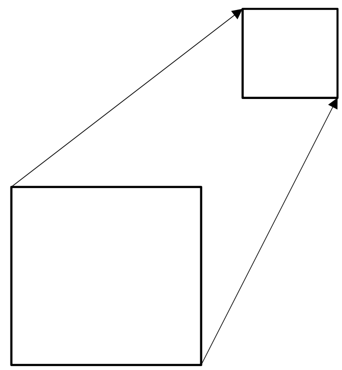

Figure 4. Concept of BTBT volume effects considered in the present model. Tunnel directions are not essentially isotropic, which affects the BTBT geration rates through integrated density of states.

The new model shows sufficient accuracy for our TFET measurements with two different gate stacks [2] [3] as shown in Fig.5. Results calculated by local BTBT model which uses local electric field to calculate tunnel distances, are also compared. It is clearly shown that the local model overestimates BTBT currents several orders of magnitude. As is widely known, that conventional local BTBT model is inadequate for TFET device simulations. On the other hand, the present nonlocal BTBT model shows good agreement with measured *Id-Vg* curves, without re-fitting of BTBT model parameters. This ensures that the TFET characteristics are well explained by tunnel distances.

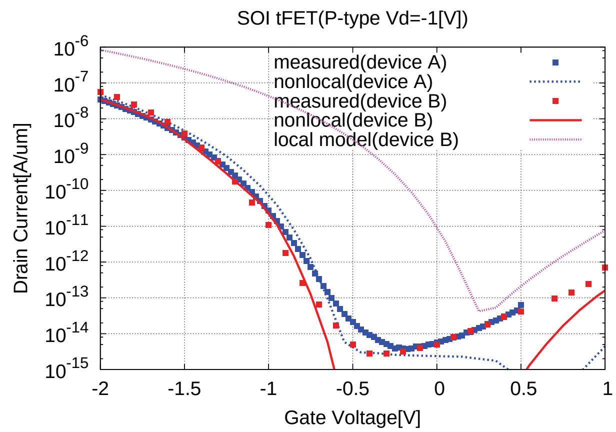

Figure 5. Comparisons of simulation results of the present model (lines) and measured *I-V* curves (markers). Simulation results using local BTBT model are also compared.

Generation rates at *Vgs=-1V* calculated with the local and the nonlocal models are compared in Fig.6 a) and b) respectively. The local model critically overestimates BTBT generation rates at the surface of source to gate overlap region as in Fig.6 a). This error is arising from the fact that strong vertical electric field exists at the source surface of gate overlapped region which does not fulfill the enough energy differences to cause the tunneling. As shown in Fig.6 b), main contribution to BTBT current is not from the overlapped surface for this sub-threshold condition, but from deeper area, where sufficient energy difference for BTBT generation is fulfilled in the depletion region.

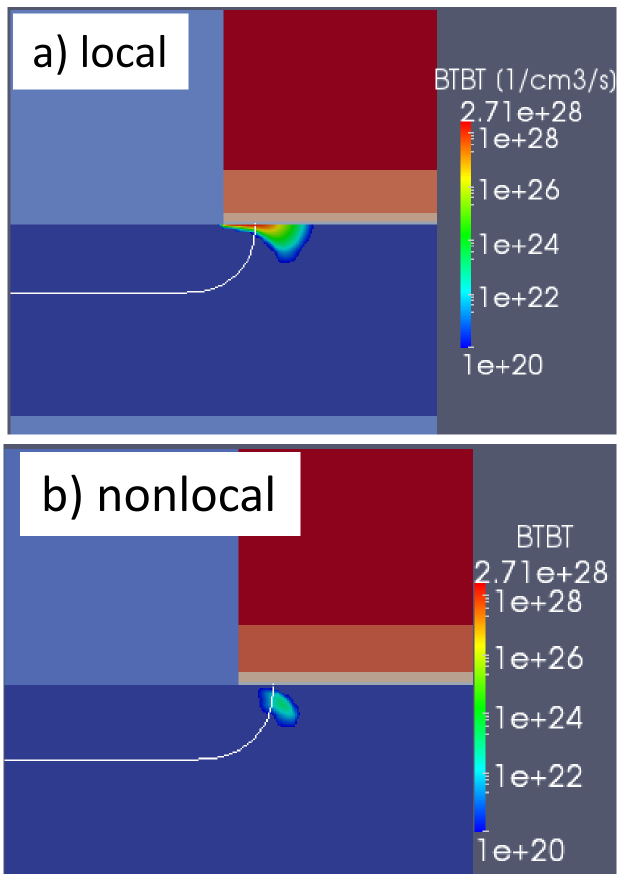

Figure 6. BTBT generation rates at *Vds=Vgs=-1V* calculated by a) the local model (upper), and by b) the nonlocal model (lower). The local model overestimates generation rates by several orders, especially at the surface of source to gate overlap region.

Key aspects of the present model have already been implemented to TCAD system HyENEXSS [4] to study TFETs of detailed device structures such as FinFET-type or nanowire-type in both 2D and 3D. More CPU time is required compared with the local BTBT model, and some speed enhancement efforts have been made.

III. Compact Modeling

To inplement main aspects of the nonlocal BTBT model to compact model, following assumptions are introduced.

1) Direction of tunneling is assumed mainly to be vertical to MIS-interface, and additional contribution of lateral electric field is incorporated. This approach enables compact model to incorporate the nonlocal effects.

2) The lateral electric fields around BTBT regions are calculated by simple capacitance model between source and gate. Created potential profile along the MIS interface agrees well with potential profiles calculated by device simulations.

Concerning the above assumption 2), potential profiles along MIS interface assumed in this approach are compared to TCAD results in Fig.7 for a drain to source voltage *Vds* of 2V, and for several gate to source voltages *Vgs*. Despite the simplicity of the assumptions, main features of the potential profiles depending on bias conditions are well explained. Since our potential profile function is expressed in simple analytical formula, lateral electric field can be directly calculated without numerical iterations.

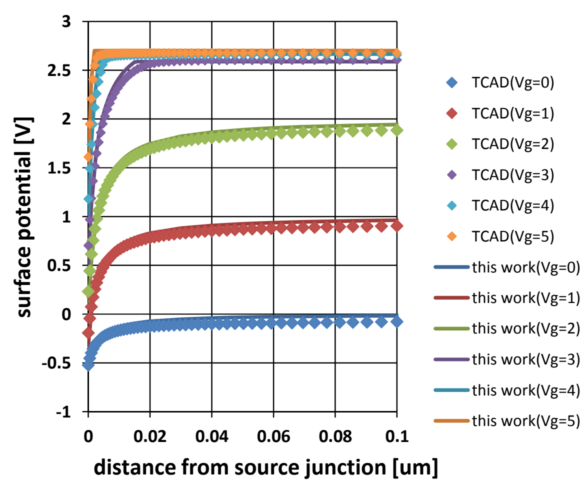

Figure 7. Assumulated surface potential in the compact model compared with TCAD for various gate bias *Vg*.

Major model parameters used in the present model are summarized in Table I. Number of parameters is restricted to be minimum, and all parameters correspond to physical device parameters. Because of these physics based parameters, the present compact model could be used as mini-TCAD to study device performances depending on each device parameters. It is enough to study various problems which may occur in TFET circuits, including their statistical problems. To consider gate induced drain leakage (GIDL) arising also from BTBT phenomena, a few more similar parameters are introduced, not described in Table I. The model assumes potential profile at the surface of the drain gate overlap region, in analogy to the source side.

TABLE I. MAJOR PARAMETERS OF THE COMPACT MODEL.

Parameters	**Descriptions**		
	unit	***typical***	***Explanation***
NSOURCE	$1/m^3$	$2x10^{26}$	source concentration
NSUB	$1/m^3$	$1x10^{20}$	channel concentration
TOX	m	10^{-9}	effective oxide thickness
OVS	m	10^{-8}	source gate overlap length
SIGMAS	m	$5x10^{-9}$	lateral sigma of source dopant

Id-*Vg* characteristics of our TCAD model and compact model are compared in Fig.8. Thorough comparison to TCAD with advanced nonlocal model guarantees the physics of the new compact model. Because of our simple assumptions for compact modeling, it is possible to expand the new model to TFETS of other materials and other structures such as double gates and nanowires.

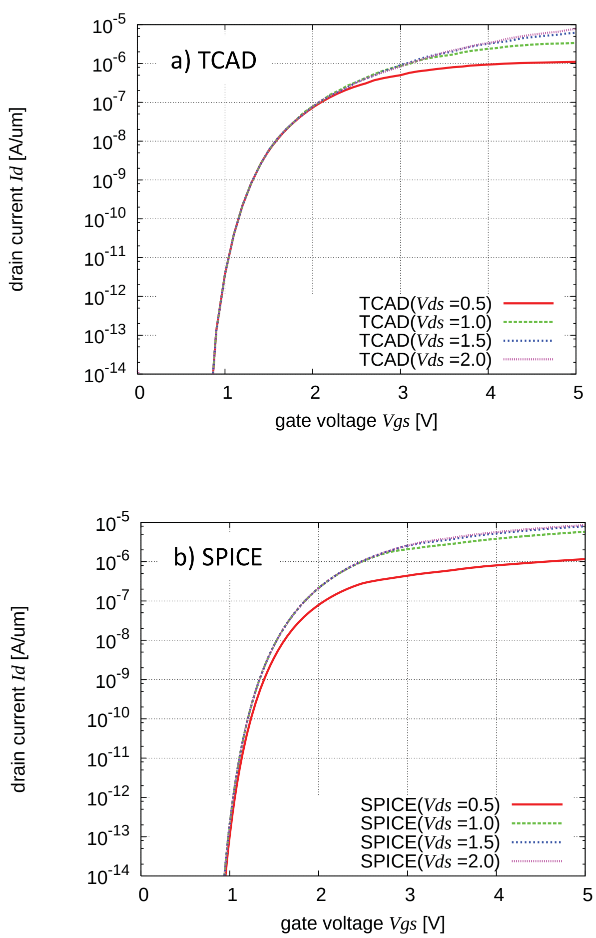

Figure 8. *Id*-*Vg* characteristics of a TFET calculated by a) the present TCAD model and b) the present compact model.

IV. CONCLUSIONS

New set of TCAD and compact models based on nonlocal band to band tunneling formalism are developed. In the device modeling, we adopt conduction and valence band trace algorithms, and include volume effects. The device simulation results are in good agreement with our measurements. In the compact modeling, nonlocal tunneling concept is successfully introduced by assuming simple potential around source gate overlap regions. These models become physics-based practical tools for active usage in developing TFETs.

ACKNOWLEDGMENT

This research is granted by JSPS through FIRST Program initiated by CSTP.

REFERENCES

[1] K. Fukuda, T. Mori, W. Mizubayashi, Y. Morita, A. Tanabe, M. Masahara, T. Yasuda, S. Migita, and H. Ota, "TCAD-based Modeling of Tunnel FETs," Int. Symp. "Develop. Core Tech. Green Nanoelectronics", Mar. 2012.

[2] T. Mori, K. Fukuda, A. Tanabe, T. Maeda, W. Mizubayashi, S. O'uchi, Y. Liu, M. Masahara, T. Yasuda, and H. Ota, "Impacts of EOT scaling on SOI Tunnel FETs and Demonstration of 33mV/decade Subthreshold Slope," Int. Symp. "Develop. Core Tech. Green Nanoelectronics", Mar. 2012.

[3] S. Migita, and H. Ota, "Fabrication of Silicon Tunnel-FETs Using Epitaxial NiSi2 Schottky Source Junctions and Dopant Segregation Technique," Int. Symp. "Develop. Core Tech. Green Nanoelectronics", Mar. 2012.

[4] HyENEXSS™, ver5.5, Selete, 2011.