Correlation-Aware Analysis of the Impact of Process Variations on Circuit Behavior

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***Abstract*—Performance variations of a 6-transistor SRAM cell were analyzed using coupled process, device, and circuit simulation. The propagation of process-induced variations to device and circuit performance was simulated. Variation sources from lithography, etching, and temperature profiles in rapid thermal annealing were considered and correlations between variations and performance parameters were studied.**

Keywords: ***MOSFET; SRAM; simulation; variations.***

I. INTRODUCTION

Process variations have become a major problem for current and future CMOS fabrication. Moreover, it is no longer satisfactory to only consider worst-case scenarios via corner analysis, as these may be overpessimistic. In consequence, the impact of process variations from their sources at equipment level or due to statistical effects must be traced throughout all process steps and device simulation up to circuit level, including the rigorous treatment of correlations.

II. METHODOLOGY

Single gate fully-depleted silicon-on-insulator (FD SOI) MOSFETs were investigated in this work. The impact of focus and dose variations in 193 nm water immersion lithography on gate length and gate width was studied using rigorous lithography simulation with Dr.LiTHO [1]. Polysilicon gate etching including critical dimension (CD) variations across the wafer was treated using CFD-ACE [2] for equipment simulation and ANETCH [3] for feature-scale simulation. Temperature variations in flash annealing were approximated by a simple analytical model [4] as input to subsequent process simulation using Sentaurus Process [5]. Device performance was simulated with Sentaurus Device [5]. SPICE parameters were extracted from the numerically simulated IV-characteristics, including the V_{th} roll-off and the narrow width effects, using BSIM3SOI [6]. Correlations between various process variations were investigated using the approach published elsewhere [7]. Details on the processes studied and results on device level were published elsewhere [4, 7, 8]. This paper focuses on the discussion of the subsequent variations of SRAM performance including a study of the correlation between the variations considered, resulting contact resistances, and parameters for SRAM performance.

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Six parameters are considered to describe the sources of variations. Four statistically distributed parameters define the defocus and illumination dose uncertainty during the photo lithography steps for the lines defining the gate length and gate width, one parameter defines the etch bias and another one the temperature uncertainty in flash annealing. Four intermediate variables that are dependent on the sources of variations mentioned above describe the variability of the contact resistances which are determined in the first line by the temperature variations during the rapid thermal annealing steps and by the contact area.

III. RESULTS

First of all, we simulated the 6-T SRAM cell without taking process variability into account. The contact resistances were included as it is presented in Figs. 1 and 2.

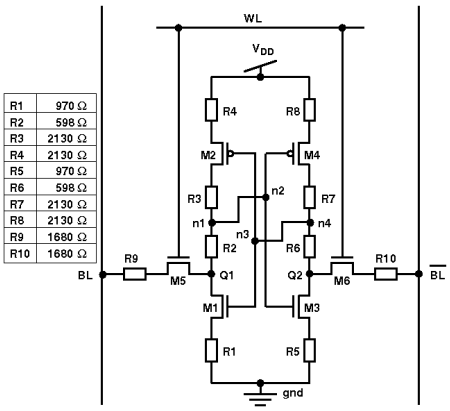

Figure 1. Circuit scheme of the 6-T SRAM cell including contact resistances [8]

The contact resistances are rather sensitive to the temperature of annealing because their values are stronger influenced by the doping concentration in silicon near the contact surface than the resistivity of silicon itself at high doping levels. We simulated the values of the contact resistance in dependence on the flash peak temperature and the contact area by the following formulas:

$$\rho_{co}\ T_{peak} = x + yT_{peak} + zT_{peak}^2,$$

$$R_{co} = \frac{\rho_{co}(T_{peak})}{A_{co}},$$

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where T_{peak} is the random peak temperature uniformly distributed in the temperature range between 1232°C and 1332°C, and A_{co} is the random area resulting from the results of photo lithography and etching simulations.

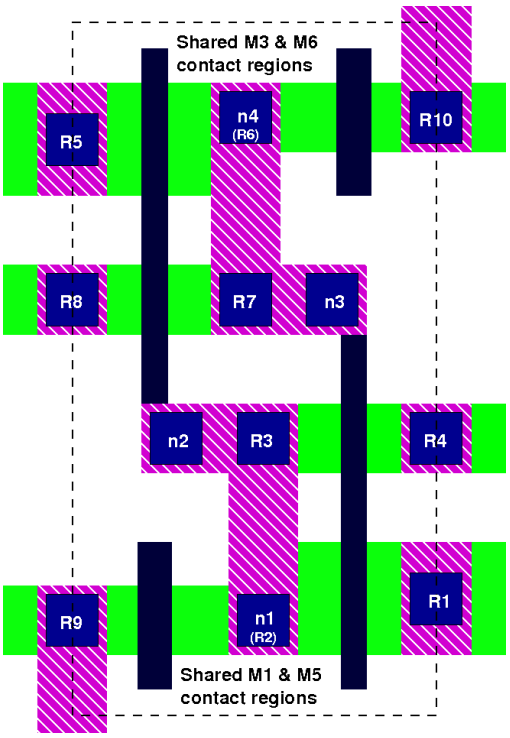

Figure 2. SRAM cell layout and locations of the contact resistances [8]

In the example studied, the contact resistances caused a performance loss of 28% in case of the READ speed (Fig. 3) and 52% of the WRITE speed (Fig. 4).

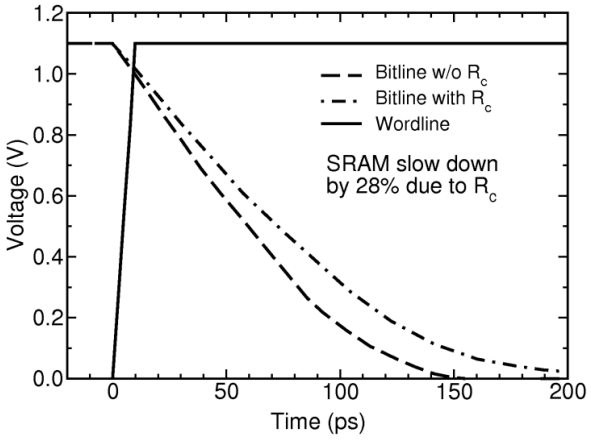

Figure 3. SRAM READ operation without R_c and with R_c

Next, concerning variations we separately simulated the NMOS and PMOS transistors of the inner SRAM flip-flop to investigate the I_{on}-I_{off} relation (Figs. 5 and 6 without and including R_{co}) and the V_{th} (Fig. 7) spread in presence of process variations.

The inclusion of the contact resistances does not change the leakage currents in the off-state of transistors but reduces the on-currents and widens their distribution. For V_{th} we observed an asymmetric distribution function (Fig. 7), although the distribution of L_{gate}, after lithography and patterning, looks Gaussian like (see insets). Therefore, in a next test, we assumed L_{gate} to be Gaussian distributed, performed 10000 simulations, and found the threshold voltage to be again asymmetrically distributed (Fig. 8). This is a result of the effect of the roll-off of the threshold voltages in the SOI based transistors at small L_{gate}.

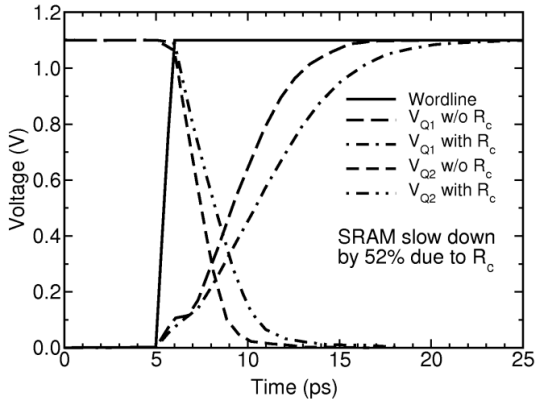

Figure 4. SRAM WRITE operation without R_c and with R_c

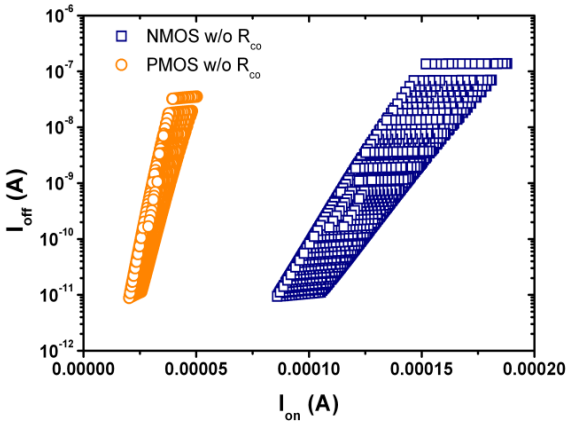

Figure 5. I_{on}-I_{off} of the inner flip-flop resulting from process variability w/o R_{co}

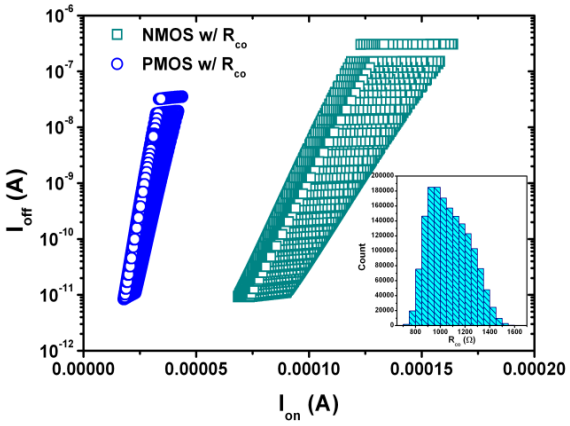

Figure 6. I_{on}-I_{off} of the inner flip-flop resulting from process variability with R_{co} variations as shown in inset

Next, we ran 1.6 million simulations of the SRAM cell to investigate the impact of the 6 sources of process variability studied on the electrical performance of SRAM.

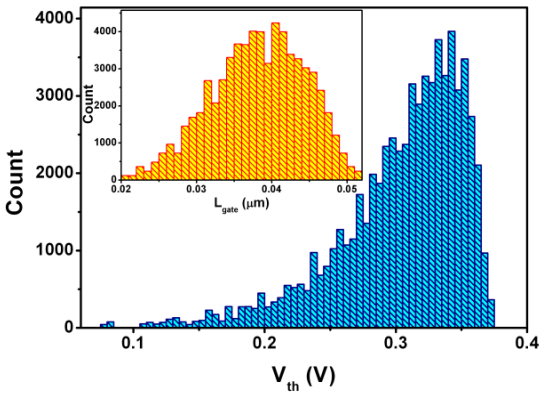

Figure 7. V_{th} distribution of the inner flip-flop NMOSFETs resulting from L_{gate} variations caused by photolithography

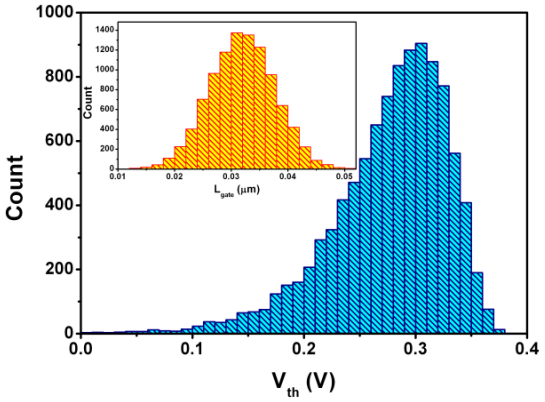

Figure 8. V_{th} distribution of the inner flip-flop NMOSFETs resulting from a Gaussian distributions of L_{gate}. Inserts: Random L_{gate} values used

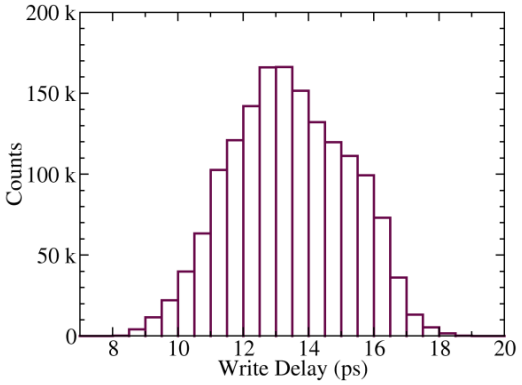

Figure 9. Asymmetric probability distribution function of the WRITE delay

The strongest impact of process variability was found in case of the WRITE delay τ_{WRITE}. The distribution of τ_{WRITE} was found to be rather asymmetrical and having a peculiar shape (Fig. 9). The READ delay is rather strongly correlated with the variations of the contact resistances. The static noise margin of SRAM cell is also strongly correlated with the variation of the dose of illumination during the photolithography step defining the gate length.

Figs. 10 and 11 show some examples of strong and of less strong correlations between processing related parameters and performance parameters of SRAM. The relative variations shown here are measured in the units of standard deviation.

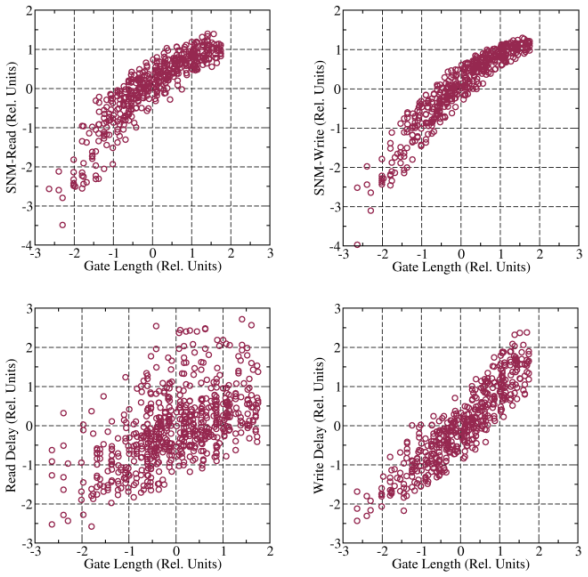

Figure 10. Correlation plots between the gate length of the transistor M2 and the static noise margins and time delays of the SRAM cell in READ and WRITE mode

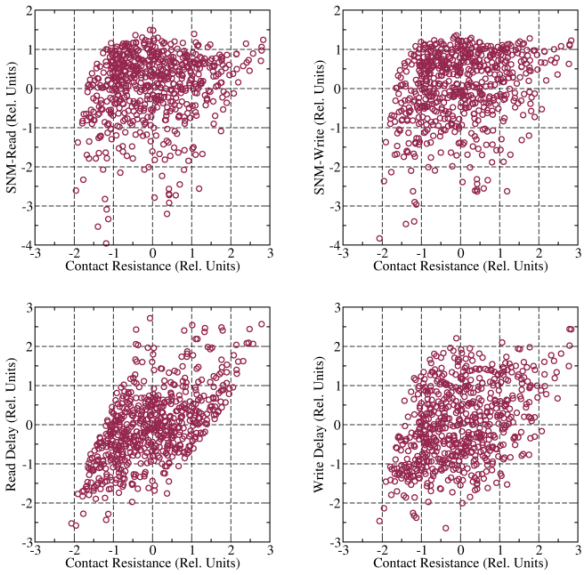

Figure 11. Correlation plots between the contact resistivity R2 and the static noise margins and time delays of the SRAM cell in READ and WRITE mode

As can be seen from Fig. 10, the gate length variations are strongly correlated with the static noise margin parameters and with the time delay in WRITE mode. The correlation between L_{gate} and the time delay in READ mode is not as strong. The dependences of the same performance parameters on variations of contact resistance R2 is shown in Fig. 11. Generally, the correlation of these performance parameters with the contact resistance R2 is not as strong as with the gate length. From Fig. 11 we can see that rather asymmetrical distributions result for example for the distributions of the static noise margins. Fig. 12 shows the

distribution of the static noise margin for the READ mode in the logarithmic scale.

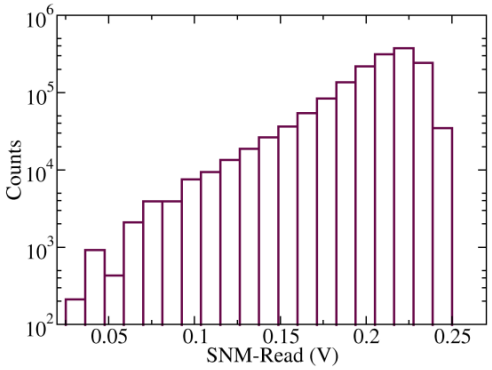

Figure 12. Asymmetric probability distribution function of the static noise margin in the READ mode

The distribution has a long tail to the lower values of the static noise margin. This means that there is a certain, although low, probability of appearing of the cells with a low static noise margin which are prone to malfunction. The delay distribution functions considered exhibit a long tail to the larger values of the delay times. This is also a potentially dangerous situation of appearance of the cells with long delay times. Fig. 13 shows an example of the distribution of the READ delays.

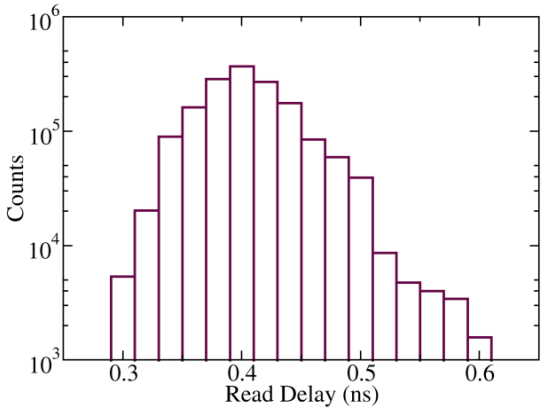

Figure 13. Asymmetric probability distribution function of the READ delay

Finally, we calculated the correlation matrix (Tab. 1) to identify the most critical process parameters. As can be seen in Tab. 1, lithography dose variations in patterning of the gate length and the gate width have the major impact on the dynamic performance of the SRAM cell. Also the contact resistivities which are strongly correlated with the variations of the temperature during the rapid thermal annealing have a significant impact on the performance of the SRAM cells.

TABLE I. CORRELATION MATRIX OF THE WHOLE SIMULATION EXPERIMENT: DO=DOSE, DEF=DEFOCUS, W=WIDTH, L=LENGTH, EB=ETCH BIAS, T=TEMPERATURE, R=CONTACT RESISTANCE, $\tau_{R,W}$= READ/WRITE DELAY

	DefW	DoW	DefL	DoL	EB	T	R1	R2	R4	R9	SNM	τ_R	τ_W
DefW	1	0	0	0	0	0	0	0	0	0	0	0.1	0
DoW	0	1	0	0	0	0	0.2	0.2	0.5	0.3	0	0.5	0.1
DefL	0	0	1	0	0	0	0	0	0.1	0	-0.1	0	0
DoL	0	0	0	1	0	0	-0.3	-0.2	-0.4	-0.2	-0.7	-0.4	-0.8
EB	0	0	0	0	1	0	0	0	-0.1	-0.1	-0.3	-0.2	-0.3
T	0	0	0	0	0	1	-0.9	-0.9	-0.6	-0.9	0.1	-0.2	0
R1	0	0.2	0	-0.3	0	-0.9	1	1	0.8	1	0.2	0.6	0.4
R2	0	0.2	0	-0.2	0	-0.9	1	1	0.8	1	0.2	0.6	0.4
R4	0	0.5	0.1	-0.4	-0.1	-0.6	0.8	0.8	1	0.8	0.4	0.8	0.6
R9	0	0.3	0	-0.2	-0.1	-0.9	1	1	0.8	1	0.2	0.7	0.4
SNM	0	0	-0.1	-0.7	-0.3	0.1	0.2	0.2	0.4	0.2	1	0.6	0.9
τ_R	0.1	0.5	0	-0.4	-0.2	-0.2	0.6	0.6	0.8	0.7	0.6	1	0.7
τ_W	0	0.1	0	-0.8	-0.3	0	0.5	0.4	0.6	0.4	0.9	0.7	1

IV. CONCLUSION

A simulation study about the impact of process variability on the performance of 6-T SRAM cells was presented, starting from lithography simulations up to the circuit level. Lithography related layout variations were determined by full resist lithography simulations. Etching related layout variations were accounted for when simulating gate lengths and widths of the SRAM transistors. The impact of temperature variations in flash annealing was taken into account by including contact resistance variability. Regarding process parameter variations, dose variations during lithography were found to be most critical.

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