Non-Hysteretic Negative Capacitance FET with Sub-30mV/dec Swing over 10^6X Current Range and I_{ON} of 0.3mA/µm without Strain Enhancement at 0.3V V_{DD}

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Abstract—**A new design for negative capacitance FET (NCFET) is proposed. Simulation using 2-D drift-diffusion and 1-D Landau Model exhibits hysteresis free I_D-V_G transfer characteristic with low subthreshold swing (28.3mV/decade over six-orders-of-magnitude current change). Without considering mobility enhancement by strain, non-hysteretic NCFET can achieve I_{ON} of 333 µA/µm at 0.3V V_{DD} (I_{OFF}=10pA/µm).**

Keywords- negative capacitance; NCFET; ferroelectric; FeFET

I. INTRODUCTION

The subthreshold current of a MOSFET varies at the rate of one decade (at best) for every 60mV change in the gate voltage. It can be overcome with different transport mechanisms such as impact ionization [1], tunneling [2], or positive feedback [3]. Another solution is to utilize negative capacitance [4], which does not alter the transport physics and rather seeks to 'amplify' the gate voltage electrostatically to achieve sub-60mV/dec subthreshold swing (SS). It has been shown that negative capacitance FET (NCFET) can be operated in (1) hysteretic (2) antiferroelectric, and (3) non-hysteretic modes [5]. Hysteretic operation has memory applications. Antiferroelectric operation has recently been proposed to dramatically reducing V_{DD} by enhancing I_{ON} and lowering SS [5]. So far, non-hysteretic operation has been overlooked because of the insignificant improvement in SS due to a large mismatch between the ferroelectric negative capacitance (C_{FE}) and the MOS capacitance (C_{MOS}) in the subthreshold regime. Nonetheless, NCFET could be more appealing to circuit designers without the complexity of hysteresis. This paper demonstrates that by using body profile engineering, non-hysteretic NCFET with sub-30mV/dec SS over six-orders-of-magnitude current change can be achieved, and is a candidate in the future for ultra-low power applications.

II. STRUCTURE AND SIMULATION METHOD

The structure of the device is shown in Fig. 1(a). The bottom layer is heavily doped p-type (N_{WELL}), which serves to terminate the depletion region in the channel and to cut off the sub-surface leakage path. The channel is a thin undoped silicon layer on heavily doped silicon or, in general, a thin semiconductor on conductor (TSOC), which is the key to this design. Similar to FinFET, the thin layer design also allows scaling to extreme short channels [6,7] and reduces the effects of random dopant fluctuation and mobility degradation. This layer could be formed by epitaxial deposition as demonstrated in [8]. A ferroelectric (FE) film is deposited over a metal/high-k dielectric stack. The function of the electrically floating metallic layer and the use of 1-D Landau model for the FE are explained in [5].

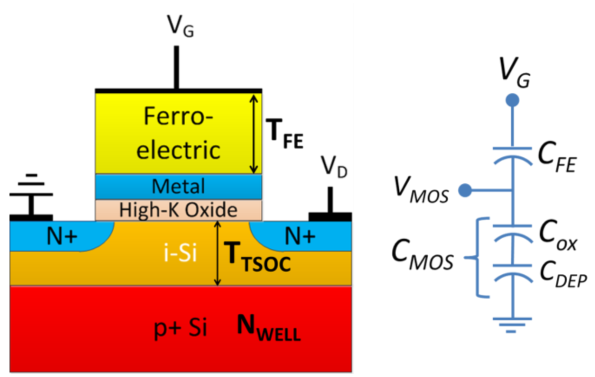

Figure 1 (a) Schematic cross-section views of a NCFET. (b) Simplified capacitance representation of a NCFET.

III. THE DESIGN CONCEPT

We use a simple capacitance model (Fig. 1(b)) to illustrate the design concept, and then present detailed 2-D simulation results.

One may consider NCFET as a MOSFET with an added voltage amplifier. Because of the negative capacitance voltage amplifying effect (**β**) (**β**=$\Delta V_{MOS}/\Delta V_G$), subthreshold swing is reduce by a factor of **β**. In the subthreshold regime, **β** can be derived from a simple capacitive voltage divider:

$$\Delta V_{MOS} = \Delta V_G * C_{FE} / (C_{FE} + C_{MOS}). \quad (1)$$

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$$\beta = \Delta V_{MOS} / \Delta V_G = |C_{FE}|/(|C_{FE}| - C_{MOS}) . \qquad (2)$$

In order to obtain a large β, the magnitude of C_{FE} and C_{MOS} needs to be relatively close. However, C_{MOS} is not a constant but varies with V_G (think the MOS CV curve); therefore β is not a constant. If and when $|C_{MOS}| >= |C_{FE}|$, e.g. in strong inversion, the "swing" is infinite and I_D jumps to another branch of the hysteretic I_D-V_G curve [5].

For non-hysteretic operation, $|C_{FE}|$ needs to be larger than C_{MOS} throughout the V_G range, meaning $|C_{FE}|$ is larger than C_{OX}. With uniformly doped substrate, the depletion capacitance (C_{DEP}) and therefore C_{MOS} could be much lower than C_{OX}. So from Equation 2, β cannot be significantly larger than 1 over a large V_G range. The proposed TSOC structure pins the depletion width at T_{TSOC}, making C_{DEP} large and insensitive to gate bias. Therefore, (1) a small SS can be achieved and (2) the SS remains small in the entire subthreshold regime.

IV. Simulation Results and Discussions

2D simulation includes all the usual effects in MOSFETs such as parasitic capacitances between the metallic floating gate and source drain, etc. For simplicity, source/drain contact resistance and strain induced mobility enhancement is not included. Fig. 2 shows I_D-V_G of non-hysteretic NCFETs at V_{DD} of 0.3 to 0.5V. The average SS is 27.2mV/dec for 0.5V_{DD}, and 28.3mV/dec for 0.3V_{DD}, calculated from I_D of 1 pA/µm to 1 µA/µm.

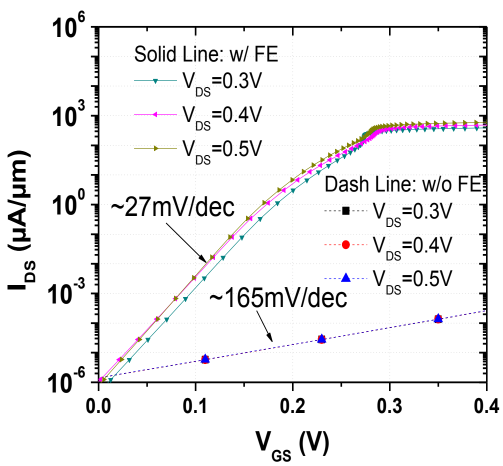

Figure 2. 2-D Simulated non-hysteretic NCFET I_D-V_G transfer characteristic. With FE, the IV curves show substantial improvements in both SS an I_{ON} without any hysteresis. Note that the MOSFET has large SS of ~165mV/dec because the structure is optimized for NCFET with a TSOC layer. The three dash lines almost overlap on each other. L_G=100nm, T_{TSOC}=5nm, N_{WELL}=2E20/cm^3. IV curves shown are Vt adjusted with I_{OFF}=1E-6 at V_G=0.

Fig. 3 illustrates the effect of C_{FE} to the design of a stable non-hysteretic NCFET. The T_{FE} required is dictated by FE material characteristics. It is around 50nm using the FE reported in [9]. The optimal C_{FE} is defined as the minimal C_{FE} required for non-hysteretic operation.

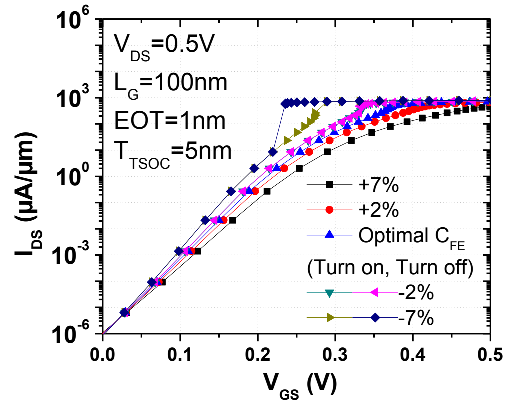

Figure 3. I_D-V_G for different C_{FE} values. +% refers to $|C_{FE}|$ larger than the optimal value and no hysteresis in the I-V curve. Optimal C_{FE} refers to minimum C_{FE} without hysteresis. -% refers to $|C_{FE}|$ smaller than the optimal value and hysteresis exists. IV curves shown are Vt adjusted with I_{OFF}=1E-6 at V_G=0.

Fig. 4 shows that average SS changes almost linearly when C_{FE} is larger than the optimal value. It also indicates that thicker EOT reduces SS even with C_{FE} optimized for C_{OX}. Since T_{TSOC} and therefore C_{DEP} is not scaled with C_{OX} in this case, C_{MOS} stays in a narrower range from subthreshold to inversion for thicker EOT, resulting in a larger β (Eq. 1) and therefore smaller SS.

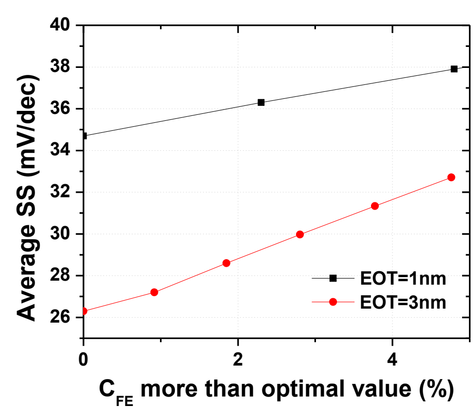

Figure 4. Effects of too large C_{FE} on the average SS. When $|C_{FE}|$ exceeds the optimal value, the SS degrades. V_{DS}=0.5V, T_{TSOC}=5nm, L_G=100nm, N_{WELL}=2E20/cm^3. Average SS is calculated from I_{DS} of 1 pA/µm to 1 µA/µm.

Fig. 5 demonstrates that the SS is lowered with increasing N_{WELL} doping concentration. Higher doping concentration is more effective in pinning the depletion region at T_{TSOC}, ensuring that C_{DEP} and therefore C_{MOS} in Eq. 2 stays in a narrower range.

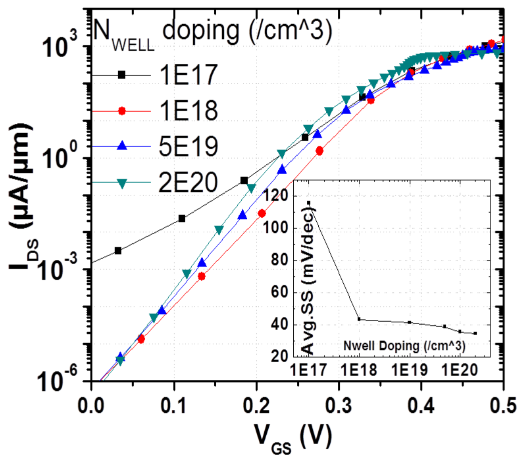

Figure 5. Effects of N_{WELL} (no hysteresis I_D-V_G).The inset shows the average SS for different N_{WELL} doping. V_{DS}=0.5, L_G=100nm, T_{TSOC}=5nm. IV curves shown are Vt adjusted with I_{OFF}=1E-6 at V_G=0. (except N_{WELL}=1E17/cm^3)

Fig. 6 shows that, in order to maintain a certain average SS, T_{TSOC} should be reduced with EOT. For any fixed EOT, SS decreases with thinner T_{TSOC}, which increases C_{DEP}, making C_{MOS} relatively constant and **β** very large from subthreshold to inversion, resulting in a smaller SS. Note that when T_{TSOC} is below 10nm, the reduction of SS becomes more significant. In this case, C_{DEP} could be larger than C_{OX}.

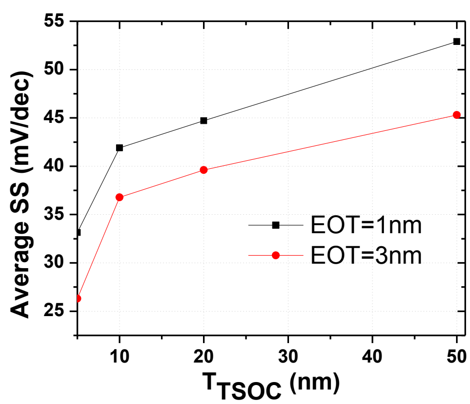

Fig. 6. Effects of T_{TSOC} and EOT on SS. V_{DS}=0.5V, L_G=100nm, N_{WELL}=2E20/cm^3. Average SS is calculated from I_{DS} of 1 pA/μm to 1 μA/μm.

Fig. 7 summarizes the I_{ON} and average SS at different V_{DD}.

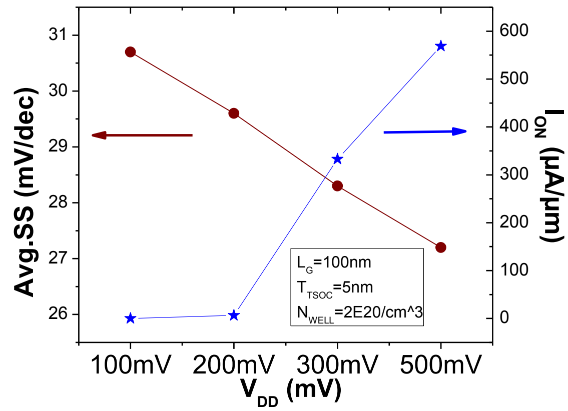

Figure 7. Summary of I_{ON} and average SS for various V_{DD}. Average SS is calculated from I_{DS} of 1 pA/μm to 1 μA/μm. EOT=3nm

V. CONCLUSION

A non-hysteretic NCFET structure with simulated SS of 28.3mV/dec over six orders of magnitude, with I_{OFF}=10pA/um, I_{ON}=0.3mA/um at V_{DD}=0.3V at L_G=100nm and without strain mobility enhancement. Performance can be further improved with shorter L_G or mobility enhancement. The thin T_{TSOC} layer design is responsible for the greatly improved performance.

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