# Toward 44% Switching Energy Reduction for FinFETs with Vacuum Gate Spacer

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*Abstract*—**Up to 44% reduction in switching energy or 22% reduction in ring oscillator delay time are obtained in simulations by FinFET gate spacer optimization. Using vacuum spacer instead of nitride spacer required for future self-aligned contact technology, the fringing gate capacitance can be lowered by 15%, which results in significant speed increase and energy consumption reduction. The speed benefit can be leveraged to further lower the supply voltage and energy consumption. The vacuum spacer can provide relief to this trend.**

***Keywords-Vacuum Spacer; Air Spacer; Spacer Optimization; FinFET; Multi-Gate; CMOS***

## I. INTRODUCTION

As the CMOS technology continues to advance, device becomes smaller and the gate to source/drain/contact-plug capacitance is increasingly important. This capacitance, further amplified by Miller effect on the drain side, has a detrimental impact on the speed and energy consumption of the circuit. Togo et al. [1] reported about 6% reduction of ring oscillator delay time with a vacuum spacer at 0.25um channel length. Park and Hu [2,3] showed how vacuum spacer can be integrated in planar CMOS (with self-aligned contacts) to achieve 30% higher inverter speed and 33% smaller switching energy at 20nm gate length. The improvement is particularly large compared with nitride spacer which would otherwise be required for high density self-aligned contact transistors [3].

The FinFET will be used at and beyond 22 nm. Vacuum structure can be integrated into FinFET similar to [2,3]. This study examines the advantage of the vacuum spacer over the nitride one on the FinFET performance. TCAD device mixed-mode simulations [4] are done using a 25600-core super computer at 177 TFLOPS [5].

## II. DEVICE AND MIXED-MODE RING OSCILLATOR SIMULATIONS

### A. *Device Structure and Electrical Characteristics*

For a better understanding, the key process flow and structure of a planar MOSFET with vacuum spacer are illustrated in Fig. 1 [2,3]. As for FinFETs, since the focus of this study is the electrical behavior, we used Sentaurus Structure Editor [6] to construct the FinFETs with nitride, oxide, and vacuum spacers based on previous works [7-9] without discussing the process flow. The three FinFET structures are shown in Fig. 2 and key dimensions are listed in Table I. Fig. 3 shows the $I_DV_G$ characteristics of the FinFETs.

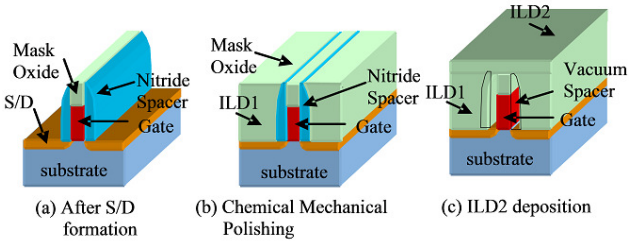


Figure 1. Key process integration for a planar MOSFET with vacuum spacer. See [2,3].

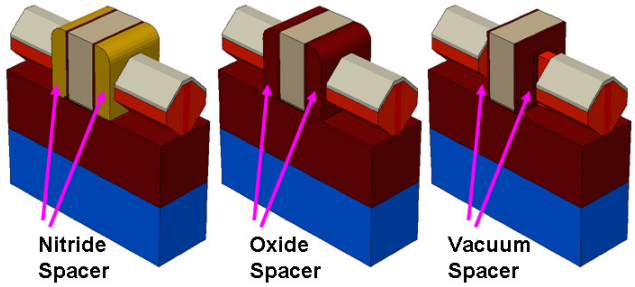


Figure 2. Structures of the FinFETs with nitride, oxide, and vacuum spacers used in simulations. The structures are covered with oxide, the vacuum spacer is a void. See [2,3].

TABLE I. KEY DIMENSIONS OF THE FINFET USED IN SIMULATIONS.

| Key Dimensions | |
|---|---|
| $L_g$ | 25nm |
| $W_{fin}$ | 10nm |
| $H_{fin}$ | 40nm |
| Liner Thickness | 2nm |
| Spacer Thickness | 15nm |
| EOT | 0.9nm |
| Channel Doping | 1e16cm$^{-3}$ |



ISBN 978-0-615-71756-2

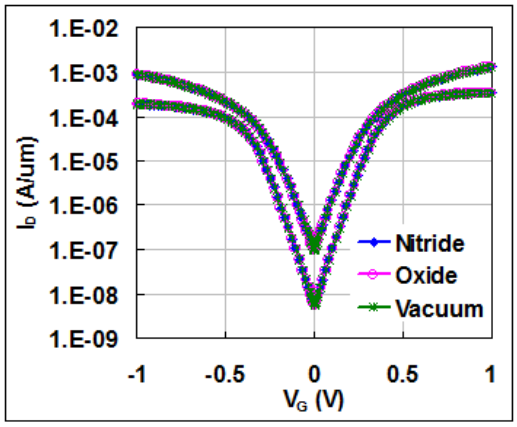


Figure 3. $I_DV_G$ characteristics. $I_{off}$ is set to 100nA/um at $V_{DD}$=1V by adjusting the gate work function.

The $I_{off}$ is set to 100nA/um at $V_{DD}$=1V by adjusting the gate work function. The device performances of three FinFETs, both n- and p-type, are very close, indicating that the spacer dielectric constant only affects the DC performance slightly [2,3].

### *B. Gate Capacitance and Ring Oscillator Simulations*

The gate capacitance $C_{gg}$ of the FinFET was extracted. With the oxide and vacuum spacers, the $C_{gg}$ can be reduced by 6% and 15% respectively compared with the nitride case. Fig. 4 shows the schematics of the inverter and 3-stage ring oscillator used in device mixed-mode simulations [4]. The node outputs of the ring oscillator are given in Fig. 5. The rise time $t_r$ and fall time $t_f$ are defined at $V_{out}$=1/2$V_{DD}$. The delay time $t_d$ is defined as $t_d$=($t_r$+$t_f$)/2. Fig. 6 is the comparison of the delay time $t_d$ of three spacers. As can be seen, the vacuum spacer lowers the $t_d$ by 22% compared with the nitride one. The switching energy SE is defined in (1) [3],

$$\textit{Switching Energy} \quad SE = V_{DD} \cdot \int_0^T I_{DD}\, dt \qquad (1)$$

where T is a cycle time or period, and the simulation result is given in Fig. 7. The advantage of vacuum spacer results in 22% lower in SE compared with the nitride spacer. The benefit of $t_d$ reduction can be leveraged to lower the $V_{DD}$ to further reduce the energy consumption. As shown in Fig. 8, the $V_{DD}$ of the FinFET with vacuum spacer can be lowered from 1V to 0.76V to have the same $t_d$ as the one with nitride spacer. The SE can be further reduced by 44%.

### *C. Impact of Spacer Thickness on FinFET Performance*

The impact of spacer thickness was also studied. Fig. 9 and 10 show the $I_{Dsat}$ vs. spacer thickness of n- and p-type FinFETs. The $I_{Dsat}$ decreases as the spacer thickness increases, mainly due to the increase of source/drain series resistance. The $C_{gg}$ and the reduction by vacuum spacer $\Delta C_{gg}$ vs. spacer thickness are given in Fig. 11. As can be seen, the $\Delta C_{gg}$ increases as the spacer becomes thinner due to the $C_{gg}$ of nitride spacer

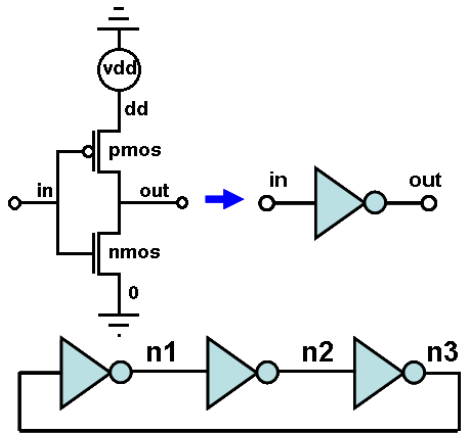


Figure 4. Schematics of the inverter and 3-stage ring oscillator used in Sentaurus Device mixed-mode simulations [4].

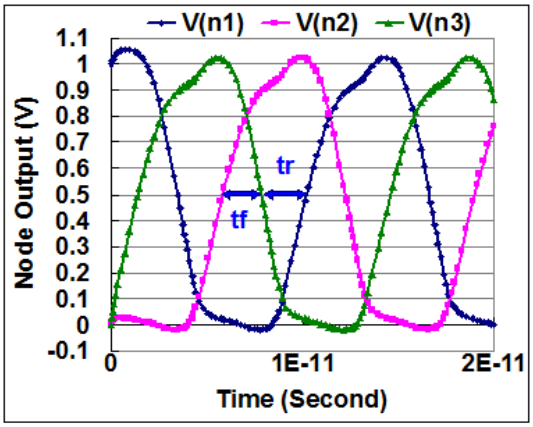


Figure 5. Node outputs of the 3-stage ring oscillator. The rise time $t_r$ and fall time $t_f$ are defined at $V_{out}$=1/2$V_{DD}$. The delay time $t_d$ is defined as $t_d$=($t_r$+$t_f$)/2.

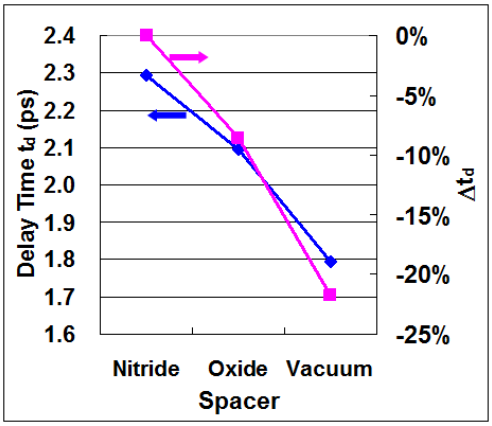


Figure 6. Delay time $t_d$ and the reduction $\Delta t_d$ vs. spacer. The vacuum spacer reduces $t_d$ by 22% and the oxide spacer by 9% compared with the nitride spacer.

increases faster than the one of vacuum spacer. Fig. 12 shows the reduction percentage of $C_{gg}$, $t_d$, and SE by vacuum spacer

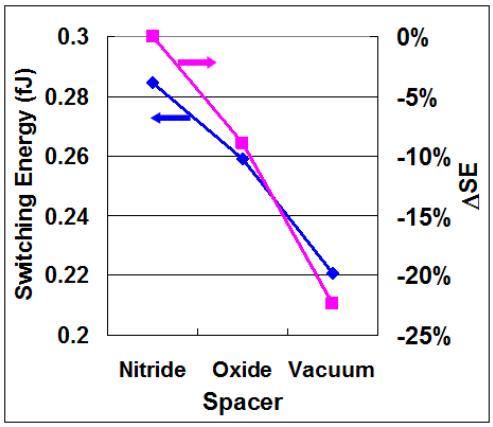


Figure 7. Switching energy SE and the reduction ΔSE vs. spacer. The vacuum spacer lowers SE by 22% and the oxide spacer by 9% compared with the nitride spacer.

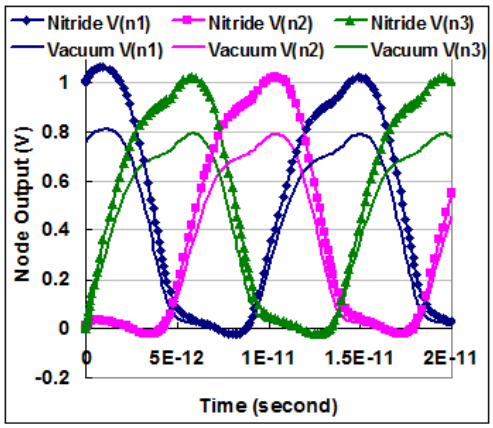


Figure 8. $V_{DD}$ of the FinFET with vacuum spacer is lowered from 1V to 0.76V to have the same $t_d$ as the one with nitride spacer. Switching energy is further reduced by 44%.

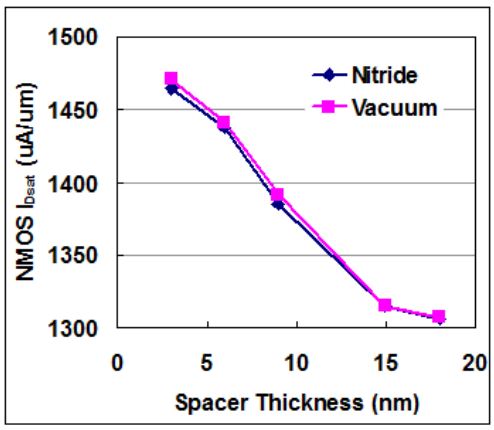


Figure 9. $I_{Dsat}$ of n-type FinFET vs. spacer thickness. The $I_{Dsat}$ decreases as the spacer thickness increases, mainly due to the increase of source/drain series resistance.

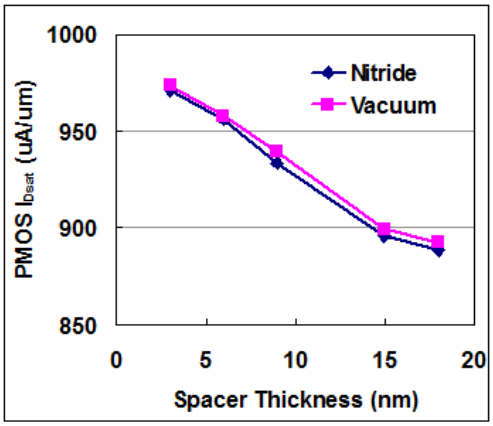


Figure 10. $I_{Dsat}$ of p-type FinFET vs. spacer thickness. The $I_{Dsat}$ decreases as the spacer thickness increases, mainly due to the increase of source/drain series resistance.

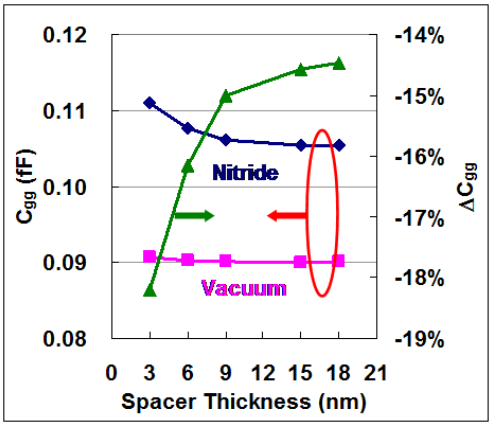


Figure 11. Gate capacitance $C_{gg}$ and the reduction by vacuum spacer $\Delta C_{gg}$ vs. spacer thickness. The $\Delta C_{gg}$ increases as the spacer becomes thinner.

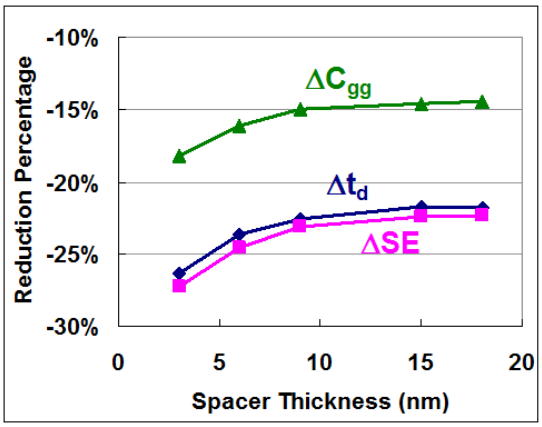


Figure 12. Reduction of gate capacitance $C_{gg}$, delay time $t_d$, and switching energy SE by vacuum spacer vs. spacer thickness. 1% reduction in $C_{gg}$ results in about 1.5% reduction in $t_d$ and SE.

vs. spacer thickness. As the spacer thickness is scaled down, the reductions of $t_d$ and SE become more significant and 1% reduction in $C_{gg}$ results in about 1.5% reduction in $t_d$ and SE.

## III. CONCLUSION

The vacuum spacer reduces the gate to source/drain/contact-plug capacitance compared with the nitride and oxide spacers and results in significant speed increase and energy consumption reduction. As the spacer thickness continues to be scaled down, the vacuum spacer is an attractive solution to the increasing gate-contact capacitance.

TABLE II. ADVANTAGE OF THE VACUUM SPACER COMPARED WITH THE NITRIDE ONE.

| **Advantage of Vacuum Spacer** | |
|---|---|
| Channel length $L_g$ | 25nm |
| Spacer thickness | 15nm |
| Gate capacitance $C_{gg}$ reduction | 15% |
| Delay time $t_d$ reduction | 22% |
| Switching energy SE reduction @ $V_{DD}$=1V | 22% |
| Switching energy SE reduction @ $V_{DD}$=0.76V | 44% |

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