A Robust and Efficient MTJ-based Spintronic IMP Gate for New Logic Circuits and Large-Scale Integration

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Abstract— **A novel circuit topology of a spintronic stateful implication (IMP) logic gate based on a spin transfer torque-operated magnetic tunnel junction (STT-MTJ) is proposed and analyzed. It is demonstrated that the proposed topology reduces the IMP error and also the energy consumption by about 60% as compared to the conventional one. Stateful IMP-based logic uses the nonvolatile memory unit (MTJ device) as the main computing element (logic gate) unlike the previously proposed MTJ-based logic-in-memory circuits, where MTJs are only ancillary devices in logical computations. Since the MTJ devices are CMOS compatible, the generalization of the spintronic IMP gate to a large-scale nonvolatile logic-in-memory system is compulsory. As an example we consider an IMP-based implementation of a full adder. In contrast to an earlier proposed IMP-based full adder with 37 operations, our design involves only 27 subsequent FALSE and IMP operations.**

Keywords- implication (IMP) logic; nonvolatile logic-in-memory; magnetic tunnel junction (MTJ); spin transfer torque (STT)

I. INTRODUCTION

Material implication (IMP) is a fundamental Boolean logic operation on two variables p and q (‘*p* IMP *q*’ or ‘if *p*, then *q*’), which is equivalent to ‘(NOT *p*) OR *q*’ as shown in Fig. 1a. Although it is in common use by logicians, it is seldomly discussed in computing and electrical engineering communities. In combination with the FALSE operation (writing Logical 0), the IMP operation forms a complete logic basis in which any Boolean function can be computed.

Recently, the realization of the IMP operation in a simple circuit including a linear resistor and two titanium dioxide (TiO_2) memristive switches was reported [1] to enable stateful logic operations, for which the memristive switches serve simultaneously as logic gates and latches. The resistance switching ratio of the TiO_2 memristive switches [2], [3] is about two orders of magnitude higher than the theoretical maximum of the magnetic tunnel junction (MTJ) switches [4], [5]. This high ratio guarantees the expected logic output by providing a high state dependent modulation (SDM) of the current or voltage required for switching.

In this work the realization of the IMP operation using spin transfer torque (STT)-operated MTJ devices based on a critical current density required for STT switching and a positive feedback between the MTJ resistance changes during the switching and the current density above the threshold has been demonstrated in a new circuit topology (Fig. 1c) as compared to the conventionally used topology (Fig. 1b).

II. MTJ-BASED IMP LOGIC GATES ANALYSIS

The MTJ contains two ferromagnetic layers separated by a thin non-conductive tunneling barrier. The electrical resistance of the device depends on the relative orientation of the magnetization directions of the ferromagnetic layers. The parallel (P) magnetization state results in a low-resistance state (R_P; logical 1) across the barrier, while the antiparallel (AP) alignment places it in a high-resistance state (R_{AP}; logical 0) and the resistance modulation is described by the tunnel magnetoresistance (TMR) ratio, defined as $(R_{AP} - R_P)/R_P$.

The magnetization of one layer (fixed layer) is pinned, while the magnetization of the second one (free layer) can be switched freely using an external magnetic field or (spin) current passing through the MTJ (STT effect [6], [7]). The STT technique [8] uses spin-polarized electrons to induce directly torque on the magnetization of the free layer and requires a critical current density for switching. With the MTJ-based IMP gate, the initial logic states of the MTJ devices (M_p and M_q) provide a state dependent modulation of the voltage or current of the target MTJ (M_q) which is equivalent to the IMP operation.

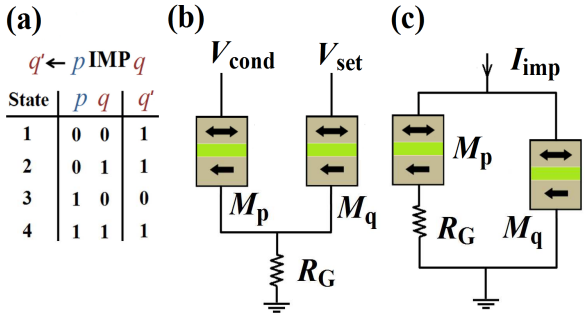

Figure 1. (a) IMP truth table. Conventional (b) [1] and proposed (c) IMP circuit topologies.

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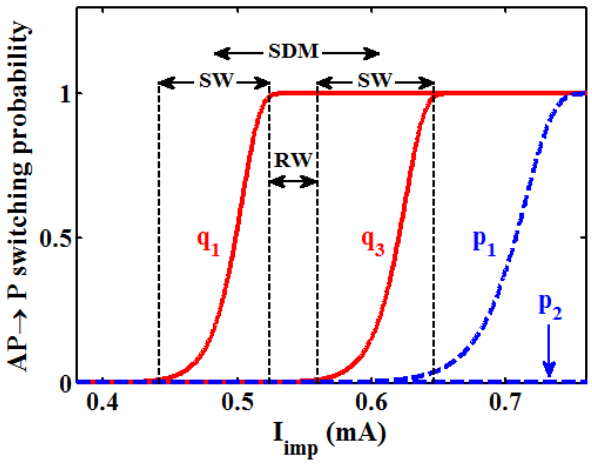

Figure 2. Switching probabilities of *M*q and *M*p for a 50ns IMP operation based on physical devices characterized in [8].

As shown in Fig. 1b, with the conventional topology performing the IMP operation involves simultaneously applying two voltage pulses, V_{SET} and the V_{COND}, to M_q and M_p respectively and the initial logic state of the source MTJ (M_p) provides a state dependent modulation of the voltage across the target MTJ (M_q) through R_G. In fact, when MP is in the parallel state (p=1; State 3 and State 4), $q \leftarrow (p \text{ IMP } q) \equiv (0 \text{ OR } q) \equiv q$, the pulse V_{COND} mostly drops on R_G, so the pulse V_{SET} cannot change q, and both M_p and M_q are left unchanged. But when M_p is in the antiparallel state (p = 0; State 1 and State 2), $q \leftarrow (p \text{ IMP } q) \equiv (1 \text{ OR } q) \equiv 1$, the pulse V_{COND} generates a lower current so the common line voltage decreases and V_{SET} can switch M_q to the parallel state (q = 1) when it is in the antiparallel state. A positive feedback between the memristance M_q and the driving strength accelerates the switching in State 1. It increases the current passing through M_q, while it decreases the current of M_p, so M_q is set ($q \leftarrow 1$), while p is left unchanged (p = 0).

With our proposed topology shown in Fig. 1c the initial logic state of M_p provides a state dependent modulation of the current through M_q, which results in a correct logic behavior of M_q. Because of R_G, the current through M_p is low enough to leave it unchanged. Therefore the current pulse I_{imp} can only switch M_q, when it is in the antiparallel state (q=0; State 1 and State 3). In State 1 M_p is in the antiparallel state, therefore a major part of the I_{imp} will pass through M_q and switch it to the parallel state (q=1). In State 3 M_p is in the parallel state, therefore more current will flow through M_p which reduces the current flowing through M_q making it below the critical current required for switching. Fig. 2 shows all possible AP→P switching probabilities of M_q and M_p as a function of the current I_{imp} for a given value of R_G and pulse duration. It illustrates how the state dependent modulation (SDM) opens a reliable window (RW) between the AP→P switching probability windows (SW) of the M_q in State 1 and State 3. In fact for a current I_{imp} in the interval RW the IMP gate shows a correct logical behavior for which only M_q will switch only in State 1.

III. MODELING

As described before, both, the conventional and the proposed topology enable stateful logic by performing the IMP operation. The IMP gate circuit parameters (R_G, V_{SET}, and V_{COND} for the conventional and I_{imp} and R_G for the proposed topology) can be optimized to minimize the error for determined pulse duration and MJT device characteristics. An example of such an optimization is shown in Fig. 3 for the proposed topology. In order to analyze the reliability of the IMP gates, we use the theoretical expressions (1) and (1′) [9] of the MTJ switching probability which has been experimentally proved in [8]:

$$P_{sw}^{qi} = 1 - \exp\left\{-\frac{t}{\tau_0}\exp\left[-\Delta_0\left(1-\frac{I_{qi}}{I_{C0}}\right)\right]\right\}, \quad (1)$$

$$P_{sw}^{pi} = 1 - \exp\left\{-\frac{t}{\tau_0}\exp\left[-\Delta_0\left(1-\frac{I_{pi}}{I_{C0}}\right)\right]\right\}, \quad (1')$$

where P_{sw}^{qi} (P_{sw}^{pi}) and I_{qi} (I_{pi}) are the AP→P switching probabilities and the current flowing through M_q (M_p) in State i (i=1, 2, 3, or 4 as shown in Fig. 1a), Δ_0 is the magnetic memorizing energy without any current and magnetic field, τ_0 is 1ns, I_{C0} is the critical switching current extrapolated to 1 ns, and t is the pulse width. According to the IMP truth table (Fig. 1a), we define the IMP error as:

$$E_{imp} = (1 - P_{sw}^{q1}) + P_{sw}^{q3} + P_{sw}^{p1} + P_{sw}^{p2} \quad (2)$$

In order to calculate I_{qi} and I_{pi} for each topology in each state we use the resistance model of the MTJ in the antiparallel state [7]

$$R_{AP} = R_P\left(1 + TMR_{real}\right) = R_P\left(1 + \frac{TMR_0}{1 + \frac{V_{bias}^2}{V_h^2}}\right) \quad (3)$$

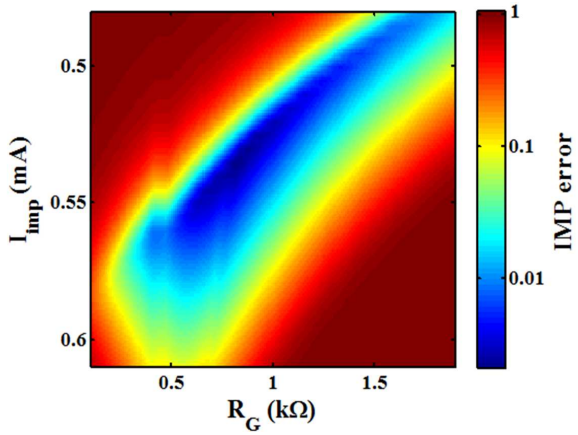

Figure 3. The IMP error as a function of R_G and I_{imp} based on physical MTJ devices characterized in [8] for a pulse duration of 50ns.

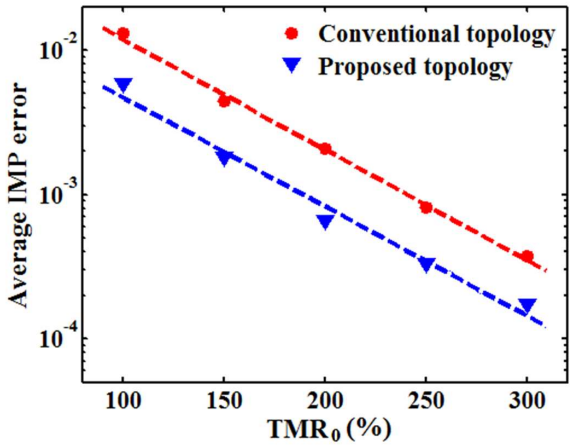

Figure 4. The average IMP error as a function of the TMR_0 ratio for both conventional and proposed topologies.

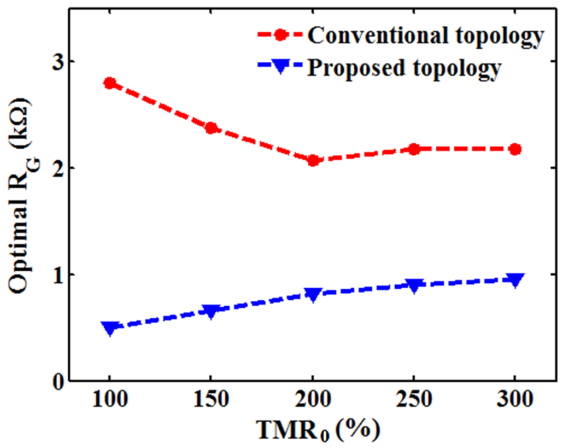

Figure 5. The optimal value of R_G (corresponding to the minimum error design) depends on the TMR_0 ratio.

where TMR_{real} and TMR_0 are the TMR ratio under non-zero and zero bias voltage (V_{bias}), respectively and V_h is the bias voltage equivalent to TMR_{real}= 0.5 TMR_0.

IV. Simulation Results and Discussion

Reliable IMP logic behavior requires a wide enough SDM of voltage or current on the M_q. The most important parameter in robust IMP gate design is the TMR ratio. The difference between the initial voltage or current on M_q and M_p in different initial states increases with increasing TMR ratio of the MTJs devices. Therefore, increasing the TMR ratio enlarges the SDM and the RW windows shown in Fig. 2. Fig. 4 shows the minimum IMP error for different TMR_0 ratios with optimal circuit parameters (R_G, V_{SET}, and V_{COND} for the conventional and I_{imp} and R_G for the proposed topology). It demonstrates that in both conventional and proposed topologies the IMP error decreases exponentially with increasing TMR ratio. At a fixed TMR the proposed topology provides a higher SDM, thus reducing the IMP error by about 60% as compared to the conventional one.

Fig. 5 shows the optimal value of R_G for different TMR_0 ratios with both topologies. It illustrates that the optimal R_G is lower in the proposed topology as compared to the conventional one. Since in the conventional topology all the current required for switching M_q will pass through R_G, higher R_G results in higher energy consumption for switching events of the IMP operation. Fig. 6 shows the IMP energy consumption calculated using the SPICE model of the MTJ [10]. It demonstrates that in the proposed topology, the IMP energy consumption is about 60% lower than in the conventional one.

V. Large-Scale Integration

Stateful IMP-based logic allows the cells to both store logic values and perform logic operations. Since the MTJ devices are CMOS compatible, the generalization of the spintronic IMP gate to a nonvolatile logic-in-memory system is compulsory.

It can be shown that based on the 1T/1MTJ structure in the spin-RAM architecture [8], the proposed topology of an IMP gate can be achieved by applying a current pulse (I_{imp}) to two bit lines simultaneously and connecting one source line directly to the ground (source line of M_q) and connecting the second source line to the ground through R_G (source line of M_p). Therefore, a large-scale logic-in-memory circuit can be achieved based on the existing magnetic memory technology for which the non-volatile memory element (MTJ) is used as the main computing element (logic gate) at the same time, in contrast to the previous logic-in-memory or MOS/MTJ-hybrid logic circuits [11]-[14] for which the non-volatile memory elements are used as ancillary devices for logical computations.

We consider an IMP-based implementation of a full adder which is a basic element of arithmetic circuits. As is well known, a full adder adds three binary inputs (q_1, q_2 and c_{in}) and produces two binary outputs, sum (s) and carry (c_{out}) as shown in Fig. 7.

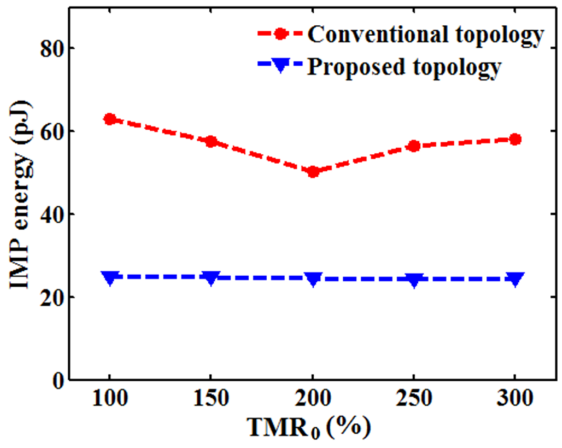

Figure 6. The IMP energy consumption depends on the TMR_0 ratio for both conventional and proposed topologies.

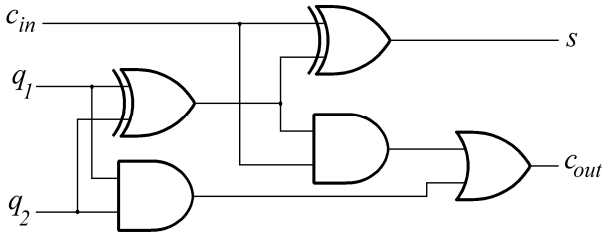

Figure 7. A logic diagrame of a full adder.

Since IMP cannot fan out, some additional memory elements (a_1, a_2, and a_3) are required to ensure that a logical value (q_1, q_2 and c_{in}) is still available, when it is needed as an input for subsequent IMP operations. We use two subsequent operations, FALSE ($a_i \leftarrow 0$) and IMP ($a_i \leftarrow q_i$ IMP a_i), to write $\bar{q}_i$ (NOT q_i) in the additional cell a_i (i =1-3), in order to ensure that the logical value $\bar{q}_i$ (therefore q_i) will be available as an input for subsequent steps. As 'q_1 IMP q_2' is equivalent to '(NOT q_1) OR q_2', some operations can be eliminated to minimize the total effort for performing a full adder. In contrast to the earlier proposed IMP-based full adder [15] with 19 and 18 operations (37 total) for generating s and c_{out}, respectively, and 4 additional bits, our design involves only 27 subsequent FALSE and IMP operations on inputs (q_1, q_2 and c_{in}) and 3 additional bits (a_1, a_2, and a_3) as

$$a_1 \leftarrow 0,\ a_1 \leftarrow q_1 \text{ IMP } a_1,\ a_2 \leftarrow 0,\ a_2 \leftarrow q_2 \text{ IMP } a_2,$$

$$a_2 \leftarrow a_1 \text{ IMP } a_2,\ a_3 \leftarrow 0,\ a_3 \leftarrow a_2 \text{ IMP } a_3,\ a_2 \leftarrow 0,$$

$$a_2 \leftarrow q_2 \text{ IMP } a_2,\ a_1 \leftarrow a_2 \text{ IMP } a_1,\ a_3 \leftarrow a_1 \text{ IMP } a_3,$$

$$(a_3 \leftarrow q_1 \text{ XOR } q_2)$$

$$a_2 \leftarrow q_1 \text{ IMP } a_2,\ q_1 \leftarrow 0,\ q_1 \leftarrow a_3 \text{ IMP } q_1,$$

$$q_1 \leftarrow c_{in} \text{ IMP } q_1,\ q_2 \leftarrow 0,\ q_2 \leftarrow q_1 \text{ IMP } q_2,\ q_2 \leftarrow a_2 \text{ IMP } q_2,$$

$$(q_2 \leftarrow c_{out})$$

$$a_1 \leftarrow 0,\ a_1 \leftarrow c_{in} \text{ IMP } a_1,\ q_1 \leftarrow 0,\ q_1 \leftarrow a_3 \text{ IMP } q_1,$$

$$q_1 \leftarrow a_1 \text{ IMP } q_1,\ a_1 \leftarrow 0,\ a_1 \leftarrow q_1 \text{ IMP } a_1,$$

$$c_{in} \leftarrow a_3 \text{ IMP } c_{in},\ c_{in} \leftarrow a_1 \text{ IMP } c_{in},$$

$$(a_3 \leftarrow q_1 \text{ XOR } q_2 \text{ XOR } c_{in}).$$

The MOS/MTJ-hybrid logic circuit presented in [11] uses 34 transistors and 4 MTJs for implementing an MTJ-based full adder, while our proposed spintronic stateful logic architecture uses 6 1T/1MTJ cells for a full adder for which the 1T/1MTJ cells serve simultaneously as logic gates and latches.

VI. Conclusion

We have shown the possibility of the realization of a logic operation named material implication (IMP) in two different circuit topologies, each one including a conventional resistor and two MTJs. It has been demonstrated that the IMP error decreases exponentially with increasing the TMR ratio of the MTJ devices. Our proposed IMP circuit topology reduces the IMP error and energy consumption by about 60% as compared to the conventional one.

The generalization of these spintronic IMP gates to a nonvolatile logic-in-memory system enable extending nonvolatile electronics from memory to logical computing applications, for which the STT-MTJ cells serve simultaneously as logic gates and latches and are not ancillary devices for logical computations as compared to conventional logic-in-memory circuits [11], [13]. This can improve the conventional CMOS logic and also opens the door for a shift away from the Von Neumann architecture for innovation in computational paradigms.

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