Development of Predictive Model and Circuit Simulation Methodology for Negative Bias Temperature Instability Effects

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Abstract—**A unified NBTI model describing reaction-limited-diffusion and hole trapping mechanisms is developed. The model is verified with various DC and AC NBTI measurements, and is implemented into the advanced MOSFET model HiSIM enabling to simulate circuit degradation induced during its operation.**

Keywords-NBTI; reaction-limited-diffusion; hole trapping; HiSIM model; circuit simulation

I. INTRODUCTION

To predict circuit degradation induced by the negative bias temperature instability (NBTI) effect is difficult due to the continuous change of the device conditions caused by the repetition of stress/recovery process [1, 2]. In the circuit simulation with the NBTI effect, the previous reaction–diffusion (R-D) model is widely used owing to its simplicity [3]. With the further development of measurement technique, the existing R-D model is demonstrated to be incorrect in describing the short term NBTI effect within the period of several micro seconds [4]. However, accurate prediction of the short term degradation is important, since circuits are usually operated under high frequency AC conditions. Therefore, it is necessary to develop a NBTI model which is able to describe the degradation from short term to long term under various bias conditions. The purpose of this work is to realize accurate circuit simulation considering the NBTI degradation. A unified NBTI model including the mechanisms of the reaction-limited-diffusion (RLD) and hole trapping (HT) is developed. This model is verified by the measurement, and then implemented into the advanced MOSFET model HiSIM [5] for circuit simulation. A simulation method is proposed for predicting AC NBTI degradation on device level as well as the circuit level.

II. MODEL DEVELOPMENT

The developed NBTI model includes two mechanisms: the reaction-limited-diffusion (RLD) of Si-H bonds [6] and the hole-trapping (HT) in the gate oxide. Under a high stress condition, the Si-H bonds at the Si/SiO_2 interface are broken by the injected holes. The H atoms diffuse into gate oxide and further into the poly-Si gate, where they form H_2 molecule. The remained Si dangling bonds cause the threshold voltage shift (ΔV_{th}). The interface state density (n_T) can be obtained with

TABLE. 1 MODEL PARAMETERS OF THE DEVELOPED MODEL.

Variable	Meaning
ΔV_{ths_RLD}	RLD induced ΔV_{th} under stress
ΔV_{thr_RLD}	RLD induced ΔV_{th} under recovery
ΔV_{ths_max}	Maximum ΔV_{th} without recovery
ΔV_{ths_HT}	HT induced ΔV_{th} under stress
ΔV_{thr_HT}	HT induced ΔV_{th} under recovery
$E_{ox}=(V_g-V_{fb}-\varphi_s)/t_{ox}$	Gate electric field
V_g	Gate voltage
V_{fb}	Flat band voltage
φ_s	Surface potential
t_{ox}	Gate oxide thickness,
C_{ox}	Gate oxide capacitance
Parameter	**Meaning**
D_{f_poly} **	H_2 forward diffusion constant
D_{r_poly} **	H_2 reverse diffusion constant
N_T **	Density of Si-H bond at Si/SiO_2 interface
N_{it} **	Density of interface state
N_0 **	Density of tunneling holes into SiO_2
k_s **	Hole trapping time coefficient
k_r **	Hole de-trapping time coefficient
τ_R **	Time constant of Si-H bond reaction
τ_{rec} **	Time constant of recovery
τ_{hs} *	Time constant of hole trapping
τ_{hr} *	Time constant of hole de-trapping
$R_{Eox}=a\cdot exp(bE_{ox})$	Si-H bond reaction rate (*a* and *b*: fitting parameters)
$R_{HT}=c+d\cdot log(e\cdot E_{ox})$	Hole trapping rate (*c*, *d* and *e*: fitting parameters)

* fixed parameter
** depends on material and process

$$\frac{dn_T}{dt}=k_f\left(N_T-n_T\right) \tag{1}$$

Here t is the stress time, $k_f=R_{Eox}/t$ is the forward reaction rate. All the parameter definitions are listed in Table.1. Combining with the diffusion theory, the RLD model during stress/recovery process is obtained as

$$\text{Stress:}\quad \Delta V_{ths_RLD}(t)=\frac{qN_T}{C_{ox}}\cdot R_{Eox}\cdot\log\left(\frac{t}{\tau_R}\right)\cdot\left[1+\left(D_{f_poly}t\right)^{1/6}\right] \tag{2}$$

$$\text{Recovery:}\ \Delta V_{thr_RLD}(t)=\Delta V_{ths_max}-\frac{qN_TR_{Eox}}{C_{ox}}\cdot\log\left(\frac{t_s}{\tau_R}\right)\cdot\log\left(\frac{t-t_s}{\tau_{rec}}\right)+\frac{qN_TR_{Eox}}{C_{ox}}\cdot\log\left(\frac{t_s}{\tau_R}\right)\cdot\left(D_{f_poly}t_s\right)^{1/6}\cdot\left[D_{r_poly}(t-t_s)\right]^{1/6} \tag{3}$$

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Under a low stress condition, holes inject into gate oxide are unable to obtain enough energy for dissociating the Si-H bonds. Therefore, impact of the Si-H bond reaction-diffusion mechanism becomes weaker, and the hole trapping dominates the ΔV_{th}. Based on the trapping theory [7] and tunneling theory [8], the hole trapping model is developed as

$$\text{Stress: } \Delta V_{ths_HT} = \frac{q}{C_{ox}} \cdot \left\{ N_{it}\left[1 - R_{HT}\cdot \exp(-k_s t)\right] + N_0 \left(\frac{t}{\tau_{hs}}\right)^n \right\} \quad (4)$$

$$\text{Recovery: } \Delta V_{thr_HT} = \frac{qN_{it}}{C_{ox}}\left[1 - R_{HT}\cdot \exp(-k_s t_s)\right] \cdot \left\{1 - \exp\left[-k_r(t-t_s)\right]\right\} + \frac{qN_0}{C_{ox}}\left[\frac{t_s}{\tau_{hs}}\left(\frac{t-t_s}{\tau_{hr}}\right)\right]^{0.14} \quad (5)$$

Finally, the unified NBTI model considering the RLD and the HT mechanisms is expressed as

$$\Delta V_{th} = \Delta V_{th_RLD} + \Delta V_{th_HT} \quad (6)$$

In order to make a clear view of contributions of RLD and HT to the total ΔV_{th}, both mechanisms are separately compared with the measured data (Fig. 1a). The RLD model shows a good agreement with measurements under high bias stress over a wide range of time duration. However, with decreased stress bias (V_{g_str}) down to 1.5V or lower, the RLD alone is not sufficient to describe the measured data. Because holes are unable to obtain large enough energy to inject into the gate oxide and the density of dissociated Si-H bond obviously reduces. Thus, the hole trapping mechanism, which is less dependent on the gate oxide field, dominates the degradation.

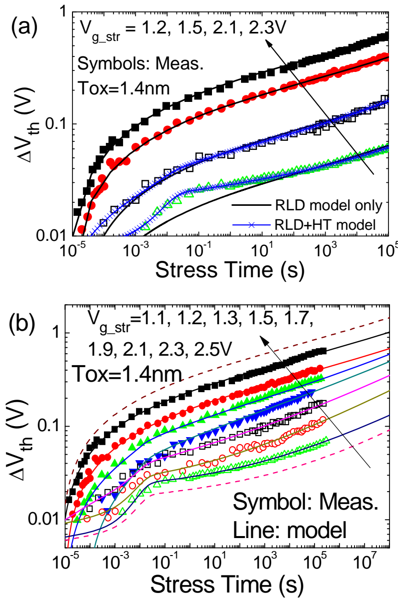

Figure 1 (a) The separate contribution of RLD and HT model to ΔV_{th} under wide stress time duration and bias conditions. (b) Unified NBTI model compared with measured data [9]. ΔV_{th} under higher (V_{g_str}=2.5V) and lower (V_{g_str}=1.1V) is predicted.

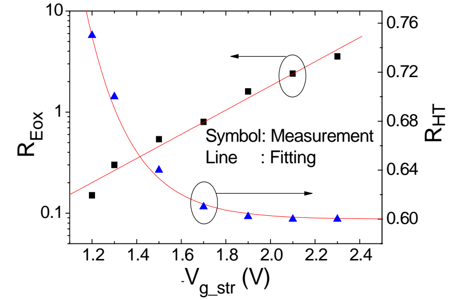

Figure 2. Extracted stress bias condition dependence of the reaction coefficient (R_{Eox}) and hole trapping rate (R_{HT}).

Combining both RLD and HT, the unified model is obtained and compared with the measure data [9] over a wide range of stress time durations and bias conditions (Fig. 1b). The ΔV_{th} under higher (V_{g_str}=2.5V) and lower (V_{g_str}=1.1V) stress biases is predicted well. As shown in Fig. 2, the Si-H reaction rate R_{Eox} and hole trapping rate R_{HT} are extracted from the measurements. Both of them are strongly related to the bias condition, which is associated with the gate oxide electric field.

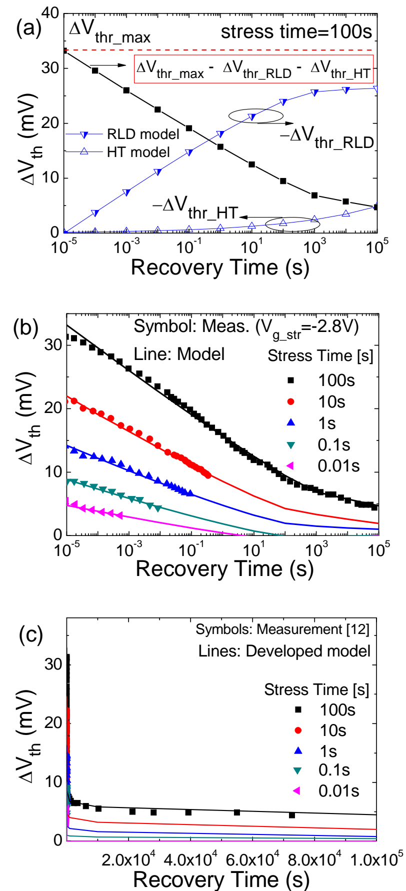

Figure 3. (a) Separate contribution of RLD and HT model to the recovery characteristics. (b) Comparison of the unified NBTI model with the recovery measured data [10] after various stress conditions. (c) Linear plot of ΔV_{th} recovery. A fast recovery is observed in the initial period and then leveling of in the long term region.

Fig. 3a shows separated contributions of the RLD and the HT mechanism in the recovery process. H atoms remained in the gate oxide diffuse back to the Si/SiO_2 interface very fast and repair the Si dangling, therefore, a fast recovery is observed in the initial recovery stage. H_2 molecules remained in the poly-Si gate take long time to diffuse back into the gate oxide, and some of them even diffuse out of the poly-Si gate, which is observed as the long term ΔV_{fb} degradation. On the contrary, the recovery rate of trapped holes is slow at the initial stage, but obviously increases in the long term period. In Fig. 3a, ΔV_{thr_max} indicates the maximum ΔV_{th} without recovery after 100s stress. ΔV_{thr_RLD} and ΔV_{thr_HT} are V_{th} recovery caused by the mechanisms of RLD and HT, respectively. Therefore, subtracting the recoverable parts (ΔV_{thr_RLD} and ΔV_{thr_HT}) from the ΔV_{thr_max}, the recovery property is predicted. The developed NBTI model also shows high accuracy after experiencing various stress time (Fig. 3b). From Fig. 3c, a fast recovery is observed at the initial stage, then leveling off in the long term region. The model parameters extracted from measurements shown in Figs. 1 and 3 are used for the following circuit simulations.

III. CIRCUIT SIMULATIONS

Observed from the previous literatures, the NBTI effect mainly results in a parallel shift of the subthreshold current [11]. Therefore, the implementation of the NBTI degradation is done as a flat band voltage shift (ΔV_{fb}) in HiSIM. As shown in the flow chart in Fig. 4a, the gate oxide field at the ith time step t_i [$E_{ox}(t_i)$] is calculated from $V_{fb}(t_i)$ given by HiSIM model, here $E_{ox}(t_i)=(V_g-V_{fb}(t_i)-\varphi_s(t_i))/t_{ox}$, V_g is the gate voltage, φ_s is the surface potential at threshold condition and t_{ox} is the gate oxide thickness. Since R_{Eox} and R_{HT} in the RLD model and the HT model are E_{ox} dependent (Fig. 2), ΔV_{fb} at t_i is calculated by $\Delta V_{th}(t_i)$, which is the function of $E_{ox}(t_i)$. Then $V_{fb}(t_{i+1})$ is calculated by adding $\Delta V_{th}(t_i)$ to $V_{fb}(t_i)$. The shift of V_{fb} makes the gate electrical field changing from $E_{ox}(t_i)$ to $E_{ox}(t_{i+1})$.

The simulation method for ΔV_{th} under arbitrary E_{ox} is described in Fig. 4b. The decision of stress or recovery is done by the sign (-/+) of E_{ox}. The time interval is Δt, thus $t_{i+1}=t_i+\Delta t$. Under a stress condition, the electrical field at the first time point $t_{s,1}$ is obtained as $E_{ox}(t_{s,1})$ by using HiSIM. The Si-H reaction rate $R_{Eox}(t_{s,1})$ and hole trapping rate R_{HT} $(t_{s,1})$ are obtained following the relationship shown in Fig. 2, so that the threshold voltage shift at $t_{s,1}$ is calculated from (2) and (4) as $\Delta V_{ths}(t_{s,1})=\Delta V_{th_RLD}[E_{ox}(t_{s,1})]+\Delta V_{th_HT}[E_{ox}(t_{s,1})]$. At the second time point $t_{s,2}$, the flat band voltage V_{fb} is shifted to $V_{fb}(t_{s,2})$ as $V_{fb}(t_{s,2})=V_{fb}(t_{s,1})+\Delta V_{ths}(t_{s,1})$. Therefore, calculated by HiSIM, E_{ox} is shifted to $E_{ox}(t_{s,2})$. The threshold voltage shift at $t_{s,2}$ is obtained as $\Delta V_{ths}(t_{s,2})=\Delta V_{th_RLD}[E_{ox}(t_{s,2})]+\Delta V_{th_HT}[E_{ox}(t_{s,2})]$. Under stress bias, ΔV_{th} at i^{th} time point t_i is calculated by accumulating the previous results: $\Delta V_{th}(t_i)= \Delta V_{ths}(t_{s,1})+\Delta V_{ths}(t_{s,2})+\ldots+\Delta V_{ths}(t_{s,i})$.

Under the recovery condition, since the recovery model parameters are insensitive to E_{ox}, ΔV_{th} recovery is calculated using (3) and (5) with the integrated recovery time ($t_{r,i}=t_{r,i-1}+\Delta t$), where $t_{r,i}$ and $t_{r,i-1}$ are the recovery time at i^{th} and $(i\text{-}1)^{th}$ step. ΔV_{th} during recovery is written as $\Delta V_{thr}(t_i)=\Delta V_{th_rec}(t_{r,i})$.

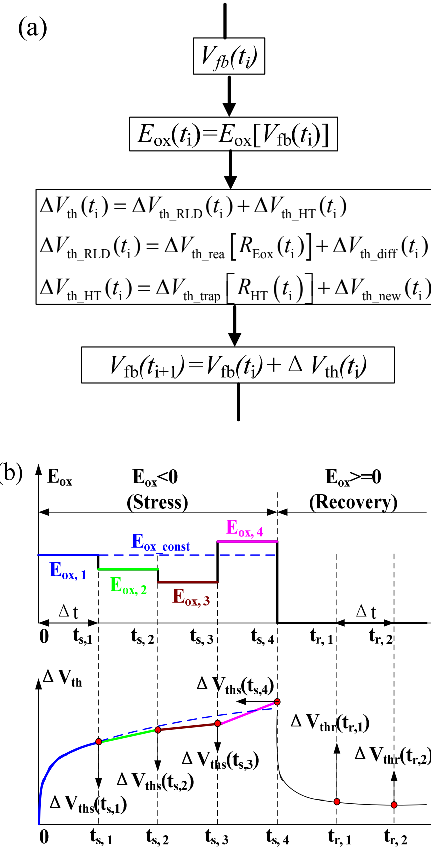

Figure 4. (a) Flow chart of the flat band voltage ($V_{fb}(t_i)$) at i^{th} time point (t_i). (b) ΔV_{th} under various $E_{ox,i}$. Stress and recovery are distinguished by (-/+)E_{ox}. At i^{th} stress time step (t_{si}), $\Delta V_{th}(t_i)$ is calculated as a function of $E_{ox,i}$ and $t_{s,i}$ by using the developed NBTI stress model ($\Delta V_{th}(t_i)=\Delta V_{th_str,i}=\Delta V_{th_str}(E_{oxi}, t_{si})$, where $\Delta V_{th_str,i}$ is stress induced ΔV_{th}). When time changes to $t_{s,i+1}$ ($=t_{si}+\Delta t$)) and E_{ox} changes to $E_{ox,i+1}$, ΔV_{th} is calculated based on the previous result ($\Delta V_{th_str,i}$) as $\Delta V_{th}(t_{i+1})=\Delta V_{th_str,i}+\Delta V_{th_str,i+1}(E_{ox,i+1}, t_{s,i+1})$.

In addition to conventional DC measurements (Figs. 1 and 3), measurements of the frequency dependent ΔV_{th} feature transient stress/recovery characteristics. Measured results of the frequency dependency of ΔV_{th} [12] are compared with model results and good agreement is obtained (Fig. 5a). With the extracted model parameter values from Fig. 1 and 3, the frequency dependence of RLD, HT as well as unified NBTI model is shown in Fig. 5b, separately. With increased frequency of stress/recovery, the decreased recovery time in each duty cycle results in a reduction of the recoverable and increase of the unrecoverable components of ΔV_{th}. Therefore, the minimum ΔV_{th} (ΔV_{th_min}: unrecoverable ΔV_{th}) increases. While the difference between the maximum (ΔV_{th_max}: without recovery) and ΔV_{th_min} decrease.

Fig. 6a shows simulated delays (t_{delay}) of a resistive-load inverter with the supply voltage V_{dd}=1.2V and the resistance R=2e5Ω. Due to the V_{th} degradation in the p-MOSFET, the delay time (t_{delay}) of the rise-edge is larger than that of the fall-edge. Since the circuit performance degradation induced by NBTI effect is mainly due to the unrecoverable component, which is demonstrated to increase with the increased

frequency (Fig. 5), the increase of t_{delay} is observed with the increased input (V_{in}) frequency. Then the duty cycle is changed from 100% to 10%. Here the 100% duty cycle indicates DC stress without recovery, and induces the degradation under the worst case (Fig. 6b). With decreased duty cycle, the delay time reduces due to shorter stress time but longer recovery time during each duty.

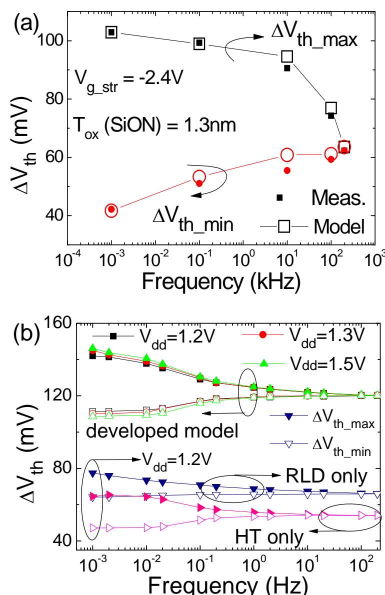

Figure 5 (a) Experimental and model results for AC NBTI degradation data [12]. Model parameters are different from those extracted from Figs. 1 and 2, because the AC data is from different devices. (b) Frequency dependence of the RLD, HT and the unified NBTI model.

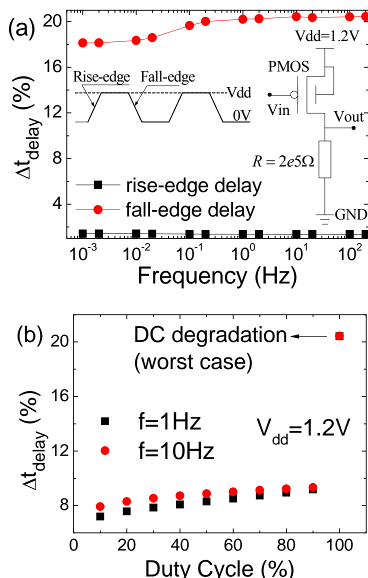

Figure 6 (a) Frequency dependence of the rise-edge and fall-edge delay and (b) duty cycle dependence of the delay time (t_{delay}) in a resistive-load inverter to avoid the impact of an n-MOSFET on t_{delay}. The supply voltage V_{dd}=1.2V. Higher frequency and longer duty cycle result in larger t_{delay}.

IV. CONCLUSION

This work developed a NBTI model valid for any operation condition, considering both the reaction-limited-diffusion and the hole-trapping mechanisms. Circuit simulation, including the device degradation, is realized by implementing the unified NBTI model into the advanced MOSFET model HiSIM. With model parameters extracted from conventional DC measurements, device and circuit degradation under various operating conditions are predicted.

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