

A Comprehensive Solution for Process Variation Characterization and Modeling

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Abstract—The variability issues caused by device scaling require a more comprehensive variation model. A conventional corner model approach that lumps all the variation sources into one corner makes the design sign off extremely difficult for leading edge technology. In this work, the different types of variation sources have been characterized and modeled associated with simulation flow. The impact to the design with different variation combination is also introduced. This is the first time the three types of variation have been fully integrated through compact modeling.

Keywords- Process variation; Monte Carlo; Statistical model; Global variation; Local variation; Correlation; Corner; Distance effect; Spatial effect.

I. INTRODUCTION

A comprehensive variation model is critical to achieve competitive design and manufacturing yield for advanced technologies. Each variation type may have different impacts to circuit performance [1]. Intra-die variations (often referred to as local variation), such as dopant fluctuation and line edge roughness [2], [3], can be cancelled out in critical paths with long stages. As a result, the local variation makes only minor impact for digital-like application. However, for an adjacent pair, the local variation is main source for the mismatch, so a correctly characterized local variation model is very critical to the analog design. Inter-die variation (often referred to as global variation), on the other hand, occurs to all devices in the same die and cannot be cancelled among devices. The inter-die variation that impacts devices globally becomes a dominant factor for the performance of stage delay and is main variation source for digital application. Compared with local variation, the global variation is more related to the concern of yield. In addition to these two types of variation, the amount of variation between two devices may depend on their relative locations in the chip due to the process uniformity. This type of variation requires a different approach to address and may have significant impact on both digital (timing sign-off) and analog (mismatch) design as the variations are spatially correlated. In this work, a novel characterization methodology to distinguish different variation sources is proposed, including test structures and data analysis flow. The new modeling methodology is also developed, especially for the spatial variation modeling. The transistor level model and simulation results are presented and

verified with 28nm technology data. Finally, the impact of the different variation sources and their partition ratio to the circuit are discussed.

II. MODELING METHODOLOGY

According to the nature of technology manufacturing, random process variation can be classified into three categories, local (intra die), global (inter die) and spatial (distance) variations. Since these three types of variation are relatively independent, for a given chip size, the total variation for a single transistor can be expressed as:

$$\sigma_{total}^2 = \sigma_{global}^2 + \sigma_{local}^2 + \sigma_{spatial}^2 \quad (1)$$

Where σ_{global} , local and spatial represent the sigma of global, local and spatial variations respectively. σ_{total} is the total variation observed from a single device. In session A below, the test patterns and characterization flow will be discussed. The modeling methodology will then be discussed in session B.

A. Variation Characterization

Taking the advantage of different variation characteristics, a set of test patterns can be designed specifically to identify the magnitude of variation for the modeling purpose.

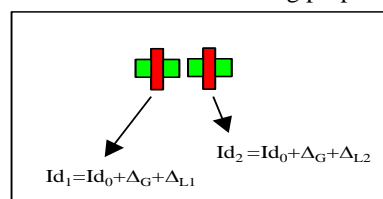


Figure 1. Illustration for the within die mismatch pair test structure. The global variation, ΔG , can be removed by the subtraction between two devices. The $\sigma_{local} = \sigma_{mismatch}/\sqrt{2}$.

Firstly, the local variation, σ_{local} , can be extracted from the mismatch variation of an adjacent device pair as described in Fig.1, $(Id1-Id2)/(Id1+Id2)/2$. Since the distance is negligible between adjacent patterns, no spatial needs to be considered.

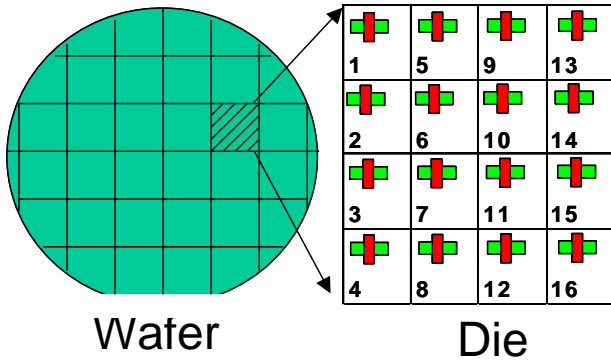


Figure 2. OCV test structure. The identical devices are placed repeatedly over the whole die. The magnitude of mismatch for different distance can be extracted from a given pair of devices. The same set of structure can be also used to define the die median for global variation.

Secondly, due to the random behavior within a die, the local variation can be cancelled among multiple transistors. Consequently, people commonly use an array of N devices to identify global variation. The variation of an array of N devices is equal to

$$\sigma_{array}^2 = \sigma_{global}^2 + \sigma_{local}^2/N + \sigma_{spatial}^2 \quad (2)$$

Although the local variation can be reduced by the array structure, the spatial variation still exists. As a result, there is a new set of test pattern needed to resolve this issue. We propose an OCV (On-Chip Variation) structure shown in Fig.2 to separate the global and spatial variations. The OCV structure consists of a set of identical patterns placed at multiple sites within a die. The proximity environment of each transistor is also maintained the same for the variation characterization. The mismatch between any two devices in the structure can be measured without the influence of global variation.

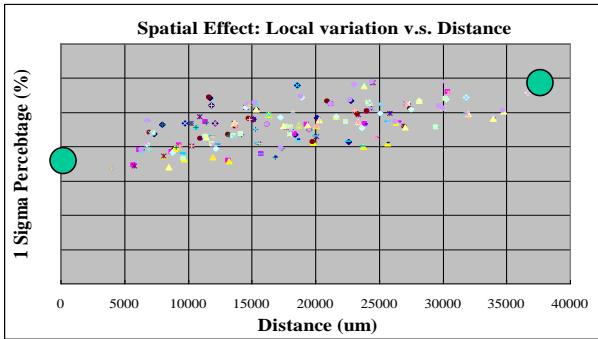


Figure 3. Data collected from OCV structure. Each small dot represents the sigma of delta (Id1-Id2)/average(Id1+Id2). The circle A at distance=0 is consistent with the σ_{local} extracted from mismatch pair. The circle B at distance=37500um can be used to extract $\sigma_{spatial}$.

The results shown in Fig. 3 are 28nm technology data. We plotted the sigma of local variation versus distance between two devices. Each data point represents the sigma of delta between two identical devices measured across the wafer. The

extracted variation can be defined as σ_{OCV} that includes the pure local variation and spatial variation as following:.

$$\sigma_{OCV}^2 = \sigma_{local}^2 + \sigma_{spatial}^2 \quad (3)$$

The sigma of delta between closest pair (dot at distance=0) can be benchmarked with conventional local variation patterns, σ_{local} . In addition, the pure spatial effect variation, $\sigma_{spatial}$, can then be evaluated from the longest distance pair (data at distance=37000um, circle-B). Once we know $\sigma_{spatial}$, the global variation can be obtained from the following equation:

$$\sigma_{global}^2 = \sigma_{total}^2 - \sigma_{local}^2 - \sigma_{spatial}^2 \quad (4)$$

If we sum up all the devices in the OCV structure and take the median (call this parameter OCV median) for each die, the local and spatial variation will be mostly cancelled out in OCV median due to random variation among multiple devices and locations respectively. Thus, global variation can also be calculated from the sigma of the OCV median. This is another way to confirm the number obtained from Eq. (4) for global variation. In other words, the OCV test structure can serve as unified test patterns for local, global and spatial variation extraction.

B. Modeling and Simulation Methodology

The local variation model can be implemented based on $1/\sqrt{\text{area}}$ scaling [4]. However, the capability of scaling is highly process dependent and it may reach some lower bound for the extremely large devices and never go through the origin point. The variation cancellation effect for the long path circuit or mismatch for analog-like application can be reflected through Monte Carlo simulation. The global variation is modeled either by a conventional corner or Monte Carlo approach. While doing Monte Carlo simulation for global variation, all the devices share the same set of random numbers in one Monte Carlo run. As a result, there is no more cancellation happened while the number of transistors increasing. In addition to the well defined local and global variation, the nature of spatial variation lies between global (dependent) and local (independent) variations. We describe the random variation between two devices for spatial effect as below:

$$\begin{aligned} dev1_ran &= dev1_ran; \\ dev2_ran &= R(dis) \times dev1_ran + \sqrt{1-R(dis)} \times dev2_ran; \end{aligned} \quad (5)$$

Where $dev1_ran$ and $dev2_ran$ are two independent random numbers for two devices and the sigma of random number is equal to $\sigma_{spatial}$. $R(dis)$ is a function of distance representing the spatial correlation coefficient between two transistors. To include the spatial effect, we modify the variation of the two random numbers as $dev1_ran$ and $dev2_ran$ for $dev1_ran$ and $dev2_ran$ respectively. Note that the sigma magnitude of each random is unchanged after this modification. However, when the mismatch between the two devices is considered, the spatial correlation of the two devices is linked through R. Neither local nor global variation can describe the spatial variation precisely.

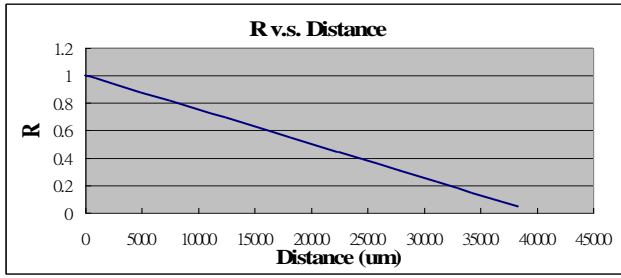


Figure 4. R v.s. Distance. For adjacent paired devices, the R is equal to 1. On the other hand, the R is close to zero for the longest paired device. Namely, the smaller R is, the larger spatial effect is observed.

Assume the R is a linear function of distance as shown in Fig. 4. For an adjacent paired devices, $R=1$ and two devices share the same random number for spatial effect, so the spatial effect is supposed to be cancelled as mismatch pair discussed in Fig. 1. There is only local variation, σ_{local} between two devices. On the other hand, R is close to 0 for a longer distance paired device, so two devices are with two different random numbers for spatial effect. As a result, there will additional spatial effect between two devices. The extreme value of variation is at $R=0$ and is supposed to be equal to σ_{OCV} as expressed in Eq. (3).

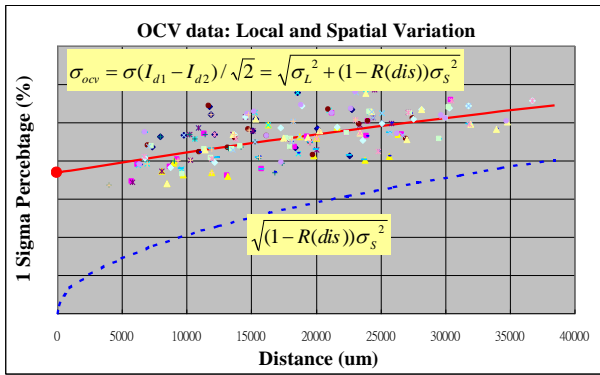


Figure 5. The on-chip-variation (OCV) fitting results base on proposed distance correlation equation. The case of $R=1$ is for the closest pair. The variation is equal to the conventional mismatch pattern without spatial effect. The case of $R=0$ is for longest distance pair. The spatial effect is observed.

We fitted the OCV data based on linear R assumption mentioned above. As shown in Fig. 5, the solid line, which considered the local and spatial variation together, can fit the OCV variation data well. By taking out the local variation from solid line, the dash line represents the spatial effect only. Due to the distance dependent R, the final spatial variation represented by dash line becomes distance dependent. For the case of distance=0, the variation is equivalent to the conventional mismatch pattern without additional spatial effect. At the longest distance, an additional spatial effect is observed and modeled by the proposed equation.

To extend the correlation for the multiple devices, a correlation matrix is introduced. The correlation matrix can keep the

magnitude of sigma for each random number unchanged, but the correlation for any given two devices can be added [5]. However, it's impractical to build a correlation matrix for every device pair in the circuit. In our example, we divide a chip into a few zones as shown in Fig. 6. Only devices between different zones have spatial variation ($R<1$). The correlation matrix between zones has the form as shown in Fig. 6. The R_{ij} describes the random number dependence and can be obtained from curve shown in Fig. 4.

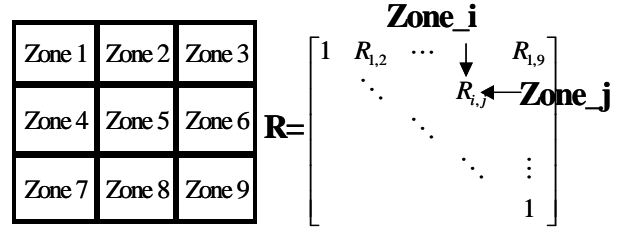


Figure 6. The area partition for layout extraction tool. The correlation matrix can be used to describe the random number dependence among different zones. R_{ij} represents the correlation coefficient between two zones. The value of R_{ij} can be obtained from Fig. 4 based on the given distance.

III. IMPACT ON CIRCUIT DESIGN

Two cases are discussed in this session. The first case focuses on the timing skew between paired delay chains. Namely, it is to discuss the mismatch for the path. The second case is to define a correct 3-sigma corner for delay chain due to additional spatial effect. The impact from each variation component will be discussed in the following two examples.

A. Example I: Timing skew within two delay chains.

The timing skew between two clock trees is important for sign off. Traditionally, only local and global variations are considered [6], and a guard band is used to cover the spatial effect. However, it's difficult to define an optimized guard band. Based on the methodology discussed above, the timing skew between two paths can be expressed as the following:

$$\sigma(\text{delay1} - \text{delay2}) = \sqrt{\frac{2\sigma_{local}^2}{N} + (2 - 2R) \cdot \sigma_{spatial}^2} \quad (6)$$

Where σ_{local} , $\sigma_{spatial}$ and R can be extracted from test patterns described above, N is the number of transistors and global variation has been cancelled between two paths. To validate this model, a group of 101-stage delay chains are selected and placed all over a chip at multiple sites. The delay delta between two delay chains is simulated and compared with measured data. The comparison results for two types of circuits, INV and NAND delay chain, are shown in Fig.7. The delay skew between two paths caused by local variation is greatly reduced due to multiple devices within each path. For the two paths nearby, the spatial effect is negligible because of strong spatial correlation ($R=1$). On the contrary, for the two paths with distance, the spatial effect exists and can be modeled by R. The correlation is weak ($R=0$) for the longest distance case. As

a result, even with a long stage, the variation skew won't be cancelled as people used to think. The skew still exists due to the spatial effect. It increases obviously when the distance increase.

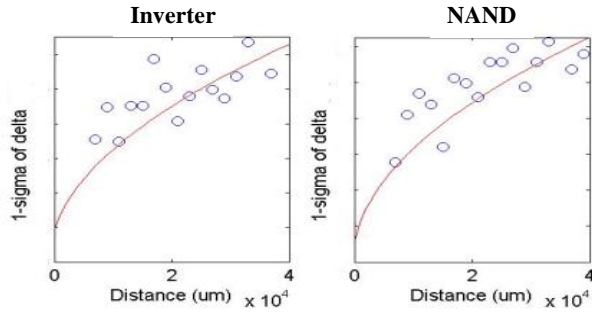


Figure 7. The fitting result for timing skew variation v.s. distance between two paths. Two examples, inverter and NAND delay chains are presented here. The local and global variation have been greatly reduced and subtracted respectively. The timing skew is mainly caused by spatial variation. The delta of sigma is getting larger along with the distance.

B. Example II: Delay time variation for a delay chain

In this case, we'd like to define a correct 3sigma variation. If the whole delay chain is placed across the different zones. The correlation coefficient R among different transistors is 0 ~ 1 as described in Fig. 4. The spatial variation is dependent on R and local variation reduction is dependent on number of stage N. However, if the whole delay chain is located within the same zone, the R is equal to 1 and the variation is as the following:

$$\sigma(\text{delay}) = \sqrt{\sigma_{\text{global}}^2 + \sigma_{\text{spatial}}^2 + \frac{\sigma_{\text{local}}^2}{N}} \quad (7)$$

In other words, the spatial effect becomes another global variation without any cancellation. The additional margin is definitely needed for the design sign-off, since this variation cannot be reduced along with the number of stage. Assume the same amount of 5% σ_{global} , σ_{local} and σ_{spatial} effect is applied to two types of circuits as shown in Fig. 8. An additional 3% for 3-sigma corner is required to cover the non-cancelled spatial effect for type A circuit compared with type B circuit. This is another example to show the importance of variation analysis.

In summary, the mismatch caused by the local variation can be reduced by a group of multiple devices as described in two examples above. In addition to the local variation, the global variation is the core variation for the digital application. It is always there for a single path, but can be removed while evaluating the path skew for the two paths as discussed in the first example. Finally, the spatial effect is a challenge for modeling. It behaves more like a "local variation" while talking the mismatch of two paths for timing skew analysis in the

example I. However, for a given short path, the spatial effect behaves more like an additional global variation that cannot be cancelled as discussed in example II.

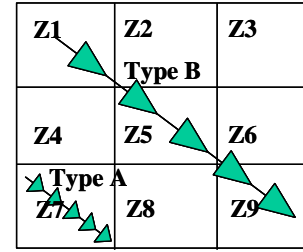


Figure 8. Type A and B delay chains. A 9X9 correlation matrix as shown in Fig.6 is needed to describe the correlation among different zones. For a short path like type B, the spatial effect can not be cancelled, so the spatial effect acts like an additional global variation. An additional guardband is needed compared with type B circuit.

IV. CONCLUSION

In this work, a comprehensive characterization and modeling approach have been proposed for three types of variation. The spatial effect modeling especially needs an extra attention due to the necessity of correlation matrix. The methodology has been verified with 28nm technology data. It demonstrated that significance of variation model to the circuit performance.

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