Impact of Single Trapped Charge in Gate-All-Around Nanowire Channels Studied by Ensemble Monte Carlo/Molecular Dynamics Simulation

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Abstract—**Impact of a single trapped charge in an oxide layer on the carrier transport is numerically investigated for gate-all-around nanowire (GAA NW) channels, using the ensemble Monte Carlo / molecular dynamics simulation. The relative amplitude of current reduction caused by a single trapped charge increases in smaller NWs. This is due to the closer mean distance of carriers and the trapped charge in a downsized device, resulting increased impact of Coulomb scattering from the trapped charge to carriers. Under the same trap density, however, the smaller NWs show a decreasing tendency of the relative amplitude of current reduction if the current per NW is the same. Even in the practical operation conditions in which the current density per unit width is kept constant for each channel diameter, the relative amplitude of current reduction does not depend on the NW diameter. This indicates that the impact of the trapped charge on the relative amplitude of current reduction is determined by the trap density.**

Keywords-component; enesmble Monte Carlo/molecular dynamics (EMC/MD), MOSFETs, gate-all-around nanowire, random telegraph noise.

I. INTRODUCTION

Gate-all-around nanowire (GAA NW) Si MOSFETs are becoming more of interest as promising building blocks for future Si CMOS technology, owing to their excellent gate controllability and current drivability. The variability in device performance and noise in current are considered to be the critical issues in the practical implementation. Random telegraph noise (RTN) due to capture and emission of carriers via traps in an oxide is one of the largest concerns because it becomes more prominent as the transistor dimensions are downsized [1,2]. Many studies have reported on the effects associated with a single trapped charge in deep submicron planar MOSFETs [1-4]. RTN on GAA NW MOSFETs has been demonstrated experimentally [5-7]. There are, however, little efforts on modeling and simulating regarding RTN amplitudes in the GAA structures.

In this work, the impact of a single oxide-trap charge on the channel current in GAA NWs is investigated, using the ensemble Monte Carlo / molecular dynamics (EMC/MD) simulation [8,9]. The amplitudes of RTN and the contribution of scattering from a trapped charge have been estimated in thin NW channels.

II. SIMULATION METHOD

A. Ensemble Monte-Carlo / Molecular Dynamics Method

Carrier transport is simulated by the EMC/MD method [8,9]. The scattering processes considered in this method are illustrated in Fig. 1. Carriers are treated as classical particles, and their real-space trajectories under the Coulomb point-to-point potentials are calculated by the MD algorithm. The acoustic and optical phonon scatterings are taken into account as stochastic changes in the momentum of carriers according to the standard energy-dependent formulations based on the Fermi golden-rule-type approach in the bulk band structure. Six equivalent X-valleys of conduction bands are expressed by an ellipsoidal non-parabolic band mode, which is represented as

$$E(1+\alpha E)=\frac{\hbar^2}{2}\left[\frac{(k_x-k_{x0})^2}{m_x}+\frac{(k_y-k_{y0})^2}{m_y}+\frac{(k_z-k_{z0})^2}{m_z}\right] \quad (1)$$

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where m_x, m_y, and m_z are the effective masses for x, y and z axes, respectively. The effective masses comprise two transverse effective masses: $m_t = 0.19m_0$, and one longitudinal effective mass: $m_l = 0.98m_0$, where m_0 is the electron rest mass. k_{x0}, k_{y0}, and k_{z0} are a set of the wave vectors at the center of X-valley coordinates, which gives the lowest value in electron energy. α (= 0.5 eV^{-1}) is a nonparabolicity parameter.

B. Device Model

The simulated GAA Si NW channel model is shown in Fig. 2. The NWs have a circular cross section with a diameter of 7.07 and 14.1 nm, respectively. The length of channels is 50 nm. A periodic boundary condition is imposed along the channel direction. Since, intrinsic channels are adopted for practical NW transistors, a channel, in this study, is treated as undoped, and only conduction electrons are considered as carriers. The simulation conditions and the number of carriers are also listed in Fig. 2. A negative point charge is placed outside the channel as a single trapped charge in the first oxide layer, 0.2 nm away from the interface of Si channel and the insulator oxide.

A potential along the cross sectional direction is introduced in order to reproduce the carrier confinement effect in the GAA structure to be considered (Fig. 3). The potential function is described in the following eqs. (2)-(4):

$$V(r) = -\frac{2k_bT}{q}\left[\ln\left[\sin\left(\frac{\pi}{\phi}(r+\frac{\phi}{2})\right)\right] + \ln\left[\exp\left(-\frac{b_0}{\phi}(r+\frac{\phi}{2})\right)+\exp\left(\frac{b_0}{\phi}(r-\frac{\phi}{2})\right)\right] + \ln\left(\frac{a_0}{\sqrt{2\phi}}\frac{N_{inv}}{n_i}\right)\right] \quad (2)$$

where ϕ is the channel diameter, r is a position along channel diameter, q the elemental charge, k_B the Boltzmann constant, T the temperature, n_i the intrinsic carrier density of Si, and N_{inv} the sheet charge density of the 2D channel. The potential function, V(r), was originally formulated for the 2D channel of gate FETs [10], and the effect of the gate bias is reflected through a parameter N_{inv}. a_0 and b_0 are parameters obtained by eqs. (3) and (4):

$$a_0 = 2\left[2\exp(-b_0)+\frac{\pi^2(1-\exp(-2b_0))}{b_0(b_0^2+\pi^2)}\right]^{-\frac{1}{2}} \quad (3)$$

$$b_0 = \phi\left[\frac{qm^*\pi^2}{4\varepsilon_{Si}\hbar^2}\left(\frac{5}{6}qN_{inv}\right)\right]^{\frac{1}{3}} \quad (4)$$

where ε_{Si} the permittivity of Si, $\hbar$ the Dirac constant , and m^* the electron effective mass.

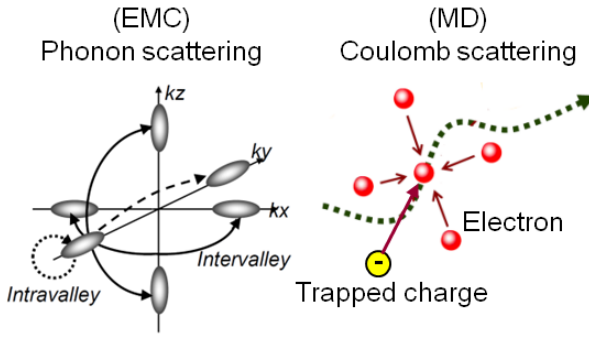
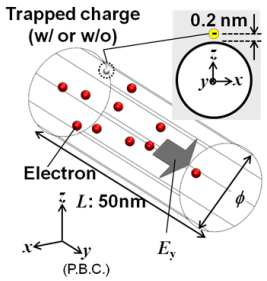


Fig. 1. Scattering processes considered in the EMC/MD method: (1) phonon scattering based on EMC algorithm, and (2) Coulomb scattering among the point charges based on MD algorithm.



Channel diameter	Number of electron in channel	Carrier density	
ϕ(nm)	N_{ele}	n_e (cm^{-3})	N_{inv} (cm^{-2})
7.07	5	2.55×10^{18}	4.50×10^{11}
	15	7.64×10^{18}	1.35×10^{12}
	30	1.53×10^{19}	2.70×10^{12}
	75	3.82×10^{19}	6.75×10^{12}
14.1	5	6.37×10^{17}	2.25×10^{11}
	15	1.90×10^{18}	6.75×10^{11}
	30	3.82×10^{18}	1.35×10^{12}
	75	9.55×10^{18}	3.38×10^{12}

Fig. 2. Simulated gate-all-around channel model and simulation conditions. 1D periodic boundary condition is imposed along the channel.

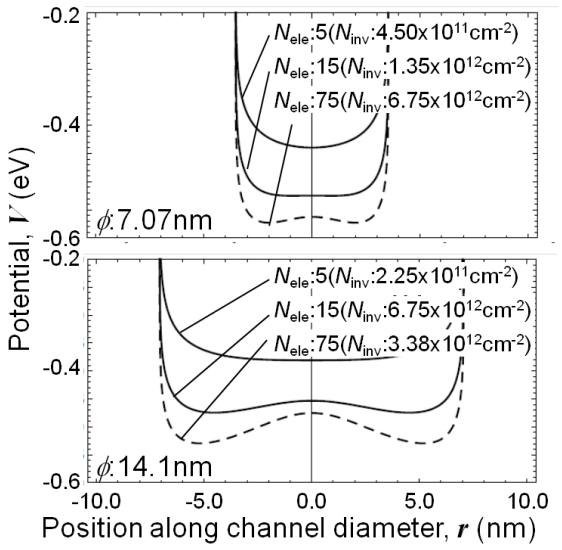


Fig. 3. Potential profiles along the channel diameter.

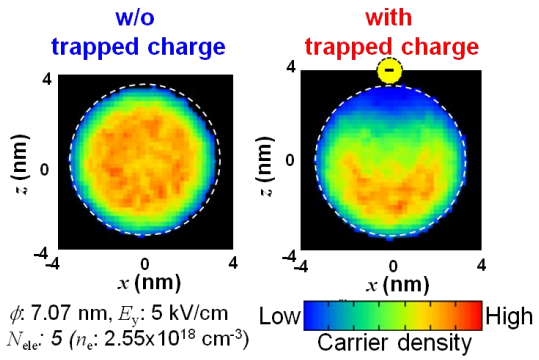


Fig. 4. Carrier distribution at the cross section of the channel without and with a single trapped charge.

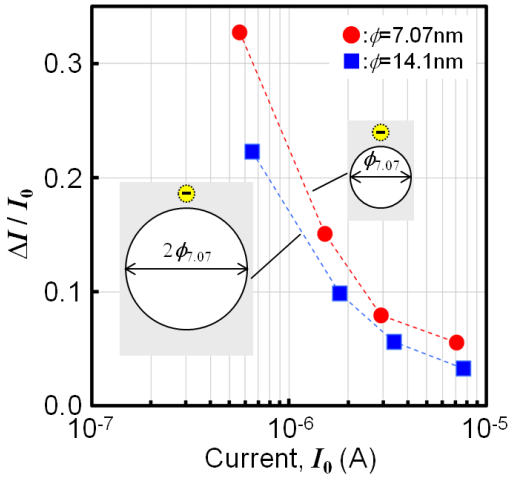


Fig. 5. Relation between the relative amplitude of current reduction and the current. I_0 denotes the mean current in case without a trapped charge.

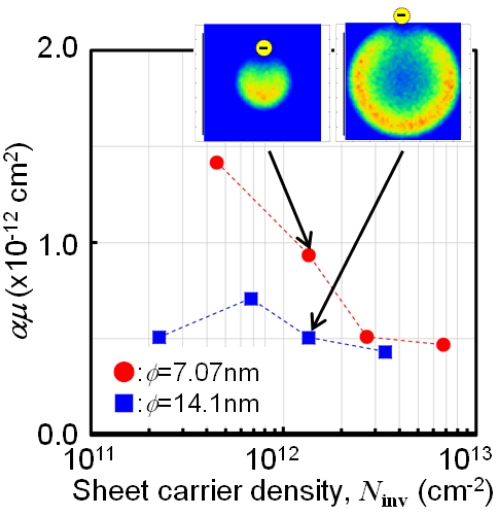


Fig. 6. Relation between the mobility fluctuation term ($\alpha\mu$) and the sheet carrier density. The insets shows carrier distributions for each NW.

The carrier transport with and without a trapped charge is simulated, respectively. The channel current under the constant electric field of 5 kV/cm along the channel is estimated by counting the number of carriers passing through the cross section of the simulated NW per unit time. The difference in the mean current between the above two cases is used for estimating the impact of the trapped charge on the carrier transport.

III. Results and Discussion

A. Carrier Distribution

Fig. 4 shows the carrier distributions at the cross section of the channels without and with a single trapped charge. Carriers are clearly repelled from the trapped charge and redistributed to the opposite side. Note that the carrier density decreases in a whole cross section of the NW with a trapped charge, which means that the mean current flow through the NW is reduced by the trapped charge.

B. Relative Amplitude of the Current Reduction

Fig. 5 shows the changes in the mean currents with and without a trapped charge (ΔI) for each diameter of NW. ΔI is normalized by the mean current without a trapped charge (I_0) to give the relative amplitude of the current reduction ($\Delta I/I_0$). $\Delta I/I_0$ decreases with increase in I_0 because the Coulomb potential of the trapped charge is shielded by the carriers. $\Delta I/I_0$ increases as the channel diameter decreases, indicating that the impact of a single trapped charge becomes significant in smaller NWs.

C. Mobility Fluctuation

The effect of a trapped charge on the carrier mobility is also estimated in this study. Fig. 6 shows the scattering coefficient (α) multiplied by the carrier mobility (μ): $\alpha\mu$, as a function of N_{inv}. The following theoretical relation for a RTN amplitude generated by a single trapped charge in a planar-structure MOSFET [11] is used for calculating $\alpha\mu$.

$$\frac{\Delta I}{I_0} = \frac{1}{LW}\left(\frac{1}{N_{inv}} + \alpha\mu\right) \qquad (5)$$

where L is the channel length. Since eq. (5) is originally formulated for the planar-structure, parameters W and N_{inv} are modified to those in the cylindrical coordinate. We set W to the channel perimeter $\pi\phi$, and N_{inv} to the number of carriers per surface area of each NW [6,7]. The term, $\alpha\mu$, indicates the contribution from the mobility fluctuation to the relative amplitude of the current reduction. The mobility fluctuation is enhanced in the smaller NW channel. This indicates that the scattering effect due to a single trapped charge is significant even with a GAA structure, because the average distance between carriers and a trapped charge is reduced in a downsized device.

D. Relative Amplitude of the Current Reduction under the Same Trap Density

The impact of trapped charges on the relative amplitude of the current reduction is investigated making the number of the trap the same areal density in the NW surface. Fig. 7 shows $\Delta I/I_0$ normalized by the surface area of each NW. As shown in Fig. 7(a), the normalized amplitude in the smaller NW has

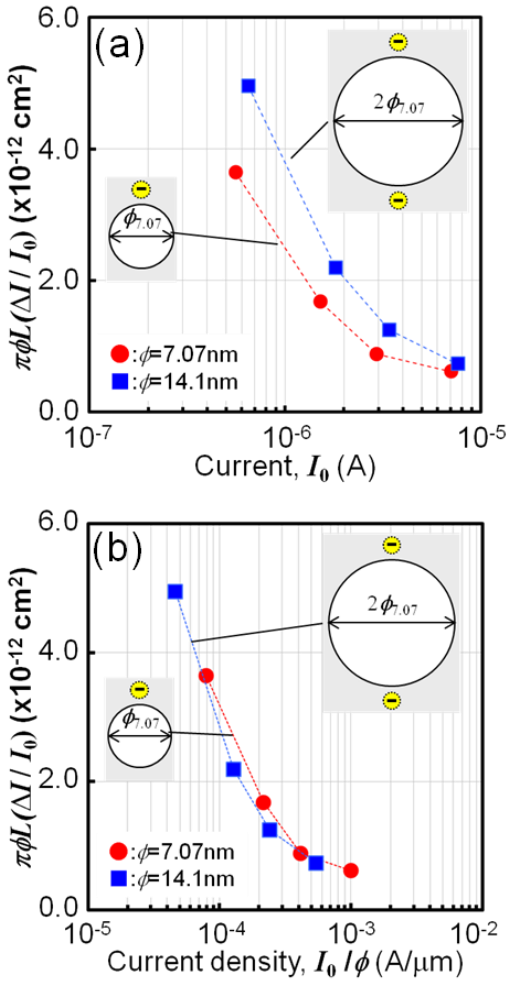


Fig. 7. I/I_0 normalized by surface channel area as a function of (a) current and (b) current density per unit width. I_0 denotes the mean current in case without a trapped charge.

smaller value at each current. This indicates that, if the same current flows in each channel, the smaller NW has the immunity for the RTN amplitude under the same density of trap charges.

In the practical operation condition, the current density per unit width is kept constant with scaling. Fig. 7(b) shows the $\Delta I/I_0$ normalized by the surface area of NW as a function of the current density per diameter. Note that similar dependences of the normalized $\Delta I/I_0$ are found for both channel diameters, indicating that the impact of a trapped charge is determined by the trap density. The result suggests that the small NW has no disadvantage on the impact of trapped charges under the practical implementation.

IV. Summary

Carrier transports in GAA Si NW channels with and without a single trapped charge in an oxide layer is numerically investigated by the EMC/MD simulation. The impact of a single trapped charge increases with downsizing channel diameters, due to the increasing impact of Coulomb scattering effect from a trapped charge to carriers as a result of size reduction.

The relative amplitude of the current reduction under the same trap density is also investigated. Assuming the same current per NW, the smaller NW shows a decreasing tendency of the relative amplitude of the current reduction, indicating that the smaller NW has the immunity against the RTN amplitude. In the case of the same current density per unit width, the relative amplitude of current reduction does not depend on channel diameter. This indicates that the impact of trapped charges is determined by the areal trap density.

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References

[1] K. Takeuchi, T. Nagumo, S. Yoko gawa, K. Imai, and Y. Hayashi,, “Single-charge-based modeling of transistor characteristics fluctuations based on statistical measurement of RTN amplitude”, 2009 symposium on VLSI technol. Dig., pp. 54-55, June 2009.

[2] N. Tega, H. Miki, F. Pagette, D. J. Frank, A. Ray, M. J. Rooks, W. Haensch, and K. Torii, "Increasing threshold voltage variation due to random telegraph noise in FETs as gate lengths scale to 20 nm", 2009 symposium on VLSI technol. Dig., pp. 50-51, June 2009.

[3] A. Asenov, R. Balasubramaniam, A. R. Brown, and J. H. Davies, “RTS amplitudes in decananometer MOSFETs: 3-D simulation study”, IEEE Trans. Ele. Dev., vol. 50 no. 3, pp. 839-845, March 2003.

[4] C. L. Alexander, A. R. Brown, J. R. Watling, and A. A.senov, “Impact of single charge trapping in nano-MOSFETs – Electrostatics versus transport effects”, IEEE Trans. Nanotechnol, vol. 4, no. 3, pp.339-344, May 2005.

[5] Y. F. Lim, Y. Z. Xiong, N. Singh, R. Yang, Y. Jiang, D. S. H. Chan, L. K. Bera, G. Q. Lo, N. Balasubramanian, and D. –L. Kwong, “Random telegraph signal noise in gate-all-around Si-FinFET with ultranarrow body”, IEEE Ele. Dev. Lett. vol. 27, no. 9, pp. 765768, September 2006.

[6] B. H. Hong, L. Choi, Y. C. Jung, S. W. Hwang, K. H. Cho, K. H. Yeo, D.-W. Kim, G. Y. Jin, D. Park, S. H. Song, Y. Y. Lee, M. H. Son, and D. Ahn, “Temperature dependent study of random telegraph noise in gate-all-around PMOS silicon nanowire field-effect transistors”, IEEE Trans. Nanotechnol., vol. 9, no. 6, pp. 754-758, November 2010.

[7] R. H. Baek, H. S. Choi, H. C. Sagong, S. H. Lee, G. B. Choi, S. H. Song, C. H. Park, J. S. Lee, Y. H. Jeong, C. K. Baek, D. M. Kim, Y. Y. Yeoh, K. H. Yeo, D. -W. Kim, and K. Kim, "Characterization of Gate-All-Around Si-NWFET, including Rsd, cylindrical coordinate based 1/f noise and hot carrier effects", Proc. IEEE Int. Reliability Phys. Symp., pp. 94-98, May 2010.

[8] C. Jacoboni and L. Reggiani, "The Monte Carlo method for the solution of charge transport in semiconductors with applications to covalent materials", Rev. Mod. Phys. vol.55, no.3, pp.645-705, July 1983.

[9] Y. Kamakura, H. Ryouke, and K. Taniguchi, "Ensemble Monte Carlo/Molecular Dynamics Simulation of Inversion Layer Mobility in Si MOSFETs--Effects of Substrate Impurity", IEICE Trans. Electron., vol.E86-C, no.3, pp. 357-362, March2003.

[10] L. Ge and J. G. Fossumet, “Analytical modeling of quantization and volume inversion in thin Si-film DG MOSFETs”, IEICE Trans. Ele. Dev., vol. 49, no. 2, pp. 287-294, Feburary 2002.

[11] K. K. Hung, P. K. Ko, C. Hu, and Y. C. Cheng, “A unified model for the flicker noise in metal-oxide-semiconductor field effect transistors”, IEEE Trans. Ele. Dev., vol. 37, no. 3, pp. 654-665, March 1990.