Monte Carlo Simulation of Program Disturb in Contact-Less Virtual Ground NOR Flash Memory

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***Abstract*—Program disturb phenomenon observed in contact-less virtual ground NOR Flash memory is investigated through the numerical simulations. The hot electron behaviors inside the memory cell structures are simulated with Monte Carlo simulators for Si and SiO_2 regions. It is suggested that the electron transport across the SiO_2 region can be attributed to the mechanism for the unintended programming to the adjacent memory cell.**

Keywords-NOR Flash memory, virtual ground architecture, program disturb, Monte Carlo simulation, hot electron transport

I. INTRODUCTION

To realize a higher-density NOR-based Flash memory, virtual ground array (VGA) architectures have been reported so far [1,2]. In this structure, as illustrated in Fig. 1, the significant area scaling benefit is achieved by replacing the drain contacts and metal interconnect in the array with a buried bitline diffusion implant. However, one of the critical issues recognized as a barrier for reducing the cell size is the program disturb phenomenon shown in Fig. 2; the adjacent unselected cell is also programmed during the hot-electron writing of the selected bit. Since the mechanism of this disturb has not been fully clarified yet, this work reports the numerical simulations to investigate the hot-electron behaviors inside the cell structure. Monte Carlo (MC) simulations are carried out in the Si channel and SiO_2 regions, and a new mechanism responsible for the program disturb in VGA-NOR Flash memory cell is discussed.

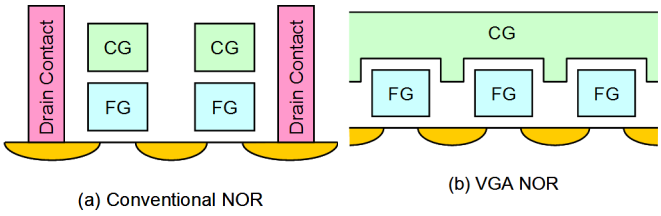

Figure 1. Cross-sectional view of (a) the conventional NOR type Flash memory and (b) the contact-less virtual ground array(VGA)-NOR Flash memory cell [2].

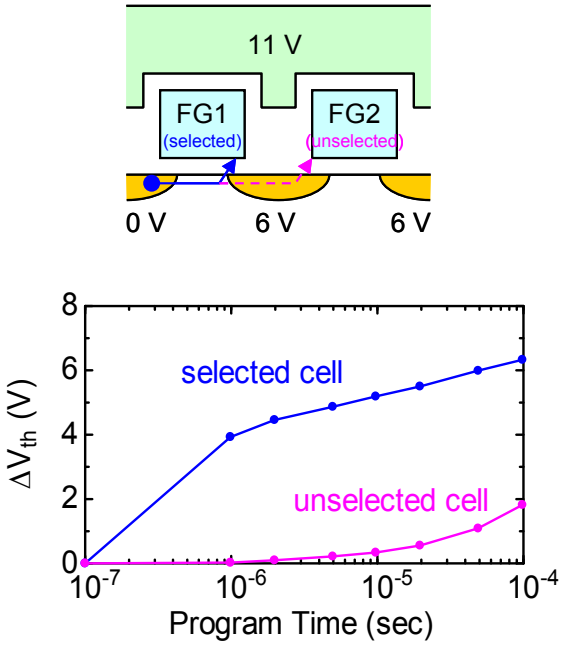

Figure 2. Program disturb phenomenon observed in VGA-NOR Flash memory. The threshold voltage in the selected cell (FG1) and the unselected cell (FG2) are plotted as a function of program time.

II. SIMULATION METHOD

Using a single-particle frozen-field MC approach [3], we investigated the hot electron transport inside the cell structure shown in Fig. 3. Two adjacent memory cells, which share the same bitline diffusion region, were considered. In this study, the potential distributions in this system under various bias conditions were firstly calculated by the hydrodynamic device simulator *HyENEXSS* [4]. In order to make contacts to each diffusion region, three-dimensional simulations had to be carried out. Figure 4 shows an example of the calculated potential distribution in the plane at $z = 0$. Then, the electron transport under the electric field extracted from the potential gradient was simulated by MC method. The simulation inside

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the Si region was performed by using the full-band MC approach [5], while the analytical band MC method [6] was employed for the electron transport in SiO_2.

III. Results and Discussion

Figure 5 shows the hot electron trajectories in the Si region simulated by the full-band MC method. After accelerated in the channel of the selected cell, the hot electrons were quickly relaxed in the drain, and at the floating gate edge of the adjacent cell, they no longer had sufficient energies to surmount the SiO_2 barrier. Thus, in this study, we considered the possibility of the program disturb mechanism due to the electron transport across the SiO_2 region.

Figure 6 illustrates the simulation method to verify this mechanism, and the simulation results are shown in Fig. 7. To take into account the potential distribution varied with program time, we carried out the simulations applying various voltages to the floating gate of the selected cell (FG1). Note that the electron trajectories in SiO_2 are strongly affected by the bias condition, i.e., the potential distribution. At the initial stage of the programming (Fig. 7a), the electric field around FG1 edge is so weak that most electrons diffused back to the drain, or otherwise were absorbed to FG1. However, supposing the reduction of FG1 voltage due to charging effect (Fig. 7b), the modulation of the electron trajectories was observed, and a portion of electrons were injected to the adjacent floating gate (FG2). This could be understood by looking at the gradients of the potential distribution.

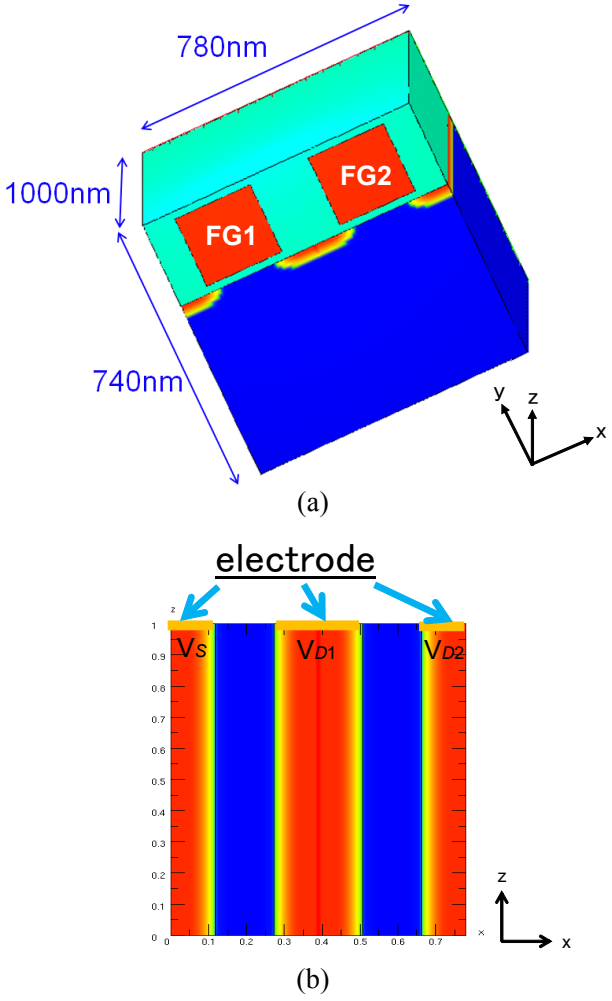

Figure 3. Device structure simulated using the 3D device simulator *HyENEXSS* [4]. The potential distributions under various bias conditions were computed, and the results were used as the input data for the frozen-field MC simulation to investigate the hot electron trajectories. (a) The 3D view. Control gate (CG) is not shown. The source/drain contacts were placed at the back side. (b) The cross-sectional view at the Si/SiO_2 interface.

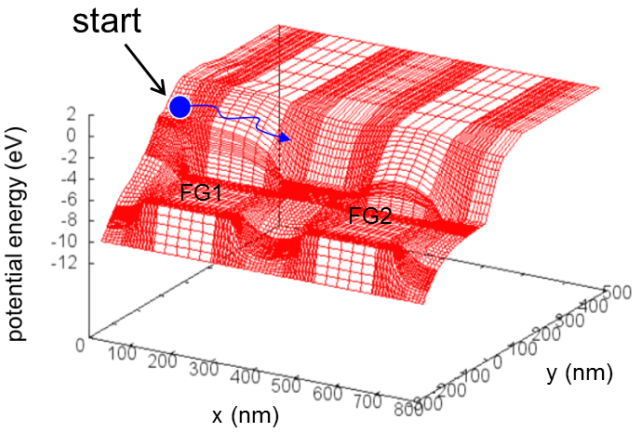

Figure 4. Potential energy distribution in the structure shown in Fig. 3 calculated by *HyENEXSS*. The distribution in the plane at $z = 0$ is plotted. The bias voltages are $V_S = 0$ V, $V_{D1} = V_{D2} = 6$ V, and $V_{CG} = 11$ V. The hot electron trajectories started from the point indicated by an arrow were simulated by the MC method.

Figure 8 shows the relative percentages of the terminals where the injected electrons were finally absorbed. The electrons injected at FG1 edge can reach to FG2 after the programming of FG1 is progressed; this is consistent with the experimental observation shown in Fig. 2. Although the mechanism due to the channel initiated secondary electrons, which has been suggested to explain the similar phenomena [7], could be another hypothesis, the possibility of the electron transport across SiO_2 should be considered to explore the origin of the disturb mechanism.

IV. Summary

Program disturb phenomenon in contact-less virtual ground NOR Flash memory has been investigated through the numerical simulations, and the possible mechanism has been discussed. The frozen field MC simulations have been performed to observe the hot electron behaviors in Si and SiO_2 regions, which suggested that the electron transport across the SiO_2 region can be attributed to the mechanism for the unintended programming to the adjacent memory cell.

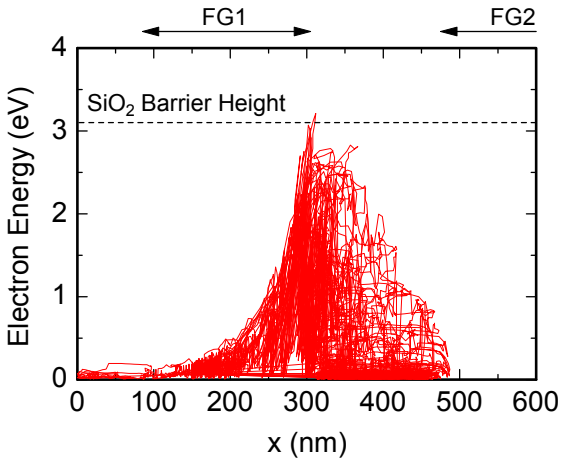

Figure 5. Trajectories of 1,000 electrons potted on a kinetic energy vs. x plane simulated using full-band Monte Carlo Method in Si substrate. The dashed line shows SiO_2 barrier height energy $q\phi_B = 3.1$ eV.

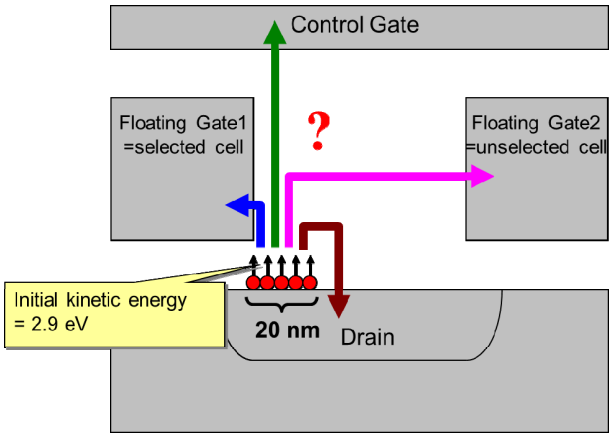

Figure 6. Schematic view of the simulation model for pursuing the electron trajectories after injected into SiO_2. 1,000 electrons were initially put at the drain edge region with a width of 20 nm, and then their trajectories were tracked until they reach any of the terminals (FG1, FG2, CG, or drain). The initial kinetic energy of $q(V_d - \phi_B) \sim 2.9$ eV was assumed.

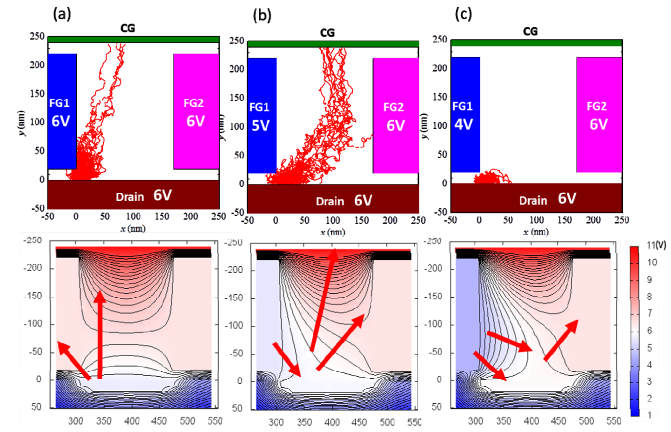

Figure 7. Results of the frozen-field Monte Carlo simulation for the electron transport in SiO_2 region. The bias conditions assumed were $V_{D1} = 6$ V, $V_{CG} = 11$ V, and $V_{FG2} = 6$ V, and V_{FG1} was varied from 6 V to 4 V considering the effect of the programming. (Top) the trajectories of 1,000 electrons, and (bottom) the potential distribution calculated from the device simulator *HyENEXSS*. Arrows indicate the gradient directions of the potential energy.

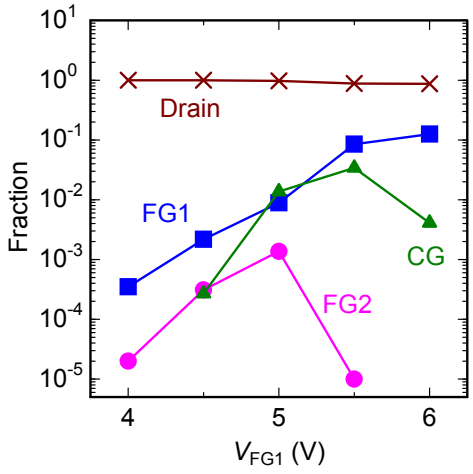

Figure 8. Relative percentages of the terminals where the injected electrons were finally absorbed. For each bias condition, 10^5 trials were carried out. Depending on V_{FG1}, the injected electrons can reach the adjacent floating gate (FG2) across the SiO_2 region.

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