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Modeling of Enhanced 1/*f* Noise in TFT with Trap Charges

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Abstract—**We have investigates influence of existing trap states of TFT on device characteristics with use of the compact model HiSIM-TFT. Special focus is given on the 1/*f* noise characteristics, where it is found the V_{gs} dependence of the 1/*f* noise characteristics is very sensitive to the trap density distributions. We have successfully extracted high density of the shallow trap states with the measured 1/*f* noise characteristics.**

Keywords-component; TFT; compact model; trap density; 1/f noise characteristics; I-V characteristics

I. INTRODUCTION (HEADING 1)

It has been demonstrated that the recrystalization of the ploy silicon results in high TFT performance valid even for RF applications [1]. This enables integration of complete circuits on a single display. This expands capability of the integrated displays for advanced applications. However, it is known that remained trapped states at grain boundaries of the poly silicon cannot be removed completely and influence on device performances. Here our purpose is to model the influence of the inevitable remained trap states on the device performances. For this purpose we have measured the 1/*f* noise characteristics, which are sensitive to the interface condition of MOSFET [2]. The different measured characteristics of the 1/*f* noise of TFTs in comparison to bulk MOSFETs without the trap sites are investigated with the compact model HiSIM-TFT, considering the trap density within the Poisson equation explicitly [3]. It is shown that the influence of the trap existence on the 1/*f* noise is much more enhanced than that on the I_{ds}-V_{gs} characteristics usually investigated. It is demonstrated that the 1/*f* noise characteristics of TFTs can be well reproduced by adjusting the trap-density distribution within the bandgap.

II. COMPACT MODEL HISIM-TFT WITH TRAP DENSITY

We have developed the TFT model HiSIM-TFT based on the surface-potential description [3]. The trap density is incorporated into the Poisson equation, which is solved iteratively

$$\frac{d^2\phi}{dx^2} = -\frac{q}{\varepsilon}\left(p - n + N_D^+ - N_A^- + N_{TA}^- - N_{TD}^+\right) \qquad (1)$$

where the trap densities (N_{TA}^- and N_{TD}^+) are modeled with a simple distribution function which decreases linearly in the bandgap as depicted in Fig. 1

$$g_A(E) = g_C exp\left(\frac{E_{fn} - E_C}{E_S}\right) \qquad (2)$$

$$g_D(E) = g_C exp\left(\frac{E_C - E_{fp}}{E_S}\right) \qquad (3)$$

where E_{fn} and E_{fp} are the quasi-Fermi energy for electrons and holes, respectively. E_C and E_V are the energy of the bottom of the conduction band and that of the top of the valence band, respectively. E_S and gc are the inverse slope of the trap states and the trap states density at E_C and E_V, respectively. By integrating the product of the Fermi-Dirac distribution function and each of (2) and (3) across the band gap, equations to describe the density of ionized acceptor-type traps and donor -type traps are obtained as [4]

$$N_{TA}^- = N_{tK} \cdot \exp\left(-\frac{E_{Fn} - E_C}{E_S}\right) \qquad (4)$$

$$N_{TD}^+ = N_{tK} \cdot \exp\left(-\frac{E_{Fp} - E_V}{E_S}\right) \qquad (5)$$

$$N_{tK} = gc \cdot E_S \cdot \frac{\frac{k \cdot T}{q \cdot E_S}}{\sin\left(\frac{k \cdot T}{q \cdot E_S}\right)} \qquad (6)$$

where T and k are the lattice temperature in kelvin and the Boltzmann constant, respectively. For compact modeling, the relation is rewritten with the quasi-Fermi potential, which is considered to be a function of electrostatic potential [5].

The potential distribution along the depth direction is obtained by solving the Poisson equation at the source side and the drain side of the channel under the quasi-gradual-channel approximation. By integrating depletion charges and trap charges in the poly-Si layer from the surface to the bottom of

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the backside, the relation between the surface potential and the backside potential are derived as

$$\Phi_b = \Phi_S - \frac{q}{2\varepsilon_{Si}} t_{Si}^2 \left\{ N_A + \left(\frac{n_i}{N_A} \right)^2 + N_{TA}^- - N_{TD}^+ \right\} \qquad (7)$$

where n_i is the intrinsic carrier density, ϕ_S is the surface potential, and t_{Si} is the silicon-layer thickness. Once the potential values are known at the source side and the drain side, all device characteristics (currents, charges, capacitances) are calculated as a function of these potential values [6].

Influence of these trapped charges on device characteristics is well confirmed by the increased subthreshold swing as well as the reduction of the current under the strong inversion condition. Calculated I_{ds}-V_{gs} characteristics are shown in Fig. 2 for three different trap distributions (see Fig. 1) together with without the trap.

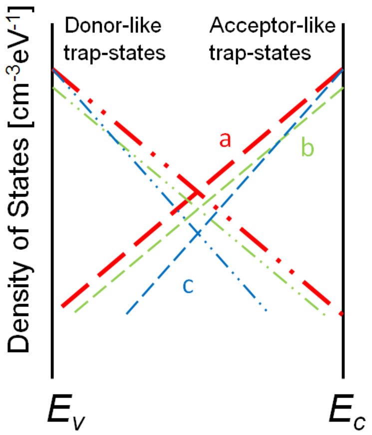

Fig.1. Two different trap types (the donor-like and the aacceptor-like) with three different density-state distributions ((a, b, c) within the bandgap approximated by a linear function.

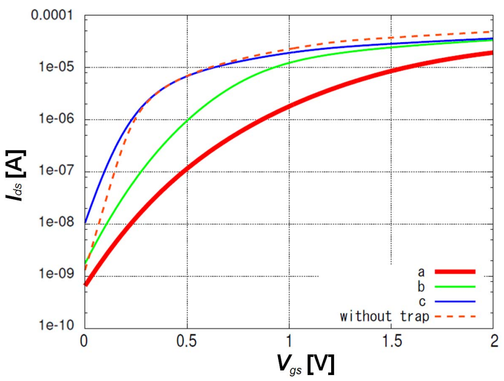

Fig.2. Calculated I_{ds}-V_{gs} characteristics with three trap densities depicted in Fig. 1. The dashed line shows the result without traps.

II. 1/*F* NOISE ANALYSIS

Measured 1/*f* noise normalized by the drain current I_{ds} and the device size are shown as a function of V_{gs} in Fig. 3 together with the I_{ds}-V_{gs} characteristics. It is recognized that the high trap density induces the strong degradation of the measured I_{ds}-V_{gs} characteristics and the increase of the 1/*f* noise at the same time as shown by thick solid lines.

Fig. 4 compares measured normalized 1/*f* noise intensity of a TFT to a bulk MOSFET as a function of V_{gs}.- V_{th}, where V_{gs} is the threshold voltage. The normalized noise intensity represents approximately the strength of the trap density [7]. Not only increase of the noise intensity but also accompanied reduction of the V_{gs} dependence is observed, namely the 1/*f* noise does not reduce with increased V_{gs} as expected from the silicon MOSFET.

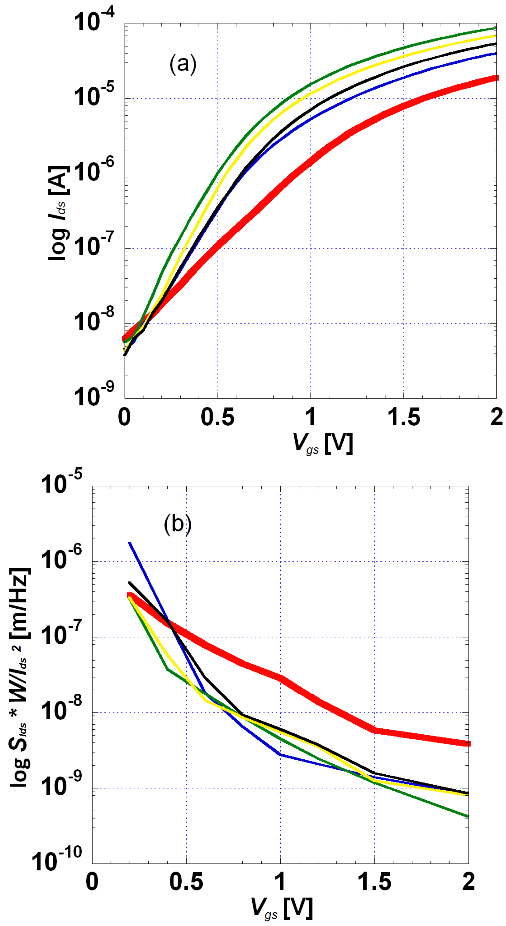

Fig. 3. Measured (a) I_{ds}-V_{gs} and (b) normalized 1/*f* noise characteristics as a function of V_{gs} for five different TFTs of the same size on a wafer.

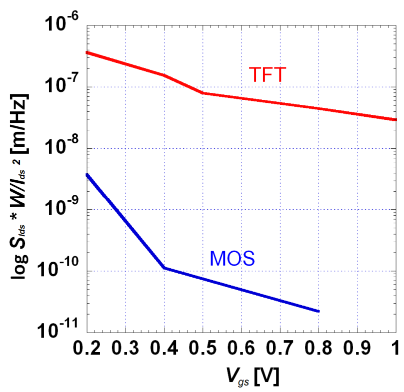

Fig.4. Measured normalized 1/*f* noise intensity as a function of V_{gs}-V_{th} for a TFT and a bulk MOSFET, where V_{th} is the threshold voltage.

Modeling of the $1/f$ noise is done by considering the carrier distribution along the channel [5]. The final equation is written as a function the drain current I_{ds}

$$S_{Ids}(f)=\frac{1}{(L-\Delta L)}\frac{I_{ds}^2}{W}\frac{N_t(E_f)}{qf}kT \left\{\frac{1}{(N_s+N^*)(N_l+N^*)}+\frac{2\alpha\mu}{N_l-N_s}\log\left(\frac{N_l+N^*}{N_s+N^*}\right)+(\alpha v)^2\right\} \quad (8)$$

where N_s, N_l, and N^* are the carrier concentration at the source side, at the drain side, and the averaged value, respectively. The trap density $N_t(E_t)$ is not necessarily equal to N_{TA}- N^+_{TD} appears in Eq. (1). Other parameters have the same meanings as used in literature [5].

With the simplified linearly decreasing function for the trap-state density depicted in Fig. 1, HiSIM-TFT reproduces measured I_{ds}-V_{gs} characteristics as shown in Fig. 5 for the case shown by the thick line in Fig. 3a. Results for two different V_{gs} values are depicted as examples. Fig. 6 compares calculated $1/f$ noise characteristics with the same trap density used for the I_{ds}-V_{gs} calculation to measurements shown by the thick line in Fig. 3b. Obvious discrepancy is detected for large V_{gs} values as shown by an arrow. For comparison the calculated result without the trap density is depicted together. The discrepancy cannot be removed by adjusting the trap density by changing g_c and E_s in Eqs. (2) and (3).

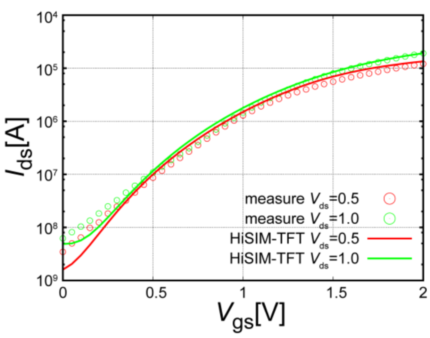

Fig.5. Comparison of calculated I_{ds}-V_{gs} characteristics with HiSIM-TFT (lines) to those of measurements (symbols).

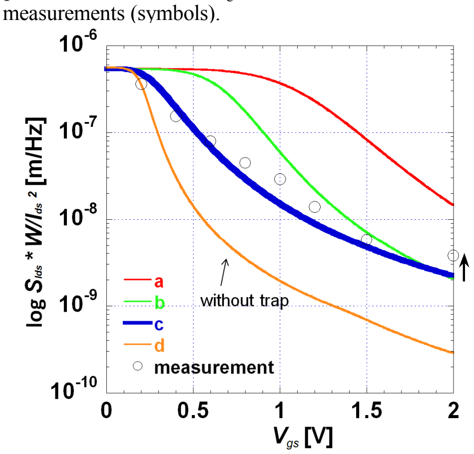

Fig.6. Calculated normalized $1/f$ noise intensities as a function of V_{gs}. The thick solid line shows the calculated result with trap density extracted from the measured I_{ds}-V_{gs} results. Circles are measured data.

Fig. 7a shows the correlation between the density of states for the acceptor-like trap states and the band structure. For small V_{gs} values, the Fermi level, where the most occupation of trapping occurs, lies nearly in the middle of the bandgap. Therefore the deep trap states are mostly responsible for the device characteristics. For large V_{gs} values, on the contrary, the Fermi level approaches to the conduction-band edge, resulting in increased occupations of the shallow trap states as can be seen in Fig. 7b.

Fig. 8 shows additional shallow trap states considered, where the deep trap states are kept the same. Three different trap-state distributions are studied. Calculated trap densities for the corresponding trap distributions are shown in Fig. 9 as a function of V_{gs}. Calculated I_{ds}-V_{gs} characteristics with the new trap density including the additional shallow trap states are depicted in Fig. 10. Influence of the shallow trap states is not so drastic for the current. Calculated $1/f$ noise characteristics are compared with measurements in Fig. 11. It is seen that the shallow trap states are much more sensitive to the noise characteristics of large V_{gs}. It can be concluded that the measured noise characteristics of TFT can be well reproduced by adjusting the additional high shallow trap tail densities. Thus more detailed investigation of the trap states is possible with the noise characteristics.

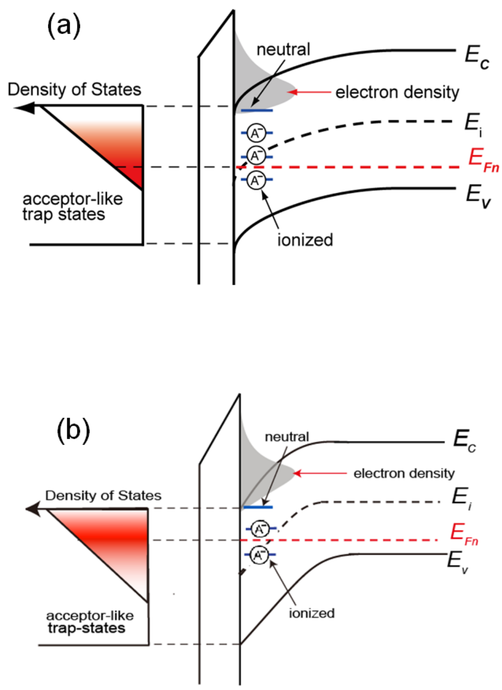

Fig.7. Linearly distributed density of acceptor-like trap states within the bandgap and the Fermi level depicted (a) for relatively small V_{gs} and (b) for relatively large V_{gs}. For relatively small Vgs the Fermi level lies nearly in the middle of the bandgap. The large V_{gs} causes strong band bending, resulting in the Fermi-level movement to the conduction-band edge. This results in the increase of the shallow trap occupation.

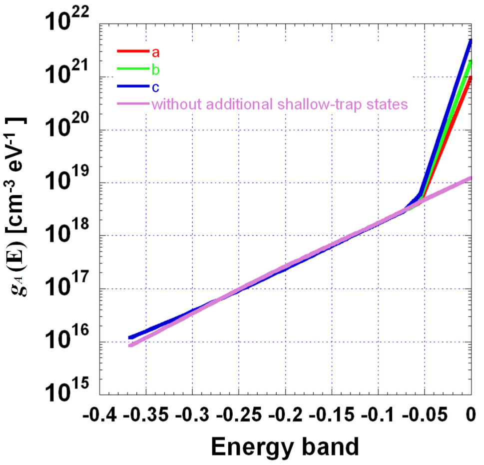

Fig.8. Additional shallow trap states considered. A linear function with different densities is studied. The thick solid line is the function for the deep trap states and the additional shallow states are shown by dashed lines.

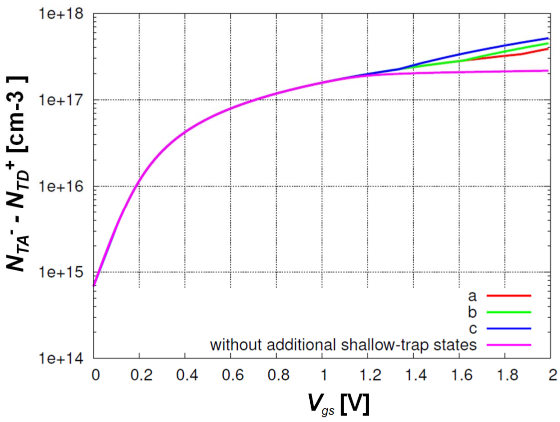

Fig. 9. Trap densities calculated as a function of V_{gs} for different density –of – states shown in Fig. 8.

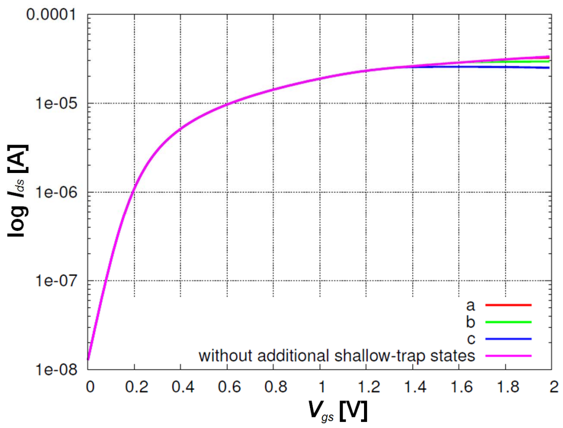

Fig. 10. Calculated I_{ds}-V_{gs} characteristics as a function of V_{gs} with the trap densities shown in Fig. 9. Influence of the different trap densities is not obvious.

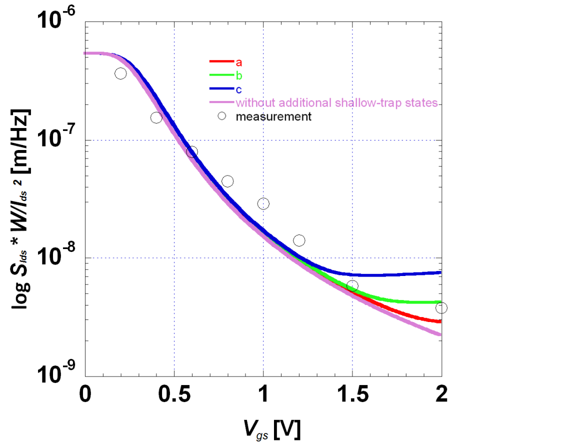

Fig. 11. Calculated normalized $1/f$ noise characteristics as a function of V_{gs} for different trap densities shown in Fig. 9. Symbols are measurements.

III. CONCLUSION

We have studied the $1/f$ noise characteristics of TFTs experimentally and theoretically. By considering the trap density in the Poisson equation, both measured I_{ds}-V_{gs} characteristics and $1/f$ noise characteristics can be well reproduced. To reproduce the measured $1/f$ noise characteristics under large V_{gs} condition, the shallow trap states must be considered. For the I_{ds}-V_{gs} characteristics, the mobility plays an important role, which conceals the influence of the trap density. Thus it can be concluded that the noise investigation is a powerful method to extract the trap density of states of devices with high density of trap states.

ACKNOWLEDGMENT

Authors would like to express their thanks to ALTEDEC and Hachioji Agilent for supporting this investigation.

REFERENCES

[1] G. Kawachi, G.Kawachi, M. Mitani, T. Okada and S. Tsuboi, "High-Frequency Performance of Sub-Micrometer Channel-Length Si TFTs Fabricated on Large Grain Poly-Si Films," SID 2007 Tech. Dig., pp.276, 2007.

[2] S. Matsumoto, H. Ueno, S. Hosokawa, T. Kitamura, M. Miura-Mattausch, H. J. Mattausch, T. Ohguro, S. Kumaoshiro, T. Yamaguchi, K. Yamashita, and N. Nakayama, "1/f Noise Characteristics in 100nm-MOSFETs and Its Modeling for Circuit Simulation, " IEICE Trans. Electron., E88-C, pp. 247, 2005.

[3] S. Miyano, Y. Shimizu, T. Murakami, and M. Miura-Mattausch, Proc. SISPAD, pp.373, 2008.

[4] T. Leroux, "Static and Dynamic Analysis of Amorphous-Silicon Fieled-Effect Transistors," Solid-State Electron., 29, pp. 47, 1986.

[5] D. Sugiyama, Master thesis, Hiroshima University, 2011.

[6] M. Miura-Mattausch, N. Sadachika, D. Navarro, G. Suzuki, Y. Takeda, M. Miyake, T. Warabino, Y. Mizukane, R. Inagaki, T. Ezaki, H. J. Mattausch, T. Ohguro, T. Iizuka, M. Taguchi, S. Kumashiro, and S. Miyamoto, "HiSIM2: Adbvanced MOSFET Model Valid for RF Circuit Simulation, " IEEE Trans. TED, 53, pp. 1994, 2006.

[7] N. Higashiguchi, Master Thesis, Hiroshima University, 2010