Analysis of geometrical structure and transport property in InAs/Si heterojunction nanowire tunneling field effect transistors

Yasuaki Miyoshi, Matsuto Ogawa,
and Satofumi Souma
Department of Electrical and Electronic Engineering,
Kobe University
1-1 Rokkodai, Nada, Kobe, 657-8501, Japan
Email: 118t266t@stu.kobe-u.ac.jp

Hajime Nakamura
Tokyo Research Lab., IBM-Japan,
1623-14 Shimotsuruma, Yamato, Kanagawa 242-8502, Japan

***Abstract*—Band-to-band tunneling (BTBT) field-effect transistors (FETs) is one of the promisng strategies in reducing the leakage current and improving the subthreshold characteristics compared with the conventional metal-oxide-semiconductor field-effect transistors (MOSFETs). However, BTBT-FETs have an intrinsic drawback of small on-current. We explore numerically the possibility of using the InAs/Si heterojunction nanowire (NW) to resolve such intrinsic difficulty in BTBT-FETs, and found that the use of the InAs/Si heterojunction nanowire is advantageous in increasing the on-current compared with the Si homojunction nanowires.**

I. Introduction

The progress of LSI technology has been based on downsizing of MOSFETs. This is because the downsizing has been the most effective way to improve the LSI circuit performance. In the present postscaling technology, however, the downsizing is becoming not effective to improve the device performance because we need to suppress leakage current, minimize short channel effect, and maintain high drive current at the same time. To meet these requirements, therefore, entirely new types of device such as nanowire transistors and carbon-based transistors have also been explored.

Among these new type devices, band-to-band tunneling transistors (BTBT-FETs) are expected to help reducing the power consumption of integrated circuits taking the advantages of the low leakage current and the small subthreshold swing (SS) below 60 mV/decade at the room temperature [1]-[3]. The reason of such property is that the magnitude of the current is mainly determined by the tunneling between the conduction and the valence bands through the barrier at the heterojunction. However, such tunneling conduction mechanism itself is a cause of small on-current. With such motivation we explore the possibility of using the InAs/Si heterojunction nanowire (NW) to resolve such intrinsic difficulty in BTBT-FETs.

II. Simulation Method and Device Model

The device structure under investigation is schematically shown in Fig. 1, where the p-Si/i-Si/n-InAs heterojunction nanowire with the circular cross section is surrounded by the SiO_2 gate oxide with the thickness 1.0 nm and the dielectric constant 4.2. A part of the gate oxide surrounding the central i-Si channel region is in turn surrounded by the metallic gate electrode as shown in Fig. 1. The length of the i-Si channel region is assumed to be 15 nm throughout this paper (the gate length is assumed to be equal to the channel length). The diameter of the NW will be given later.

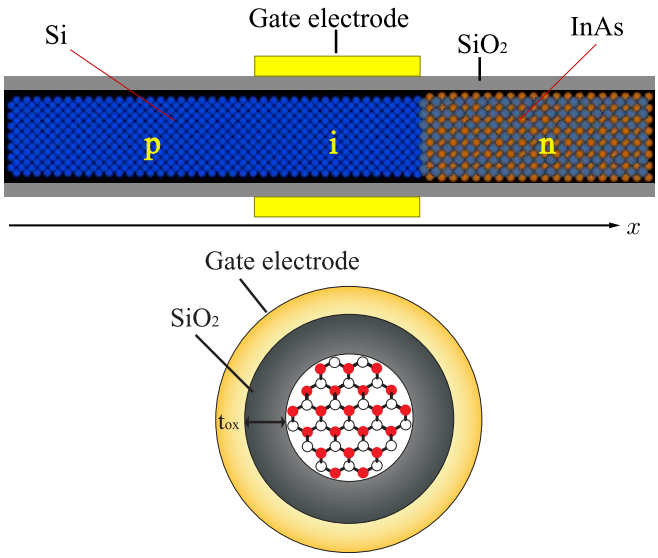


Fig. 1. Schematic illustrations of the InAs/Si heterojunction nanowire TFET structure considered in this study, where Si nanowire is used in p- and i-type regions while InAs nanowire is used in n-type region. The channel orientation is ⟨110⟩.

We note that the the source and the drain electrodes are assumed to be p-type and n-type, respectively, which make it possible to realize the tunneling conduction from the valence band in the source to the conduction band in the drain through the channel region. We also assume that the lattice matching between Si and InAs nanowire. In order to take into account the strain which arises from the different lattice constant of Si

978-1-61284-418-3/11/$26.00 © 2011 IEEE

and InAs, we use the valence force field method along with the Keating potential [4], [5], where the strain energy in the ith atom is given by

$$V(i) = \sum_j \frac{3\alpha_{ij}}{8d_{ij}^2}\left(|\boldsymbol{r}_{ij}|^2 - d_{ij}^2\right)^2 + \sum_{j,k>j} \frac{3\beta_{ijk}}{4d_{ij}d_{ik}}\left(\boldsymbol{r}_{ij}\cdot\boldsymbol{r}_{ik} - \frac{1}{3}d_{ij}d_{ik}\right)^2. \quad (1)$$

Here α_{ij} and β_{ijk} are the proportionality constants determined by the crystal elasticity, and are actually responsible for the changes of the bond length and the bond angle, respectively. In Eq. (1), $\boldsymbol{r}_{ij} = \boldsymbol{r}_i - \boldsymbol{r}_j$ with $\boldsymbol{r}_j$ being the position of the ith atom, and d_{ij} the equilibrium bond length between the ith and the jth atoms. Since the lattice constant of InAs is 10% larger than that of Si, the positions of atoms close to the Si/InAs hetero interface are expected to deviate from their original positions to minimize the total strain energy, making the structural relaxation calculation essentially important for the more rigorous analysis of transport property.

Once the relaxed structure is obtained, the calculation of the band-to-band tunneling current is carried out by using the three-dimensional non-equilibrium Green's function (NEGF) formalism [6] based on the sp^3s^* tight-binding (TB) method, which can properly take into account the quantum mechanical effect in the device within the atomistic resolution. In the NEGF formalism the device structure is described using the retarded Green's function obtained from the following equation for each electron energy E,

$$G(E) = [EI - H - U - \Sigma_{\rm L}(E) - \Sigma_{\rm R}(E)]^{-1}, \quad (2)$$

where H is the device Hamiltonian, and $\Sigma_{\rm L,R}(E)$ are appropriate boundary self-energies which replace the effect of the source and drain electrodes. In Eq. (2) U is the additional potential energy due to the gate voltage, and is assumed to be zero in the source region and $-qV_{\rm D}$ in the drain region. In the central channel region the value of U is assumed to be homogeneous and is determined by solving the Poisson's equation self-consistently with the charge density in the channel region assuming the infinitely long NW. The band-to-band tunneling current is calculated by

$$I = \frac{2q}{h}\int dE T(E)(f(E-\mu_{\rm S}) - f(E-\mu_{\rm D})), \quad (3)$$

where q (>0) is the elementally charge, $f(E-\mu)$ is the Fermi-Dirac distribution function, $\mu_{\rm S} = E_{\rm F}$ and $\mu_{\rm D} = \mu_{\rm S} - qV_{\rm D}$ are the Fermi energies in the source and the drain electrode, with $V_{\rm D}$ being the source-drain voltage. We assume the room temperature T =300 K throughout this paper. In Eq. (3), $T(E)$ is the transmission coefficient expressed in term of the Green's function as

$$T(E) = {\rm Tr}[\Gamma_{\rm R}(E)G(E)\Gamma_{\rm L}(E)G^\dagger(E)], \quad (4)$$

where $\Gamma_{\rm L,R}(E)$ are broadening functions represented by the self energies as

$$\Gamma_{\rm L,R}(E) = i\left([\Sigma_{\rm L,R}(E)] - [\Sigma_{\rm L,R}(E)]^\dagger\right). \quad (5)$$

III. Results and Discussions

A. Band structures

Figure 2 shows the band structures of ⟨110⟩ axis-oriented intrinsic Si and InAs NWs calculated using the sp^3s^* tight-binding model [7], [8]. The diameters of the Si NW and InAs NW assumed in our calculations are estimated as 1.55 nm and 1.72 nm, respectively. Our calculations show that the Si NW has the indirect transition bandgap with the bandgap energy $E_{\rm g}$=1.29 eV, while the InAs NW exhibits the direct transition bandgap with $E_{\rm g}$=1.29 eV. In order to simulate the p-type doping in the Si NW source electrode and the n-type doping in the InAs NW drain electrode effectively, we simply shift their intrinsic band structures in Fig. 2 by 0.7 eV (upward shifting) for Si NW and by -0.75 (downward shifting) for InAs NW, while the equilibrium Fermi energy is kept at $E_{\rm F} = 0$.

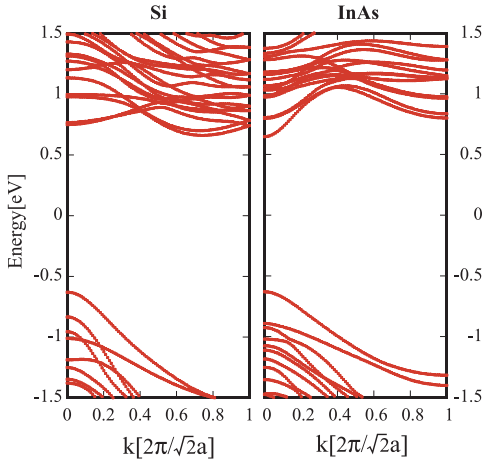


Fig. 2. Band structures of the ⟨110⟩ oriented Si NW (left side) and InAs NW (right side), where a = 5.4309 and 6.058 Å are the lattice constants of bulk Si and InAs, respectively.

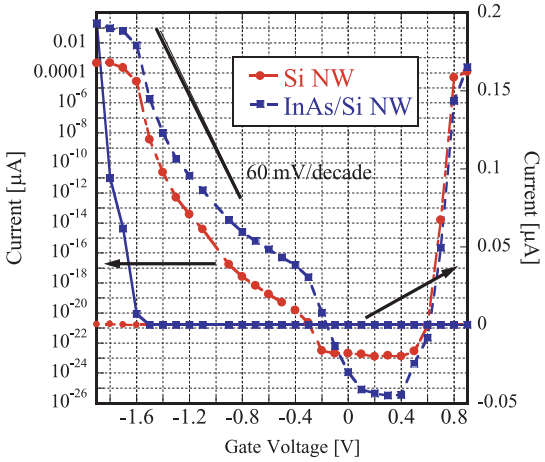
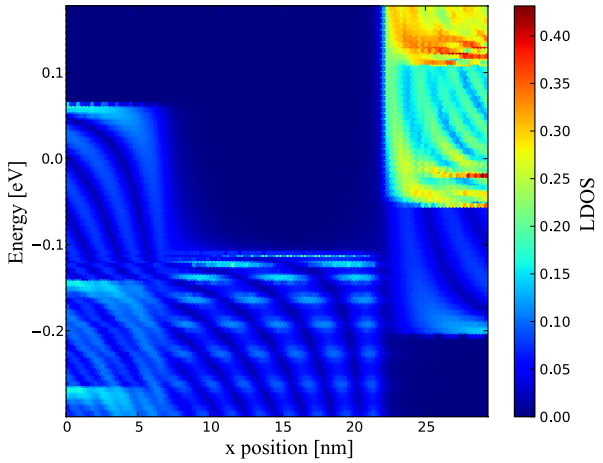
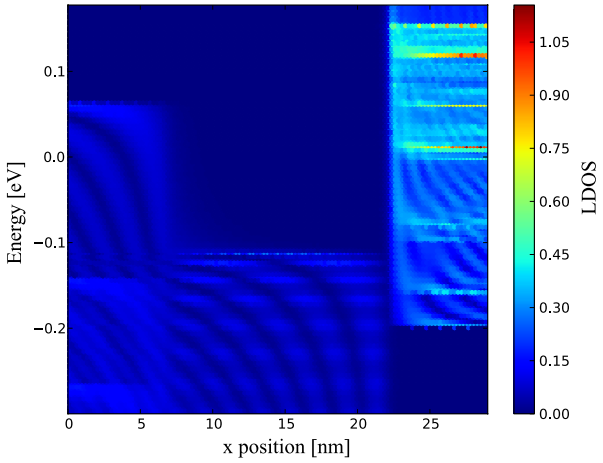


Fig. 3. $I_{\rm D}$-$V_{\rm G}$ curves of Si/InAs NW TFET and Si NW TFET are plotted for a given source-drain voltage $V_{\rm D}$ = 0.1 V. The room temperature 300 K is assumed.



(a) InAs/Si heterojunction NW



(b) Si NW

Fig. 4. Local density of states in (a) Si/InAs NW model and (b) Si NW model for $V_{\rm D} = 0.1$ V and $V_{\rm G} = -1.9$ V. Here three clearly distinguishable regions correspond to the p-Si source (left), i-Si channel where the gate voltage has been applied (center), and the n-InAs (a) or n-Si (b) drain (right).

B. $I_{\rm D}$-$V_{\rm G}$ characteristics

Having understood the band structures in Si and InAs NWs, we now show the calculated current in our p-Si/i-Si/n-InAs heterojunction NW BTBT-FET. For comparison we also analize the current through p-Si/i-Si/n-Si homojunction NW BTBT-FET in the same condition. (These two devices are hereafter referred to as Si/InAs NW model and Si NW model, respectively.) Such comparison makes it possible to understand the essential difference between the band-to-band tunneling at the Si/Si homo interface and that at the Si/InAs hetero interface as we will explain later. Figure 3 shows the $I_{\rm D}$-$V_{\rm G}$ curves for Si/InAs NW model and for Si NW model. When the positive gate voltage is applied ($V_{\rm G} > 0$), the bandstructure in the channel region is shifted lower in energy, and then the n-channel opens in the central i-Si region if $V_G > V_{\rm th}^{(\rm n)} \simeq 0.8$ V. In such situation the tunneling probability from the source valence band to the channel conduction band mainly limits

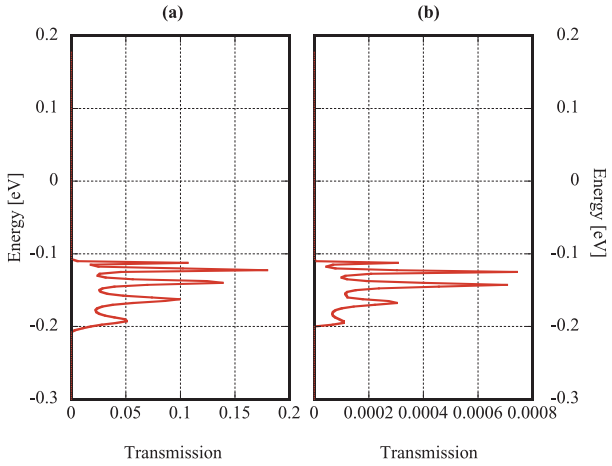


Fig. 5. Transmission probabilities in (a) Si/InAs NW model and (b) Si NW model for $V_{\rm D} = 0.1$ V and $V_{\rm G} = -1.9$ V are plotted as a function of electron energy.

the current both for Si NW and InAs/Si NW models. In other words, the band-to-band tunneling process takes place at the p-Si/i-Si interface in both two models, leading to the same characteristics of the current for two models in $V_{\rm G} > 0$ as seen in Fig. 3. When the negative gate voltage is applied ($V_{\rm G} < 0$), on the other hand, the band structure in the i-Si channel region is shifted upper in energy, and then the p-channel opens in the central i-Si region if $V_G < V_{\rm th}^{(\rm p)} \simeq -1.6$ V, where the current is mainly governed by the tunneling probability from the channel valence band to the drain conduction band. In contrast to $V_{\rm G} > 0$ regime, such tunneling process takes place at different typs of interface in two models, that is, Si/Si homo interface in the Si NW model and Si/InAs hetero interface in the InAs/Si NW model. Evidently, when the gate voltage $V_{\rm G} = -1.9$ V, the on-current is 0.19 μA in InAs/Si NW model while it is 0.44 nA in Si NW model. From these observations we notice that the Si/InAs interface gives higher on-current compared with the Si/Si interface. Moreover, the subthreshold swing in the p-channel operation regime ($V_{\rm G} < 0$) is estimated as 28 mV/decade for InAs/Si NW model and 26 mV/decade for Si NW model, both of which are better characteristics compared with the conventional MOSFETs with the typical subthreshold swing being 60 meV/decade. Therefore, it is found that the use of the InAs/Si heterojunction nanowire is advantageous in increasing the on-current compared with the Si homojunction nanowires keeping the lower subthreshold swing.

C. Local density of states and transmission probability

In order to understand the switching behaviors discussed above more deeply, we now analyze the local density of states (LDOS) and transmission probability. Here the LDOS is calculated as $\rho(\boldsymbol{r}, E) = -\mathrm{Im}\,\langle \boldsymbol{r}|\, G(E)\, |\boldsymbol{r}\rangle\, /\pi$ in terms of the Green's function given in Eq. (2). Figures 4 (a) and (b) show the spatial distributions of the LDOS in InAs/Si NW and the Si NW models, respectively, which are estimated for

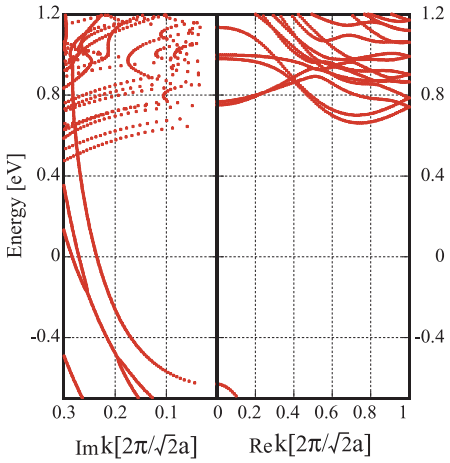


Fig. 6. Complex band structures of Si NW.

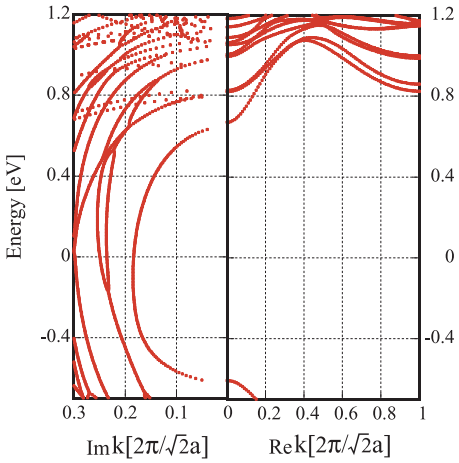


Fig. 7. Complex band structures of InAs NW.

the gate voltage $V_G = -1.9$ V. The brighter region in the figure represents higher DOS. As seen in these figures, two models do not show significant difference of the LDOS in the source and the channel regions even though the source material is different in two models. However, the LDOS near the bottom of conduction band in the source region is clearly different, which can be cast into the different behaviors of the conduction band structure in Si NW and InAs NW shown in Fig. 2, resulting in the different characteristics of Si/InAs NW and Si NW models. Figure 5 shows (a) the transmission probability from the p-Si souce electrode to the n-InAs drain electrode for InAs/Si NW model and (b) that from the p-Si source electrode to n-Si drain electrode for Si NW model, estimated for $V_D = 0.1$ V and $V_G = -1.9$ V. As seen in these figures, the tunneling transmission probability from the Si NW valence band to the InAs NW conduction band is about a handred times larger than that form the Si NW valence band to the Si NW conduction band. This explains the reason why Si/InAs NW model exhibits significantly larger on-current than Si NW model in $V_G < 0$ regime as shown in Fig. 3. Then it is meaningful to consider the physical mechanism behind such property. For such purpose now we plot the complex band structures of intrinsic Si NW and InAs NW in Figs. 6 and 7, respectively, where we have employed the calculation method described in Ref. [9] . Here the imaginary part of the complex wavenumber Im[k] in the bandgap region is interpreted as the magnitude of decay rate, so that the bigger value of Im[k] means the faster spatial decay of the wavefunction through the bandgap. By comparing Figs. 6 and 7, we observe that Im[k] in the bandgap region is much larger in Si NW than in InAs NW especially near the conduction band bottom, meaning that the wavefunction is more likely to decay in Si NW bandgap than in InAs NW bandgap. Since the band-to-band tunneling probability is mainly determined by the decay rate through the bandgap region responsible for respective materials, we can understand that the smaller decay rate of the InAs NW bandgap makes the barrier at the Si/InAs interface more penetrable than that at the Si/Si interface, leading to the higher tunneling on-current in Si/InAs NW model than Si NW model.

IV. Conclusion

We have analyzed the performance of the BTBT-FET comprised of InAs/Si heterojunction nanowires. By comparing with the performance of BTBT-FET comprised of Si homojunction nanowire, we found that the use of the InAs/Si heterojunction NW is advantageous in the negative gate voltage regime in increasing the on-current by hundred times compared with the Si homojunction nanowire, while keeping the lower subthreshold swing as low as 28 mV/decade.

References

[1] K. Lam, D. Seah, S. Chin, B. Kumar, S. Samudra, G. Y. Yeo, and G. Liang, "A Simulation Study of Graphene-Nanoribbon Tunneling FET With Heterojunction Channel," IEEE Electron Device Letters, **31**, 555 (2010).

[2] M. Luisier and G. Klimeck, "Atomistic Full-Band Design Study of InAs Band-to-Band Tunneling Field-Effect Transistors," IEEE Electron Device Letters, **30**, 602 (2009).

[3] S. Agarwal, G. Klimeck, and M. Luisier, "Leakage-Reduction Design Concepts for Low-Power Vertical Tunneling Field-Effect Transistors," IEEE Electron Device Letters, **31**, 621 (2010).

[4] P. N. Keating, "Effect of Invariance Requirements on the Elastic Strain Energy of Crystals with Application to the Diamond Structure," Phys. Rev **145**, 637 (1966).

[5] R. M. Martin, "Elastic Properties of ZnS Structure Semiconductors," Phys. Rev. B **1**, 4005 (1970).

[6] S. Datta, "Electronic Transport in Mesoscopic Systems," Cambridge University Press (1995).

[7] J. C. Slater and G. F. Koster, "Simplified LCAO Method for the Periodic Potential Problem," Phy. Rev. **94**, 1498 (1954).

[8] P. Vogl, H. P. Hjalmarson, and J. Dow, "A Semi-Empirical Tight-Binding Theory of the Electronic Structure of Semiconductors," J. Phys. Cem. Solids **44**, 365 (1983).

[9] T. Ando, "Quantum point contacts in magnetic fields," Phys. Rev. B **44**, 6207 (1985).