P17

Enhancement of the device characteristics for nanoscale charge trap flash memory devices utilizing a metal spacer layer

Hyun Woo Kim, Joo Hyung You, Dea Uk Lee, and Tae Whan Kim
Department of Electronics and Computer Engineering
Hanyang University
Seoul, 133-791, Korea
twk@hanyang.ac.kr

Keun Woo Lee
Research and Development Division
Hynix Semiconductor Inc.
Icheon-si, Kyungki-do, 467-701, Korea

Abstract—**Nanoscale charge trap flash (CTF) memory devices with a metal spacer layer were designed to decrease the interference effect and to increase the fringing field effect and the coupling ratio. The optimum metal spacer depth of the memory devices was determined to enhance the device performance of the memory devices. The drain current and the threshold voltage shifts of the CTF memory devices were increased due to an increase in the fringing field and the coupling ratio resulting from the existence of the optimized metal spacer. The interference effect between neighboring cells was decreased due to the shielding of the electric field resulting from the existence of the metal spacer layer.**

Keywords-charge trap flash memory; interference effect; fringing field; coupling ratio

I. INTRODUCTION

Low-cost and high-density nonvolatile memory (NVM) devices have been currently receiving considerable attention for potential applications in portable devices [1-4]. Among the NVM devices, the charge trap flash (CTF) memory devices have been particularly interesting because of potential applications in mobile devices due to their excellent advantages of better scaling capability and smaller capacitive coupling interference between the adjacent cells in comparison with traditional floating gate flash memory devices [5]. However, the scaled down CTF memory devices still have inherent problems of the coupling interference between the adjacent cells in a bit-line direction [6-10]. The metal spacer layer existing in both sides of each memory cell closes to the Si substrate, resulting in an increase of the interference effect and fringing field on the channel area. However, a high electric field in an oxide layer between the metal spacer layer and the Si substrate is generated due to the small distance between the lower edge of the metal spacer and the Si substrate, resulting in a high gate leakage current [11]. Even though some works concerning the coupling interference phenomenon in the CTF memory devices have been conducted [10], systematic studies on the decrease in the coupling interference of the CTF memory devices utilizing a metal spacer with an optimum depth are very important for enhancing their device performance and density.

This paper reports data for the device characteristics of the decrease of the interference effect between neighbor cells and to increase the fringing field on the channel surface between cells and the coupling ratio of the control gate for the CTF memory devices fabricated utilizing a metal spacer. The optimum size of the metal spacer layer for the CTF memory devices was determined by using a technology computer-aided design (TCAD) simulation tool taking into account the gate leakage current, the interference effects, and the fringing field effects.

II. FABRICATION PROCESS

Nanoscale metal-oxide-nitride-oxide-semiconductor, denoted by CTF memory devices, memory devices with a metal spacer layer are designed by using the conventional device process technology. The cleaned Si wafer is used as a substrate, as shown in Fig. 1(a). After the deposition of the tunnel oxide and the nitride layers, the nitride layer is etched, as shown in Fig. 1(b). After the deposition of the blocking oxide layer shown in Fig. 1(c), the blocking oxide layer is etched, as shown in Fig. 1(d). After the metal electrode is deposited, the source/drain is doped, as shown in Fig. 1(e). Finally, the gates and the source/drain contacts are patterned, as shown in Fig. 1(f). The thicknesses of the oxide-nitride-oxide layers formed on the substrate are 4/5/6 nm. The doping concentrations of the source region, the drain region, and the substrate are 3×10^{18}, 3×10^{18}, and 1×10^{17} cm^{-3}, respectively. Fig. 1(f) shows the fabricated memory devices with a 30-nm channel length and a 14-nm length between neighboring cells. The metal spacer layer is formed to surround the nitride trap layer in the proposed CTF memory devices. The distance between the lower edge of the metal spacer and the Si substrate is defined as the metal spacer depth, as indicated in Fig. 1(f). The thickness of the blocking oxide and the oxide layers between the metal spacer and the nitride trap layers is 6 nm. The left and right cells in memory devices for conventional

978-1-61284-418-3/11/$26.00 © 2011 IEEE

memory devices and proposed memory devices are defined as cell 1 and cell 2, respectively.

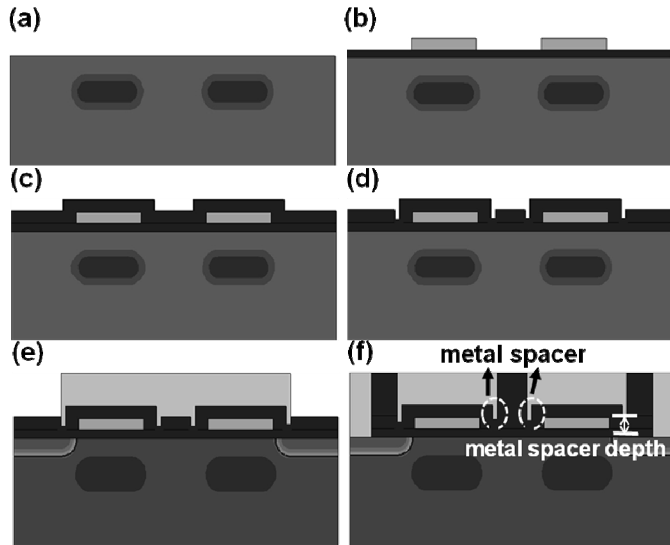

Figure 1. Fabrication method of the proposed CTF memory devices.

III. Results and Discussion

A. The optimization of the metal spacer layer depth

Fig. 2(a) shows the gate leakage current as a function of the gate stress time for the proposed CTF memory devices with a different metal spacer layer depth and the conventional memory devices at a programming voltage of 16 V. The gate leakage current of the conventional device have the lowest value among the memory devices. The gate leakage current decreases with increasing metal spacer depth from 2 to 6 nm. The electric field across the tunnel oxide layer decreases with increasing the distance between the lower edge of the metal spacer and the Si substrate, resulting in a decrease in the gate leakage current. Fig. 2(b) shows the magnitude of the electric field along the cell to cell direction at a ground voltage of the Vg1 and the 5 V pass voltage of Vg2. Fig. 2(c) shows the magnitude of the electric field along the channel surface direction at the 5 V pass voltages of Vg1 and Vg2. The electric field of the region between the nitride and the right metal spacer layer of the cell 1 along the cell to cell direction for the device with a metal spacer depth of 6 nm is decreased in comparison with that of the conventional device, as shown in Fig. 2(b). The electric field of the devices with metal spacer depths of 2 and 4 nm disappears in the region between the nitride and the right metal spacer layers of the cell 1, indicative of the perfect shielding effect. The fringing field of the channel region increases with decreasing metal spacer depth, as shown in Fig. 2(c). Because the distance between the metal spacer and the channel region decreases with decreasing metal spacer depth, a larger fringing field is generated in a channel region, resulting in an increase in the drain current [12]. When the metal spacer depth increases above 4 nm, while the gate leakage current characteristics of the devices with a metal spacer were improved, their interference and fringing field characteristics were deteriorated. Therefore, the optimum metal spacer depth of the devices is 4 nm.

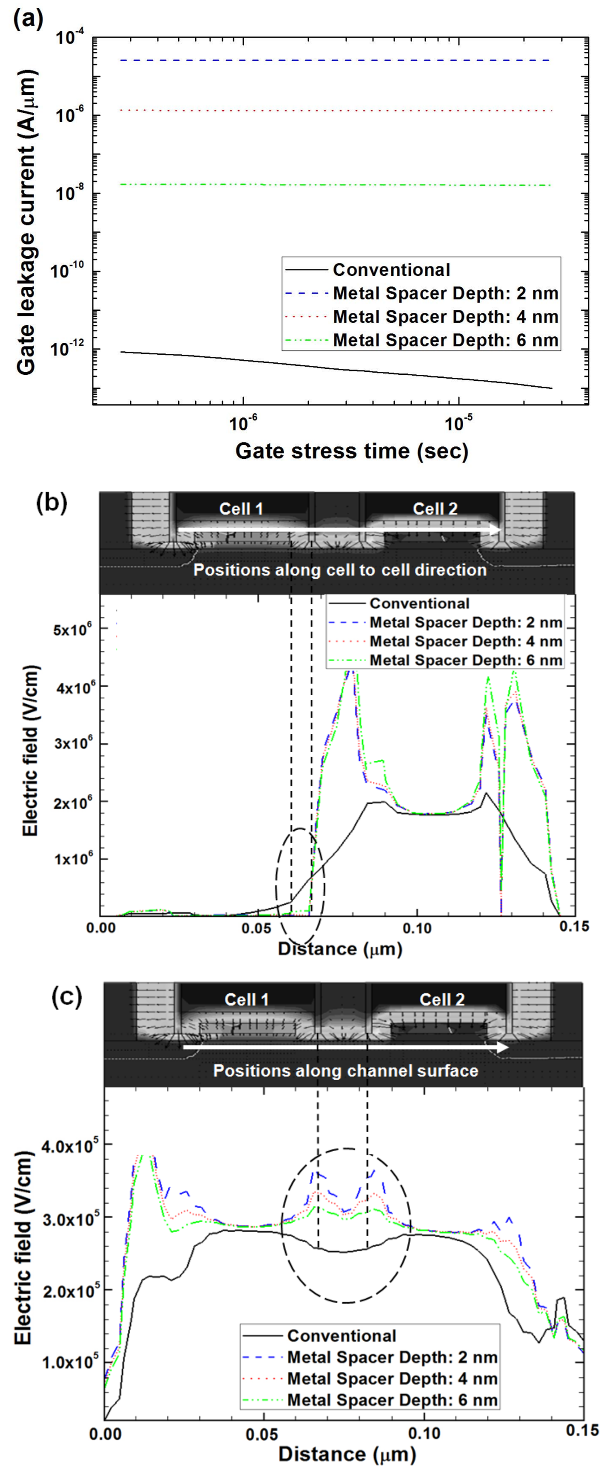

Figure 2. The optimization of the metal spacer layer depth; (a) gate leakage current as a function of the gate stress time, (b) the magnitude of the electric field along the cell to cell direction at the ground voltage of Vg1 and the pass voltage of 5 V for Vg2, and (c) the magnitude of the electric field along the channel surface direction at the pass voltage of 5 V for Vg1 and Vg2. The solid line indicates the gate leakage current as a function of the gate stress time for the conventional device without a metal spacer layer, and the dashed line, the dotted line, and the dashed-dotted line represent the data for the devices with a metal spacer depth of 2, 4, or 6 nm, respectively.

B. Operation characteristics

Fig. 3 shows the current-voltage (I-V) characteristics for the (a) conventional and (b) proposed CTF memory devices with an optimized metal spacer depth of 4 nm before and after programming of the cell 1. After the programming operation at the same operation condition, the threshold voltage shift of the CTF memory devices with a metal spacer layer is larger than that of the conventional memory devices. The coupling ratio of the control gate for the proposed memory devices is increased due to the surrounding metal gates. The threshold voltage shifts of the conventional and proposed CTF memory devices are 4.5 and 6 V, respectively, as shown in Figs. 3(a) and 3(b). An increase in the threshold voltage shift for the proposed CTF memory devices provides potential applications in the multi-level cell operation. After the erasing operation, the threshold voltage shift of the cell for the proposed memory devices return to the initial state, as shown in Fig. 3(b). The voltages of the program and the erasing operations are 16 and -12.8 V, respectively. The programming and erasing times of the proposed memory devices are approximately 1×10^3 and 5×10^3 µs, respectively. The operation conditions of the proposed CTF memory devices used in this simulation are shown in Table I.

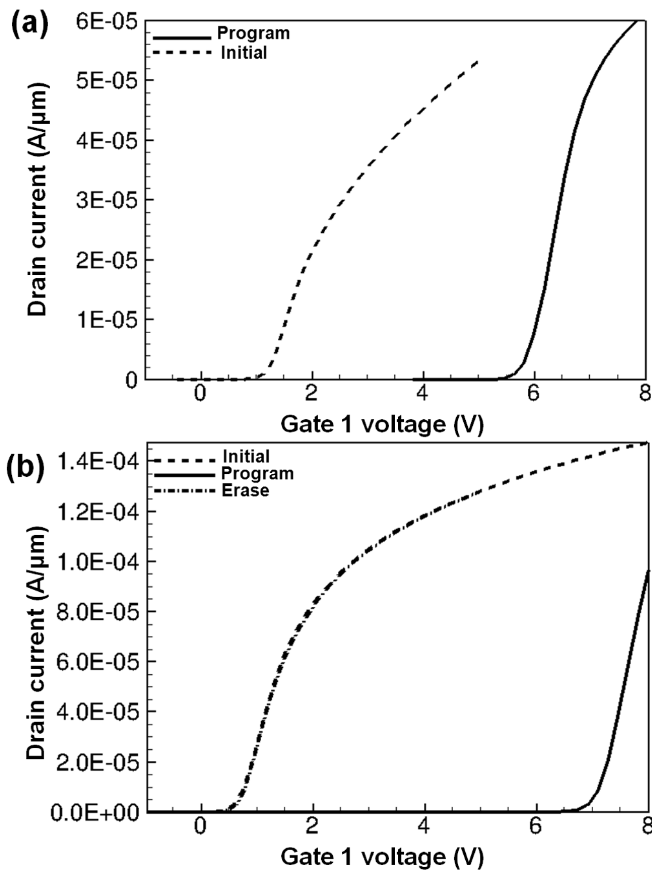

Figure 3. Current - voltage characteristics of the cell before and after program operations for the (a) conventional and (b) proposed CTF memory devices.

TABLE I. OPERATION CONDITIONS OF THE PROPOSED CTF MEMORY DEVICES.

		Program	Erase	Read
Gate(V)	Selected WL	16	-12.8	V_{read}
	Unselected WL	0	0	V_{pass}
Drain (V)		0	Floating	0.1
Source (V)		0	Floating	GND
Operation speed (µs)		10^3	5×10^3	
Operation mechanism		F-N tunneling	F-N tunneling	

Fig. 4 shows the I-V characteristics of the cell 1 for the (a) conventional and the (b) proposed CTF memory devices before and after programming of cell 2. Because the coupling interference between the cells is significantly decreased due to the existence of the metal spacer layer, the I-V characteristics of cell 1 before and after programming cell 2 for the proposed CTF memory devices are almost constant in comparison with those of the conventional devices, as shown in Figs. 4(a) and 4(b). Simultaneously, the drain current of the proposed device is larger than that of conventional devices due to an increase in the fringing field resulting from the existence of the metal spacer layer. Because the metal spacer layer of the device increases the coupling ratio and the fringing field and shields the electric field resulting from the generation of the coupling interference between the cells, the device performance for the CTF memory devices with a metal spacer layer is significantly improved. The magnitudes of the drain current and the threshold voltage shift affect the coupling interferences between the cells during the program operation.

IV. SUMMARY AND CONCLUSIONS

I-V characteristics of the proposed CTF memory devices showed that the interference effect of the devices was decreased due to the existence of the metal spacer layer and that their fringing field effect and coupling ratio were increased. The optimum metal spacer depth of the memory devices was 4 nm. The drain current and the threshold voltage shifts of the CTF memory devices utilizing an optimized metal spacer were increased due to the increase of the fringing field and the coupling ratio. The interference effect between neighboring cells was decreased due to the shielding of the electric field. These results indicate that CTF memory devices with an optimum metal spacer depth hold promise for potential applications in nanoscale nonvolatile memory devices.

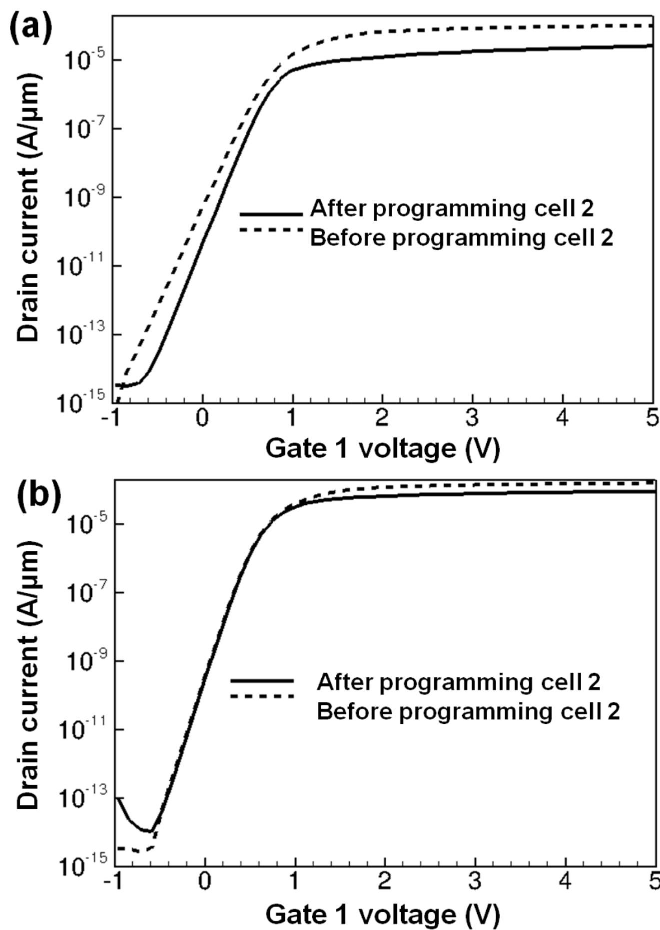

Figure 4. Current-voltage characteristics of the cell 1 for the (a) conventional and the (b) proposed CTF memory devices before and after programming of the cell 2.

ACKNOWLEDGMENT

This work was supported by the National Research Foundation of Korea (NRF) grant funded by the Korea government (MEST) (No. 2010-0018877), and this work was also supported in part by the Hynix semiconductor Inc.

REFERENCES

[1] K. T. Park, J. S. Sel, J. Choi, Y. Song, C. Kim, and K. Kim, "A novel NAND flash emory with asymmetric S/D structure using fringe-field-induced inversion layer," IEEE Trans. Electron Devices, vol. 55, pp. 404–410, January 2008.

[2] S. G. Jung and J. H. Lee, "Flash memory device with 'I' shape floating gate for sub-70 nm NAND flash memory," J. Appl. Phys, vol. 45, pp. 1200–1202, November 2006.

[3] C. Y. Ng, T. P. Chen, J. I. Wong, M. Yang, T. S. Khor, C. L. New, C. M. Li, A. D. Trigg, and S. Li, "Performance of silicon nanocrystal non-volatile memory devices under various programming mechanisms," J. Nanosci. Nanotechnol, vol. 7, pp. 329–334, December 2007.

[4] R. Bez, E. Camerlenghi, A. Modelli, and A. Visconti, "Introduction to flash memory," Proc. IEEE, vol. 91, pp. 489–502, April 2003.

[5] A. Otake, K. Yamaguchi, K. Kobayashi, and K. Shiraishi, "Theoretical studies on the charge trap mechanism of MONOS type meories – relationship between atomistic information and program/erase actions," Microelectronic Engineering, vol. 86, pp. 1849–1851, March 2009.

[6] J. D. Lee, S. H. Hur, and J. D. Choi, "Effects of floating-gate interference on NAND flash memory cell operation," IEEE Electron Device Letters, vol. 23, pp. 264–266, May 2002.

[7] T. Kitamura, M. Kawata, I. Honma, I. Yamamoto, S. Nishimoto, and K. I. Oyama, "A low voltage operating flash memory cell with high coupling ratio using horned floating gate with fine HSG," VLSI Symp. Tech. Dig., pp. 104–105, 1998.

[8] T. Cho, Y. Lee, E. Kim, J. Lee, S. Choi, S. Lee, D. Kim, W. Han, Y. Lim, J. Lee, J. Choi, and K. Suh, "A 3.3 V 1 Gb multi-level NAND flash memory with non-uniform threshold voltagedistribution," ISSCC Dig. Tech. Papers, pp. 28–29, February 2001.

[9] Y. W. Chang, G. W. Wu, P. C. Chen, C. H. Chen, I. C. Yang, C. Y. Chin, I. J. Huag, W. J. Tsai, T. C. Lu, W. P. Lu, K. C. Chen, and C. Y. Lu, "A new interference phenomenon in sub-60 nm nitride-based flash memory," IEEE Non-Volatile Semiconductor Memory Workshop, pp. 81–82, 2007.

[10] M. C. Park, K. S. Kim, J. H. Park, and J. H. Choi, "Direct field effect of neighboring cell transistor on cell-to-cell interference of NAND flash cell arrays," IEEE Electron Device Letters, vol. 30, pp. 174–177, February 2009.

[11] M. T. Quddus, T. A. DeMassa, and J. J. Sanchez, "Unified model for Q_{BD} prediction for thin gate oxide MOS devices with constant oltage and current stress," Microelectronic Engineering, vol. 51, pp. 357–372, 2000.

[12] M. Schlosser, K.K. Bhuwalka, M. Sauter, T. Zilbauer, T. Sulima, and I. Eisele, "Fringing-induced drain current improvement in the tunnel field-effect transistor with high-k gate dielectrics," IEEE Trans. Electron Devices, vol. 56, pp. 100–108, January 2009.