P16

Effect of the trap density and distribution of the silicon nitride layer on the retention characteristics of charge trap flash memory devices

Joo Hyung You, Hyun Woo Kim, Dong Hun Kim, and Tae Whan Kim
Department of Electronics and Computer Engineering
Hanyang University
Seoul, 133-791, Korea
twk@hanyang.ac.kr

Keun Woo Lee
Research and Development Division
Hynix Semiconductor Inc.
Icheon-si, Kyungki-do, 467-701, Korea

Abstract—**The trap distribution in the silicon-nitride layer, which was estimated by using experimental results, was used to clarify the retention characteristics of TaN-Al_2O_3-Si_3N_4-SiO_2-Si (TANOS) memory devices. The dependence of the trap density and distribution of the silicon nitride layer on the retention characteristics in TANOS memory devices was investigated by using the two-coupled rate equations together with the Shockley-Reed statistics. Simulation results showed that the retention characteristics in TANOS memory devices increased with increasing trap density near and above the Fermi-level in the silicon-nitride layer. The simulation results for the retention characteristics of TANOS memory devices were in reasonable agreement with the experimental results. These observations can help improve understanding of the retention mechanisms and the reliability problems in charge trap flash (CTF) memory devices.**

Keywords-TANOS flash memory; retention characteristics; trap distribution; silicon nitride

I. INTRODUCTION

High-density nonvolatile memory (NVM) devices have attracted much attention because of their promising applications in portable mobile devices utilizing flash memories for data storage [1-3]. Among the NVM devices, charge trap flash (CTF) memory devices using a localized-trapping layer and a high-k dielectric material have been particularly interesting due to their excellent advantages of lower program/erase operation voltage, simpler fabrication process, better scaling capability and smaller capacitive coupling between adjacent cells in comparison with traditional floating gate flash memory devices [4-6]. Flash memory devices utilizing a charge trap layer decrease the stress-induced leakage current and are used for three-dimensional structural flash memory devices [7, 8]. However, the data retention characteristics in the CTF memory devices at high temperatures have inherent problems due to the charge loss in the charge trap layer [9, 10]. The carrier transport mechanisms in a charge trap layer with many trap sites have been extensively investigated to address reliability issue and to increase the retention time in CTF memory devices [11-13]. Even though some theoretical works concerning the retention characteristics of CTF memory devices have been performed using a simple trap distribution model of the charge trap layer [12, 13], very few studies on the long retention mechanisms in CTF memory devices based on the intrinsic characteristics of the charge trap layer have been reported. Systematic studies on the dependence of the retention characteristics on the trap distribution of the charge trap layer in CTF memory devices are very important if the retention characteristics and the device reliabilities of CTF memory devices are to be improved [14, 15]. This paper reports data for the dependence of the retention characteristics on the trap distribution in the Si_3N_4 layer in TaN-Al_2O_3-Si_3N_4-SiO_2-Si (TANOS) CTF memory devices. For the simulation, the trap distribution inside the Si_3N_4 layer was modeled using a combination of an exponential distribution near the conduction band and two Gaussian distributions, one for shallow energy levels and the other for deep energy levels. The dependence of the retention characteristics on the trap distribution inside the Si_3N_4 layer was numerically calculated to investigate the material parameters needed to enhance the memory performance. The theoretical results for the retention characteristics in the TANOS structure were compared with the experimental results.

II. THEORETICAL CONSIDERATION

The structure of the memory device used in this simulation is TANOS. Electrons injected from the Si substrate are captured in the trap sites existing in the Si_3N_4 layer. The electrons trapped in the Si_3N_4 layer of the memory devices with a TANOS structure leak from the trapping layer through various paths. The carrier transport between the conduction band, the trap states in the Si_3N_4 layer, and the leakage paths of the stored charges are illustrated in the energy band diagram in Fig. 1.

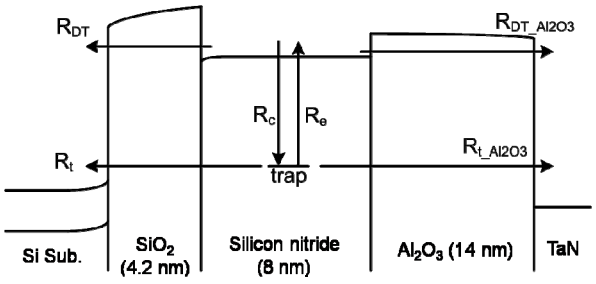

Figure 1. Energy band diagram of charge trap flash memory devices with a TANOS structure containing electron leakage paths.

978-1-61284-418-3/11/$26.00 © 2011 IEEE

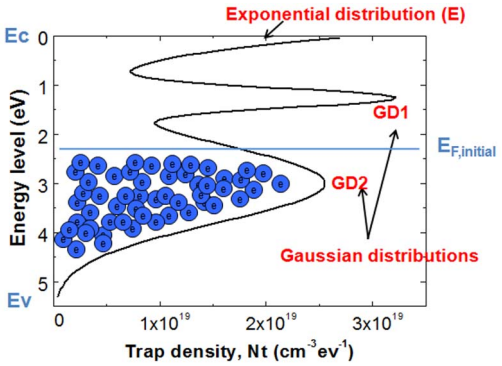

Figure 2. Trap densities as functions of the energy from the conduction band edge to the valence band edge inside the nitride layer.

The trapped electron and free electron densities in the Si_3N_4 layer are calculated by using the two-coupled rate equations utilizing the Shockley-Reed trapping rate model and the thermionic emission model [16, 17]. The trap distribution from the conduction band to the valence band inside the Si_3N_4 layer for the calculation is assumed to be the combination of three groups, as shown in Fig. 2. The determination of the trap distribution of the Si_3N_4 layer in CTF memory devices with a TANOS structure is very important for improving their retention characteristics and device reliabilities. The exponential distribution near the conduction band edge and the Gaussian distribution in the shallow and the deep trap energy levels used in their calculation. The threshold voltage shift of the memory devices at each time step is calculated. The initial Fermi level (E_{F_init}) inside the Si_3N_4 layer before the program operation was aligned with the Fermi level of the Si substrate, which was located between the trap depths of the two Gaussian distributions, the one for shallow traps and the other for deep traps. The electrons injected from the Si substrate during the program operation were simulated by using the Fowler-Nordheim tunneling process. Because the injected electrons were captured in the trap sites existing in the Si_3N_4 layer, the Fermi level and the threshold voltage of the device gradually increased. The threshold voltage shift from the initial threshold voltage (V_{th_init}) during the program operation (ΔV_{th_PGM}) used in this simulation was 3.5 V.

III. Experimental Details

The memory device used in this simulation has a TANOS structure. The thicknesses of the tunneling oxide layer, the charge trap layer, and the blocking oxide layer are 4.2, 8, 14 nm, respectively. The Si_3N_4 materials used in TANOS flash memory devices are two types of the Si-rich silicon nitride and the stoichiometric silicon nitride. During the deposition process of the charge trap layer, the flow rate of the $SiCl_2H_2$:NH_3 gas for the formation of the Si-rich silicon nitride is higher than that for the formation of stoichiometric silicon nitride. The number of the traps in the shallow levels of the Si-rich silicon nitride is higher than that of traps in the stoichiometric silicon nitride [18]. Because the traps in the stoichiometric silicon nitride layer exist far from the conduction band edge in comparison with those in the Si-rich silicon nitride layer, the retention time of the stoichiometric silicon nitride is longer than that of the Si-rich silicon nitride. The exponential distribution of traps near the conduction band edge and the Gaussian distributions of traps in shallow and deep energy levels, respectively, are estimated and then used with the material properties of the Si-rich and the stoichiometric silicon nitride layers, as determined from the experimental results, to investigate clearly the retention characteristics in memory devices with a TANOS structure [18, 19]. The theoretical optimized trap distribution in the silicon nitride layer, taking into account the material properties, was in reasonable agreement with the experimental results [20]. The optimized parameters of the Si-rich and the stoichiometric silicon nitride materials used in this numerical simulation are listed in Table I.

TABLE I. Optimized parameters of Si-rich and stoichiometric Si_3N_4 materials for numerical simulations.

Optimized parameters / Si_3N_4 materials		λ	N_t (cm^{-3}eV^{-1})	E_t (eV)	σ (eV)
Si-rich	*ED*	0.4	3×10^{19}		
	GD1		0.54×10^{19}	1.26	0.08
	GD2		5.21×10^{19}	3.0	0.8
Stoichiometric	*ED*	0.4	3×10^{19}		
	GD1		0.54×10^{19}	1.33	0.08
	GD2		5.29×10^{19}	2.8	0.88

IV. Results and Discussion

Fig. 3 shows the threshold voltage shifts (ΔV_{th}) as functions of the retention time for various (a) total trap densities N_{t0} and (b) trap depths E_t of the Gaussian distribution for traps in shallow energy levels (GD1) at a ΔV_{th_PGM} of 3.5 V. The simulation results show that the retention time increases with increasing total trap density and trap depth of GD1. During program operation, the trap sites inside the Si_3N_4 layer are sequentially filled with injected electrons from the unoccupied trap site of the lowest energy level. When the program operation starts, the position of the Fermi level slowly approaches the conduction band of the Si_3N_4 layer. Because the number of trap sites in the GD1 increases with increasing number of trap sites at energies above E_{F_init}, the Fermi level after program operation is located far from the conduction band edge. Therefore, the trapped electrons are located far away from the conduction band edge of the Si_3N_4 layer and hardly escape, resulting in an increased retention time, as shown in Fig. 3 (a).

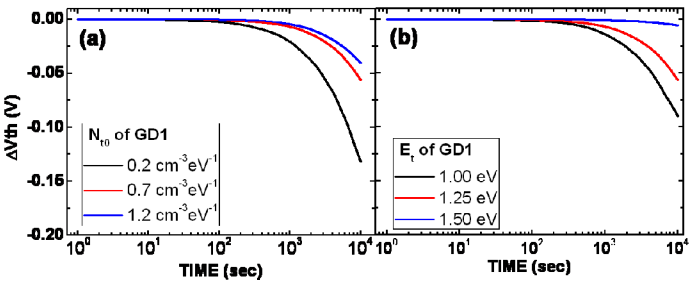

Figure 3. Threshold voltage shifts as functions of the retention time for charge trap flash memory devices with a TANOS structure for various (a) total numbers of trap sites N_{t0} and (b) energy depths Et of the GD1 at a threshold voltage shift of 3.5 V after the program operation.

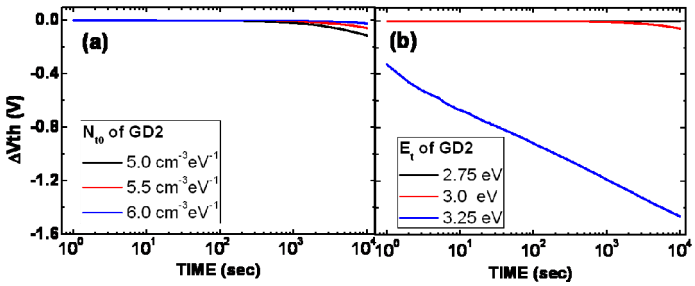

Figure 4. Threshold voltage shifts as functions of the retention time for charge trap flash memory devices with a TANOS structure for various (a) total numbers of trap sites N_{t0} and (b) energy depths Et of the GD2 at a threshold voltage shift of 3.5 V after the program operation.

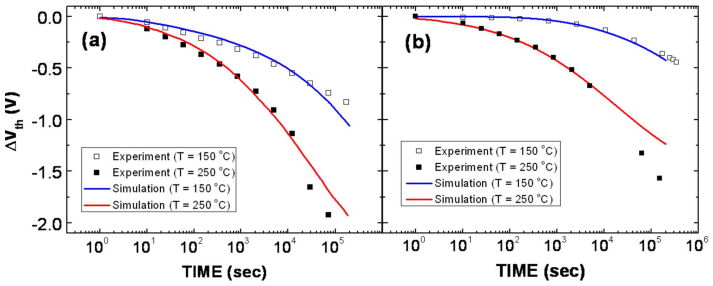

Figure 5. Experimental and simulated threshold voltage shifts as functions of the retention time for charge trapping layers in (a) Si-rich silicon nitride and (b) stoichiometric silicon nitride in TANOS memory devices.

When the trap depth of the GD1 becomes deeper, after program operation with the same threshold voltage shift of 3.5 V, the Fermi level is located far from the conduction band edge, again resulting in an increased retention time.

Fig. 4 shows the threshold voltage shifts as functions of the retention time for various (a) total trap densities N_{t0} and (b) trap depths E_t of the Gaussian distribution for traps in deep energy levels (GD2) at a ΔV_{th_PGM} of 3.5 V. While the retention time increases with increasing total trap density of the GD2, it decreases with decreasing trap depth of the GD2. Because the number of trap sites in the GD2 increases with increasing number of trap sites at energies above E_{F_init}, the retention characteristics of memory devices with a TANOS structure are improved with increasing total trap density in the GD2. However, because almost all of the trap sites in the GD2 are located at energies below the E_{F_init}, the trap sites in the GD2 are almost fully occupied before the program operation, and the variation of the threshold voltage shift with the total trap density N_t of the GD2 is smaller than that of the GD1. The number of trap sites in deep energy levels increases with increasing trap depth of the GD2. However, the number of trap sites between the GD2 and the initial Fermi level decreases with increasing trap depth of the GD2. Therefore, the Fermi level after the program operation is located near the conduction band edge, resulting in a severely degraded retention time for the memory devices with a TANOS structure, as shown in Fig. 4 (b). These results indicate that the trap density near and above E_{F_init} in the silicon nitride layer must be increased to enhance the retention characteristics in TANOS memory devices.

Fig. 5 shows the variations in the retention characteristics for charge trapping layers of (a) Si-rich silicon nitride and (b) stoichiometric silicon nitride in TANOS memory devices at T = 150 and 250°C. The shift in the threshold voltage increases with increasing temperature from 150 to 250°C because of increased leakage of trapped electrons resulting from the thermal emission. The simulation results obtained by using an optimized trap distribution in memory devices with a TANOS structure are in reasonable agreement with experimental results. Because the trap depth of the GD1 in the stoichiometric silicon nitride layer is larger than that of the GD1 in the Si-rich silicon nitride and the trap depth of the GD2 in the stoichiometric silicon nitride layer is smaller than that of the GD2 in the Si-rich silicon nitride, the trap density near and above E_{F_init} in the stoichiometric silicon nitride layer is larger than that near and above E_{F_init} in the Si-rich silicon nitride, resulting in an increased retention time for memory devices with a TANOS structure utilizing a stoichiometric silicon nitride layer.

Fig. 6 shows the threshold voltage shifts as functions of the time in the retention mode for TANOS memory devices for various threshold voltage shifts after program operation, ΔV_{th_PGM}, of (a) 3, (b) 3.5, (c) 4, (d) 4.5, and (e) 5 V. Because the electrons are stored in trap sites in the charge trap layer in TANOS memory devices whereas they are stored at the conduction band edge of the floating gate in conventional memory devices utilizing a floating gate, the retention characteristics of the TANOS memory devices can be changed by varying the number of trapped electrons in the charge trapping layer during the program operation. The retention time of the devices decreases with increasing threshold voltage shift from the initial threshold voltage after the program operation. When the program starts to operate, the trap sites in the Si_3N_4 layer are sequentially filled with injected electrons, resulting in the electron occupation of the trap sites in the lowest energy level. The Fermi level after the program operation is located farther from the conduction band edge with decreasing threshold voltage shift from the initial threshold voltage. Therefore, the electrons are deeply trapped far from the conduction band of the Si_3N_4 layer, resulting in an increased retention time.

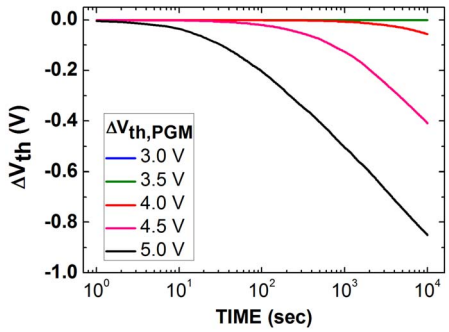

Figure 6. Threshold voltage shifts as functions of the time in the retention mode for TANOS memory devices with threshold voltage shifts after program operation, ΔV_{th_PGM}, of (a) 3, (b) 3.5, (c) 4, (d) 4.5, and (e) 5 V.

V. SUMMARY AND CONCLUSIONS

The effects of the trap density and distribution in the silicon nitride layer on the retention characteristics of TANOS flash memory devices were investigated. The trap distribution of the silicon nitride, estimated from the experimental results, was introduced to investigate the retention characteristics in TANOS memory devices and was composed of an exponential distribution near the conduction band and two Gaussian distributions, one for shallow energy levels and the other for deep energy levels. The retention time increased with increasing total trap density and trap depth of the Gaussian distribution in the shallow energy levels. The retention time increased with decreasing trap depth of the Gaussian distribution in the deep energy levels, and with increasing trap density of the Gaussian distribution in a deep energy level. The simulation results showed that the trap density at energies near and above the initial Fermi level in a silicon nitride layer needs to be increased if the retention characteristics in TANOS memory devices are to be enhanced. The simulation results obtained using an optimized trap distribution in the TANOS structure were in reasonable agreement with the experimental results. The retention characteristics in TANOS memory devices could be changed by varying the threshold voltage shift according to the program operation due to electrons trapped in trap sites.

ACKNOWLEDGMENT

This work was supported by the National Research Foundation of Korea (NRF) grant funded by the Korea government (MEST) (No. 2011-0018877), and this work was also supported in part by the Hynix semiconductor Inc.

REFERENCES

[1] Y. Yang and M. H. White, "Charge retention of scaled SONOS nonvolatile memory devices at elevated temperatures," Solid-State Electron., vol. 44, pp. 949-958, January 2000.

[2] K. A. Nastyrov, V. A. Gritsenko, M. K. Kim, H. S. Chae, S. D. Chae, W. I. Ryu, J. H. Sok, J-W. Lee, and B. M. Kim, "Charge Transport Mechanism in Metal–Nitride–Oxide–Silicon Structures," IEEE Electron Device Lett., vol. 23, pp. 336-338, June 2002.

[3] Y, Wang, Y. Zhao, B. M. Khan, C. L. Doherty, J. D. Krayer, and M. H. White, "A novel SONOS nonvolatile flash memory device using substrate hot-hole injection for write and gate tunneling for erase," Solid-State Electron., vol. 48, pp. 2031-2034, June 2004.

[4] C. M. Compagnoni, A. Mauri, S. M. Amoroso, A. Maconi, and A. S. Spinelli, "Physical Modeling for Programming of TANOS Memories in the Fowler–Nordheim Regime," IEEE Trans. Electron Devices, vol. 56, pp. 2008-2015, September 2009.

[5] Y. Wang and M. H. White, "An analytical retention model for SONOS nonvolatile memory devices in the excess electron state," Solid-State Electron., vol. 49, pp. 97-107, August 2005.

[6] J. H. Yi, S. D. Lee, J. H. Ahn, H. C. Shin, Y. J. Park, and H. S. Min, "Device degradation model for polysilicon-oxide-nitride-oxidesilicon (SONOS) based on anode hole fluence," Microelectronic Eng., vol. 80, pp. 329-332, June 2005.

[7] A. Furnémont, M, Rosmeulen, K. Zanden, J. V. Houdt, K. D. Meyer, and H. Maes, "Root Cause of Charge Loss in a Nitride-Based Localized Trapping Memory Cell," IEEE Trans. Electron Devices, vol. 54, pp. 1351-1359, June 2007.

[8] Y.-H. Hsiao, H. -T. Lue, T.-H. Hsu, K.-Y. Hsieh, and C.-Y. Lu, "A critical examination of 3D stackable NAND flash memory architectures by simulation study of the scaling capability," Proceeding of the International Memory Workshop (IMW), pp.1-4, May 2010.

[9] M. Chang, M. Jo, S. Kim, Y. Ju, S. Jung, J. Lee, J. Yoon, H. Hwang, and C. Lee, "Charge loss behavior of a metal-alumina-nitride-oxide-silicon-type flash memory cell with different levels of charge injection," Appl. Phys. Lett., vol. 93, pp. 232105-3, December 2008.

[10] A. Padovani, L. Larcher, D. Heh, G. Bersuker, V. D. Marca, and P. Pavan, "Temperature effects on metal-alumina-nitride-oxide-silicon memory operations," Appl. Phys. Lett., vol. 96, pp. 223505-3, June 2010.

[11] G. Molas, M. Bocquet, E. Vianello, L. Perniola, H. Grampeix, J.P. Colonna, L. Masarotto, F. Martin, P. Brianceau, M. Gély, C. Bongiorno, S. Lombardo, G. Pananakakis, G. Ghibaudo, and B. De Salvo, "Reliability of charge trapping memories with high-k control dielectrics," Microelectronic Eng., vol. 86, pp. 1796-1803, March 2009.

[12] E. Vianello, F. Driussi, A. Arreghini, P. Palestri, D. Esseni, L. Selmi, N. Akil, M. J. van Duuren, and D. S. Golubovic, "Experimental and Simulation Analysis of Program/Retention Transients in Silicon Nitride-Based NVM Cells," IEEE Trans. Electron Devices, vol. 56, pp. 1980-1990, September 2009.

[13] E. Gnani a, S. Reggiani, A. Gnudi, G. Baccarani, J. Fub, N. Singh, G.Q. Lo, and D.L. Kwong, "Modeling of gate-all-around charge trapping SONOS memory cells," Solid-State Electron., vol. 54, pp. 997-1002, May 2010.

[14] A. Arreghini, N. Akil, F. Driussi, D. Esseni, L. Selmi, and M.J. van Duuren, "Long term charge retention dynamics of SONOS cells," Solid-State Electron., vol. 52, pp. 1460-1466, May 2008.

[15] E.Vianello, E.Nowak, L.Perniola, F. Driussi, P.Blaise, G.Molas, B.De Salvo, and L.Selmi, "A Consistent Explanation of the Role of the SiN Composition on the Program/Retention Characteristics of MANOS and NROM like Memories," Proceeding of the International Memory Workshop (IMW), pp.106-109, May 2010.

[16] S. H. Gu, C. W. Hsu, T. Wang, W. P. Lu, Y. H. J. Ku, and C. Y. Lu, "Numerical simulation of bottom oxide thickness effect on charge retention in SONOS flash memory cells," IEEE Trans. Electron Devices, vol. 54, pp. 90-97, January 2007.

[17] J. Frenkel, "On pre-breakdown phenomena in insulators and electronic semiconductors," Phys. Rev., vol. 54, pp. 647-648, 1938.

[18] T. H. Kim, I. H. Park, J. D. Lee, H. C. Shin, and B. G. Park, "Electron trap density distribution of Si-rich silicon nitride extracted using the modified negative charge decay model of silicon-oxide-nitrideoxide-silicon structure at elevated temperatures," Appl. Phys. Lett., vol. 89, pp. 063508-3, August 2006.

[19] Y. J. Seo, K. C. Kim, H. D. Kim, M. S. Joo, H. M. An, and T. G. Kim, "Correlation between charge trap distribution and memory characteristics in metal/oxide/nitride/oxide/silicon devices with two different blocking oxides, Al_2O_3 and SiO_2," Appl. Phys. Lett., vol. 93, pp. 063508-3, August 2008.

[20] V.A. Gritsenko, S.S. Nekrashevich, V.V. Vasilev, and A.V. Shaposhnikov, "Electronic structure of memory traps in silicon nitride," Microelectronic Eng., vol. 86, pp. 1866-1869, March 2009.