A Novel Simulation Methodology for Development of ESD Primitives on a 0.18µm Analog, Mixed-Signal High Voltage Process Technology

Frederic Roger, Juri Cambieri, Rainer Minixhofer
Austriamicrosystems
Tobelbaderstrasse 30, 8141 Schloss Premstatten, Austria
e-mail: frederic.roger@austriamicrosystems.com

Abstract—**This paper presents a full simulation methodology dedicated to the ESD primitive devices development in High Voltage technology. This workflow based on layout generation, 2D, 3D and mixed-mode TCAD simulations and SPICE simulations provide robust devices sustaining ESD stress tests.**

Keywords: ESD; 2D and 3D TCAD simulation; Mixed-mode simulations; SPICE; 0.18µm High voltage technology.

I. INTRODUCTION

Electrostatic discharge (ESD) is a major problem in low voltage and high voltage integrated circuits or analog designs where this discharge can be the source of more than 20% of design failure [1]. The development and optimization of ESD protection and their primitive elements is a key task of treating this problem. We propose a novel and robust development methodology based on a complete and predictive simulation workflow. It includes layout generation, process and device TCAD and provides robust devices sustaining the required ESD stress tests like TLP, HBM or Latchup.

II. ESD PRIMITIVE DEVELOPMENT

Following the simulation methodology shown in Fig. 1, we can provide solution components for the ESD protection. Two main ESD primitive elements, out of the complete ESD protection library of a 0.18 µm analog mixed-signal high voltage process technology, described in detail in [2], namely forward and trigger diode, are specifically studied in this work.

A trigger diode is a diode operated in reverse direction which has to provide the reference voltage for clamping the whole integrated circuit at a certain voltage given by the “ESD design window” [3],[4]. By performing several experiments with TCAD process simulation using different, parameterized layout geometries and doping distributions, the target devices, meeting the breakdown value specifications, are selected. Fig. 2 shows the resulting layout of a 20V operating voltage trigger diode and its 2D process simulation structure.

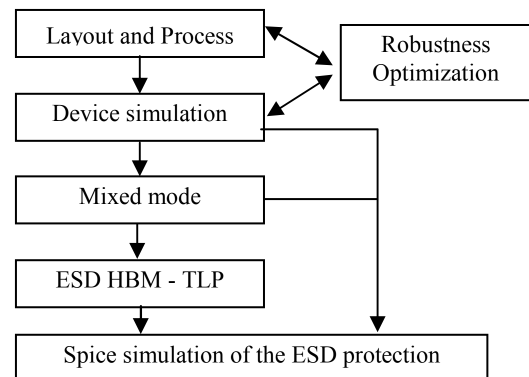

Figure 1. Simulation methodology

Calibrated 2D DC simulations match the experimental results with a breakdown of 24V. Since the devices have to sustain high currents during the ESD event, robust devices are mandatory. Current filamentation at the corners of the device during breakdown has to be prevented and the layout has to be optimized to remove this weak spots. 3D TCAD simulations show that the original layout experiences breakdown at the corners, an observation confirmed by EMMI measurements (Fig. 3). The chamfered and optimized layout is simulated in 3D and shows a far better distribution of the current during breakdown along the edge of the device (Fig. 4).

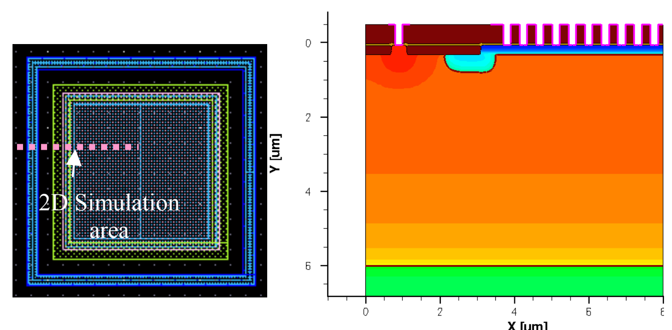

Figure 2. Trigger diode layout and 2D TCAD simulation with doping concentration

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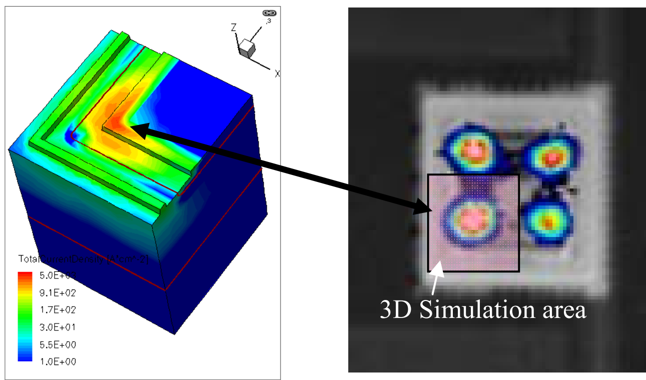

Figure 3. 3D TCAD simulation with current density during breakdown operation compared to EMMI picture on Silicon

In addition to trigger diodes, forward diodes which are used in forward mode and have to conduct the ESD current with the lowest possible resistivity are developed in a similar way. In addition to standard DC characteristics, transient and mixed-mode simulations are used to model the standard ESD stress characterization methods with TLP and HBM pulses [5]. TLP measurements provide insight into ESD failure threshold through offering I-V characteristics by using very short time pulses where self-heating does not occur excessively. TLP TCAD simulations [5] are done in forward mode of the diode (Fig. 5) with different pulse widths (100ns down to 5ns) and compared to measurements, showing excellent agreement. These results highlight the predictability of our proposed method and the robustness to high current levels (up to 8A, equivalent to 12kV HBM) of the forward diode.

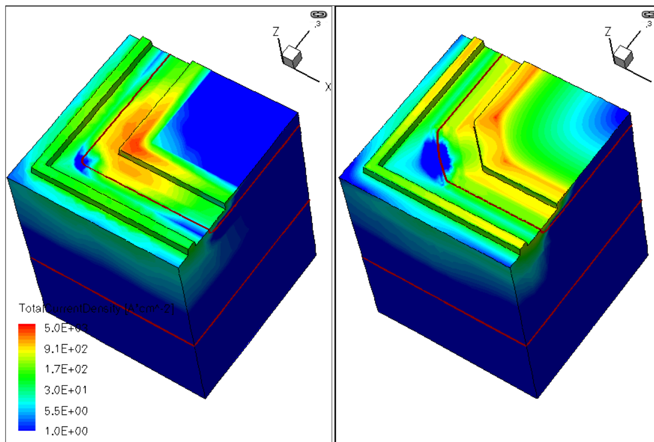

Figure 4. Robustness improvement by cutting the corner of the Trigger diode (right), current density distribution moving from the corner (left) to the edge (right).

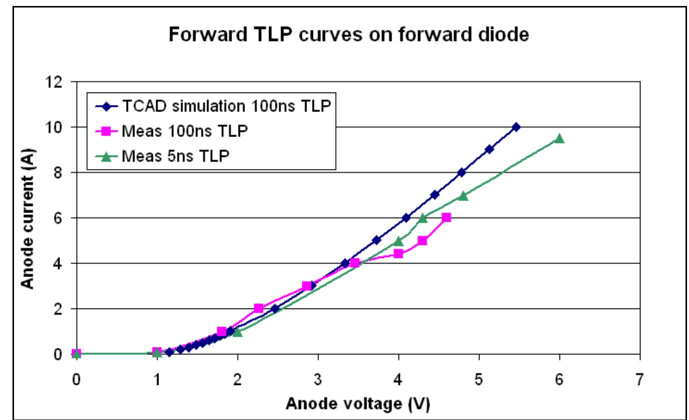

Figure 5. TLP TCAD simulation on forward mode compare to measurement with different pulse width (100ns and 5ns)

Furthermore HBM mixed mode simulations and transient I-V measurements are done on this device. During the so called "mixed mode" HBM simulations, the forward diode is represented as fully meshed TCAD device, while the rest of the circuit is specified by a netlist and the respective spice parameters of its circuit elements. Several HBM levels (300V, 400V and 700V) are simulated and compared with the transient I-V measurements of the experiment (Fig. 6). The device is failing at 700V (measurement curve discontinuity) because of thermal destruction related to the relatively small size of the diode (area of 300µm²).

The respective relevant electrical parameters of the two ESD primitives such as breakdown value and leakage current for the trigger diode and forward resistance and high current level capability of the forward diode are extracted as SPICE parameters. Finally the full ESD protection schematic is simulated using above described methodology. Fig. 7 presents the comparison of the simulation to experiment for a 2kV HBM pulse with a good agreement, highlighting the quality of the methodology.

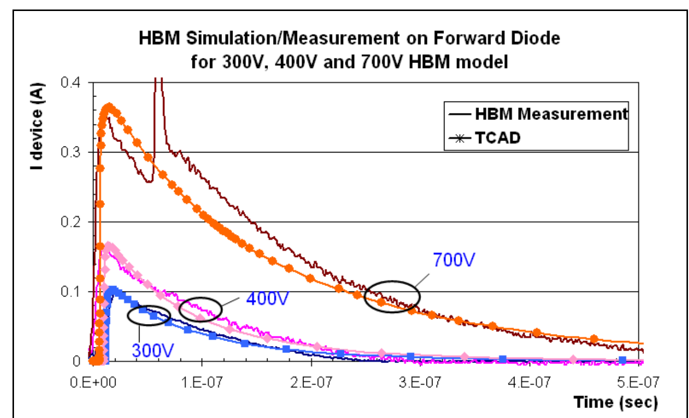

Figure 6. HBM TCAD simulation and experiments on forward diode before device failure (300V, 400V and 700V HBM)

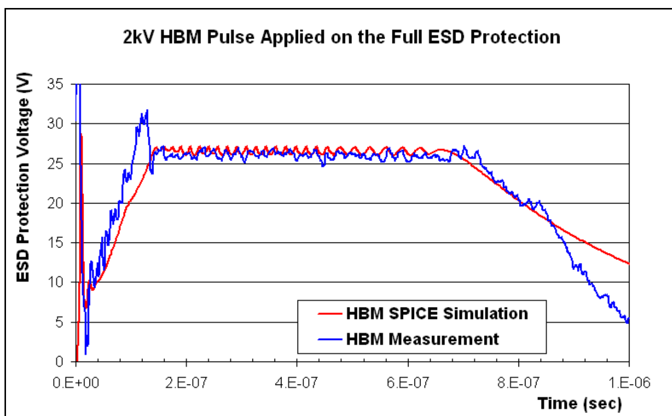

Figure 7. Full ESD Protection Voltage comparison between SPICE simulation and Measurement during 2kV HBM pulse

III. CONCLUSION

This paper presents a novel, predictive and complete methodology for the development of robust ESD primitive devices. This methodology, based on calibrated TCAD simulations including mixed-mode ESD stress simulations and 3D process and device simulations, provides very clear understanding of the devices and then in turn, of the circuit protection. SPICE parameters which can be used for SPICE modeling of the whole ESD circuit protection can be extracted. This feature permits the further optimization of the overall ESD protection by pure SPICE simulations and before any experimental Silicon has been processed.

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